IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

DESIGN OF DELAY AND DOPPLER MODULE FOR ECM SYSTEM BASED ON DRFM TECHNIQUE

[1]Vaddi Jhansi

[1]Post Graduation student, Department of ECE, JNTUK, UCEK, Kakinada, Andhra Pradesh, India

Abstract: Electronic Warfare is much more evolved than most other domains of information security. The most often exercised electronic warfare types are jamming, which comes under the division of Electronic Counter Measures(ECM). The purpose of jamming is to restrict an opponent's capability to exchange data by overriding radio transmissions or by sending electronic signals to prevent or disrupt radar detection or convey false information. A number of advanced techniques are used earlier to give us an edge from information warfare. But the emergence of jammers based on digital radio frequency memory holds out the prospect of much more complex attack and defence. DRFM Jamming is a repeater technique, that manipulates received radar energy and retransmits it to change the skin return, the radar perceives. This technique can change the range which radar detects, by changing the delay in transmission of pulses and the velocity which radar detects by changing the Doppler shift of the transmitted signal. There are very few ECM Systems that are available in the global scenario, that have public information. This paper aims at minimization of the architecture of the ECM Systems, such that it can be easily ported in any air based defence/flight. This project discusses the implementation of memory controller for delay modulation and for simulation of delay and Doppler in ECM System. Various performance scenarios are being realized, tested and documented in this paper.

Index Terms **– Digital Radio Frequency Memory, DRFM jamming, Electronic Counter Measures, false target generation.**

I. INTRODUCTION

Digital Radio Frequency memory (DRFM) is one of the prime technology that is leading the modern electronic warfare. DRFM is an electronic technique which uses high speed sampling and digital memory to capture and store the radio frequency and microwave signals and retransmits the digitally modified signals. This ability to store and recall can be put to use in many potential applications. Currently the most attention of DRFM technology is being directed to electronic warfare applications, in particular, for generation of false targets to dupe hostile radar systems.

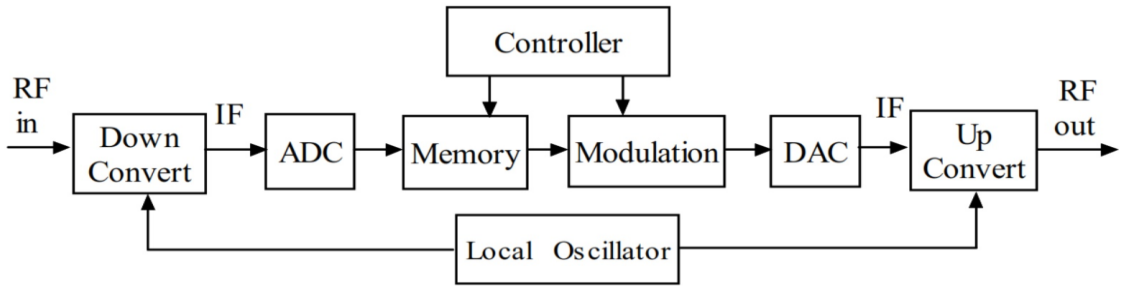

Fig.1: Block Diagram Of Digital Radio Frequency Memory

A simple block diagram of a digital radio frequency memory system is shown in figure 1. The incoming RF signal is received and down converted to an intermediate frequency (IF). The IF signal is sampled by high speed analogue to digital converter(ADC), and the resulting samples are stored in a high speed digital memory. These stored samples can be manipulated in amplitude, frequency and phase to generate false target signals. The memory controller module adds the desired delay and doppler shifts to simulate the false target range and velocity. This reconstructed digital signal is then up converted back to RF frequency and retransmitted. The local oscillator(LO) used for down conversion and up conversion is same to make sure the transmitted signal is coherent with input signal. The DRFM memory controller simulates any target by maintaining the coherency of incoming signal and altering the phase of the signal. The high speed DRFM should be dual ported so that radio signals are recorded and replayed simultaneously. A DRFM is an attractive way of implementing a false target system for following reasons:

- Once a radar signal has been intercepted and digitized it may be stored indefinitely without degradation in contrast to analogue storage methods.
- With a suitable high speed memory design, several targets either stationary or moving objects are simultaneously recreated with different delays and doppler

II DELAY MODULE AND DOPPLER MODULE

2.1 DISTANCE DECEPTION USING DELAY MODULE

The received radar signal is delayed, modulated and amplified to distance deceive the pulse radar. The delay module is implemented by using a dual ported RAM block. The received input signal is stored in the RAM and periodically the time delays are injected. This modified signal is then amplified and retransmitted much stronger than the return signal. By increasing these time delays, the radar gate will detect an increase in the range and move off to false target.

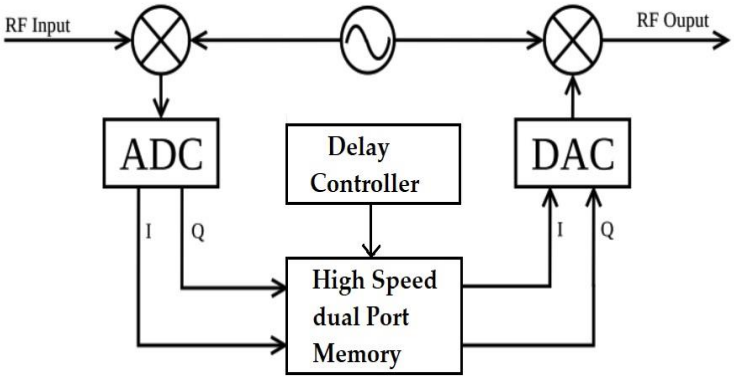

Fig.2: Block Diagram Of Delay Module

The time delay operation is mathematically expressed as:

$$S_{delay}(n, k) = S_{rx}(n-k),\ n \geq k \qquad (1)$$

Where $S_{delay}(n, k)$ = time delayed representation of input signal $S_{rx}(n)$.

The time delay of radar pulse is given as:

$$t_r = {}^{2R}/_{C} \qquad (2)$$

Where R = real distance between radar and target.

C = Speed of the light

When time delay is introduced to the radar signal, the delay of radar pulse is given as:

$$t_f = {}^{2R_f}/_{C} \qquad (3)$$

Where R_f = distance between radar and false target.

When the user enters the delay input values, a digital sorter program is used to sort the delay inputs in ascending order and is fed to a down counter. After each delay input is count down to zero, the input signal sample may be outputted every clock cycle. This modulated signal is then further fed to doppler module so that the output signal can be quadrature modulated.

2.2 VELOCITY DECEPTION USING DOPPLER MODULE

The frequency difference been transmitting and receiving signals is used by the radar to get the target speed information of the aircraft. When the frequency of received signal is different from the transmitted signal, doppler effect will occur. Based on the doppler shift, the speed tracking system of radar can easily capture the target. We make use of the doppler module to deceive the radar successfully.

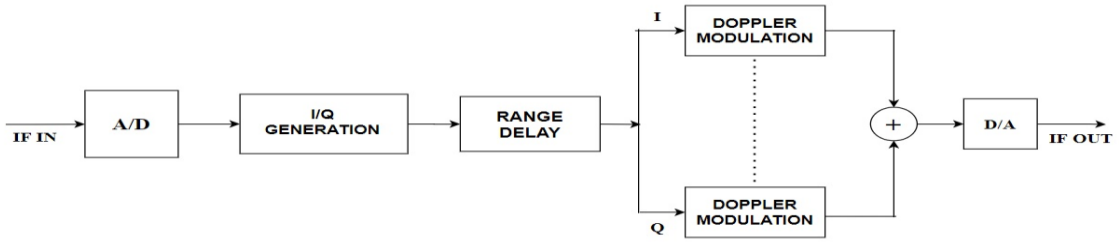

Fig.3: Block Diagram Of Velocity False Target Generation In DRFM

The conventional block diagram of delayed, modulated and doppler shifted DRFM architecture is shown in Fig.3. The received IF signal is sampled and further decomposed to I/Q components and stored in memory, which is recalled for false range target generation. The doppler module block is used to induce doppler shift using direct digital synthesizers(DDS), a digitally controlled method for generating multiple frequencies from a reference frequency source. The multiple signals with different time delays and doppler shifts are summed to convert them into real signal and passed through digital to analogue converter(DAC) to generate the analogue signal. To generate multiple velocity false targets at different doppler frequencies multiple DDS are required.

The mathematical representation of the frequency shifting model carried out on the DRFM system can be shown as:

$$S_s(n) = S_{rx}(n)e^{j2\pi f_s n} \quad (4)$$

Where $S_s(n)$ = shifted version of $S_{rx}(n)$,

f_s = frequency shift.

By expanding the complex exponential term using the I/Q signal model we can see that:

$S_s(n) = [I(n)+j\ Q(n)][Cos(2\pi f_s n)+j\ Sin(2\pi f_s n)]$

$= [I(n)\ Cos(2\pi f_s n) – Q(n)\ Sin(2\pi f_s n)] +$

$j\ [I(n)\ Sin(2\pi f_s n)]+Q(n)\ Cos(2\pi f_s n)]$

$= I_S(n) + j\ Q_s(n)$ (5)

Where $I_S(n)$ = real frequency shifted component

$j\ Q_s(n)$ = complex frequency shifted component.

To create multiple frequency shifts at the same time, these equations can be extended as:

$I_S(n) = I(n)\sum_{n=1}^{N} Cos(2\pi f_{s,n} n) – Q(n)\sum_{n=1}^{N} Sin(2\pi f_{s,n} n)$ (6)

$Q_s(n) = I(n)\sum_{n=1}^{N} Sin(2\pi f_{s,n} n) + Q(n)\sum_{n=1}^{N} Cos(2\pi f_{s,n} n)$ (7)

Where $f_{s,n}$ = multiple doppler shifts for n= 1,2,…N.

It can be seen that, to generate frequency shift at same time, multiple Sin/Cos operations are necessary. This can be done using single multiplexed or multiple DDS IP cores.

III DESIGN OF DOPPLER MODULE

The general block diagram of the proposed multiple velocity target generation module consists of three main blocks each having specific tasks.

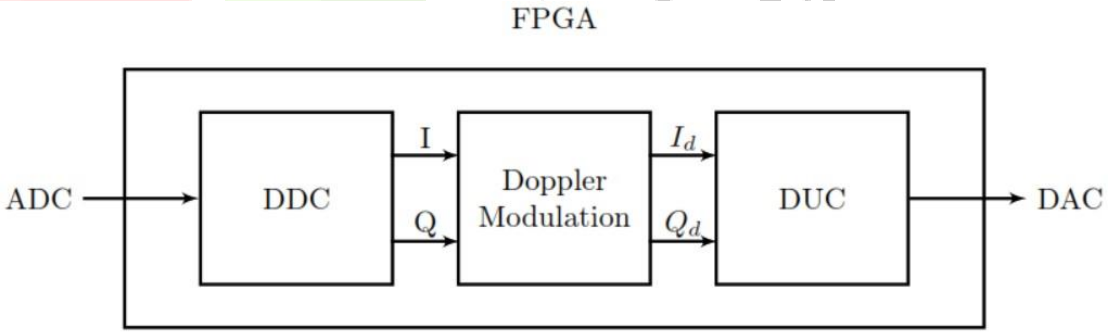

Fig.4: Block Diagram Of Multiple VFT Generation Module

3.1 DIGITAL DOWN CONVERTER (DDC):

The input signal from ADC is down converted using the DDC block. The DDC block is also designed to generate I/Q components.

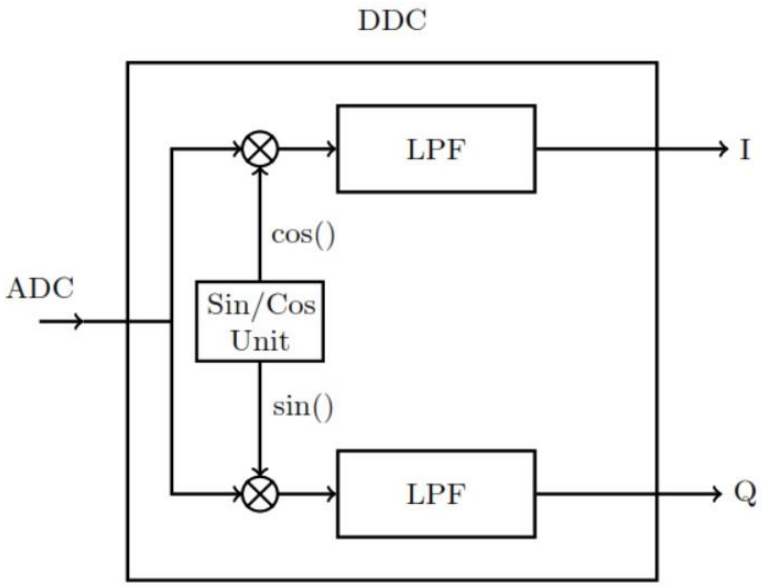

Fig.5: Block Diagram Of DDC

The down converted digital IF signal is received by the DDC. The DDC block modulates the signal to produce two baseband signals, in-phase signal and quadrature-phase signal, as outputs. The quadrature modulation is implemented by multiplying the sampled IF signal with Sin/Cos operations. Then the I and Q components are obtained after passing the modulated signals through low pass filter(LPF).

3.2 MULTIPLE DOPPLER MODULATION:

Multiple doppler modulation block can generate multiple frequency shifts by inducing multiple doppler shifts to the incoming signal using two methods such as DDC blocks and Inverse Fast Fourier Transform (IFFT) operation.

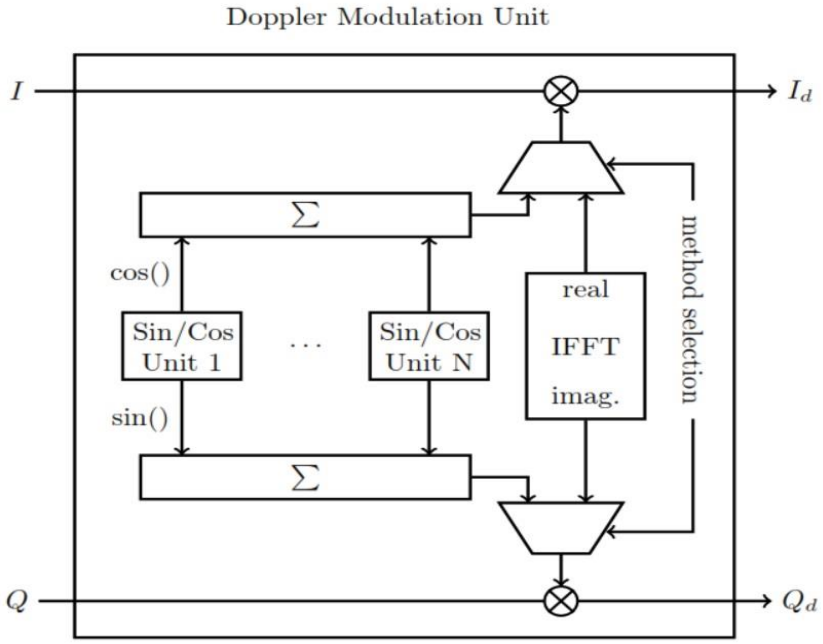

Fig.6: Block Diagram Of Bank Of Sin/Cos Units

Multiple Cos/Sin operations are done simultaneously using the bank of Cos/Sin generators. The modulated Cos/Sin signals are added and mixed with the incoming I/Q signals. The IFFT is designed to generate the sum of multiple frequency sinusoids. Instead of generating $\mathrm{Sin}(2\pi f_{s,n} n)$ or $\mathrm{Cos}(2\pi f_{s,n} n)$ in time domain for different $f_{s,n}$ values and summing them up, IFFT generates the sum by supplying related frequency, phase and amplitude values. The addition of parallel sinusoids signals can be implemented with much easier control over multiple doppler frequencies.

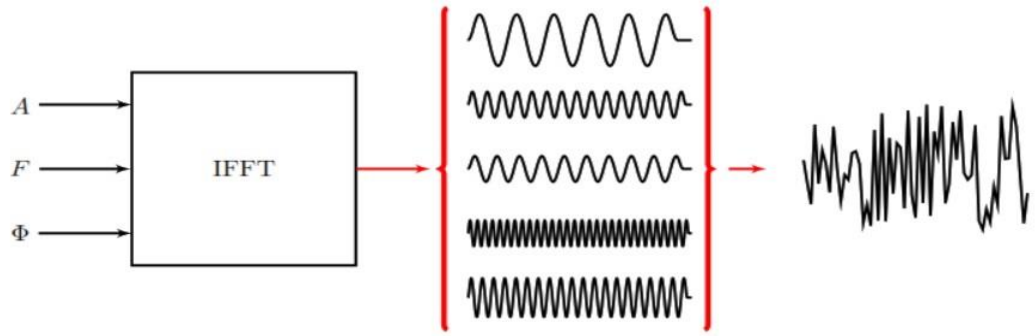

Fig.7:Sum Of Parallel Sins With IFFT

Corresponding IFFT bins must be selected to generate false target velocity signals with IFFT and the amplitudes are adjusted for both real and imaginary parts. The selection of corresponding frequency bin depends upon:

$$IFFT_{bin} = \frac{F_i \times F_S}{F_S/N} = \frac{F_i}{N} \quad (8)$$

Where $IFFT_{bin}$ = Corresponding frequency bin number

F_i = Frequency value generated in the specified interval

F_s = Sampling frequency

3.3 DIGITAL UP CONVERTER (DUC)

The DUC block modulates the in-phase and quadrature-phase base band signals into a single real bandpass signal.

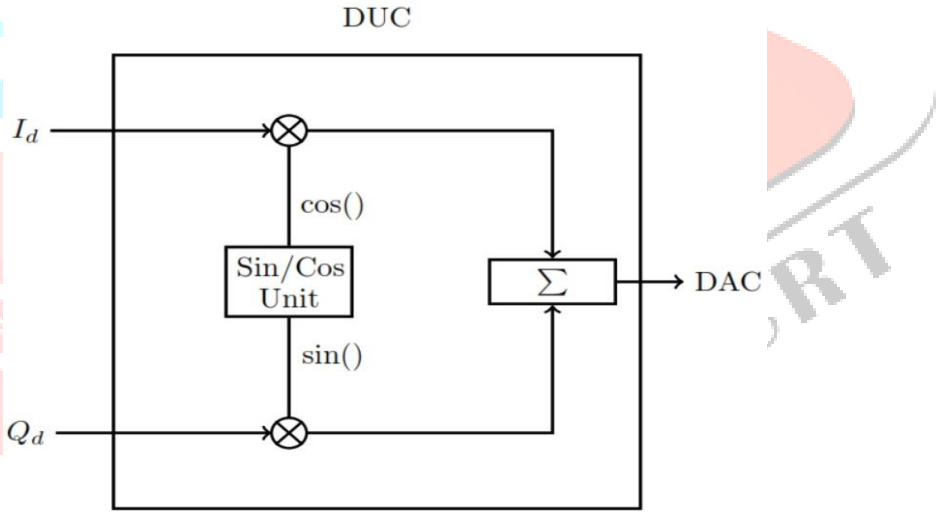

Fig.8: Block Diagram Of DUC

IV DRFM BASED RADAR TARGET SIMULATOR

The basic concept of Radar target simulator (RTS) is to electronically generate the Radar illuminated environment without switching on actual Radar transmitter in the field. These Radar target simulators are used to develop, optimize, and test the Radar System and to generate false targets for radar.

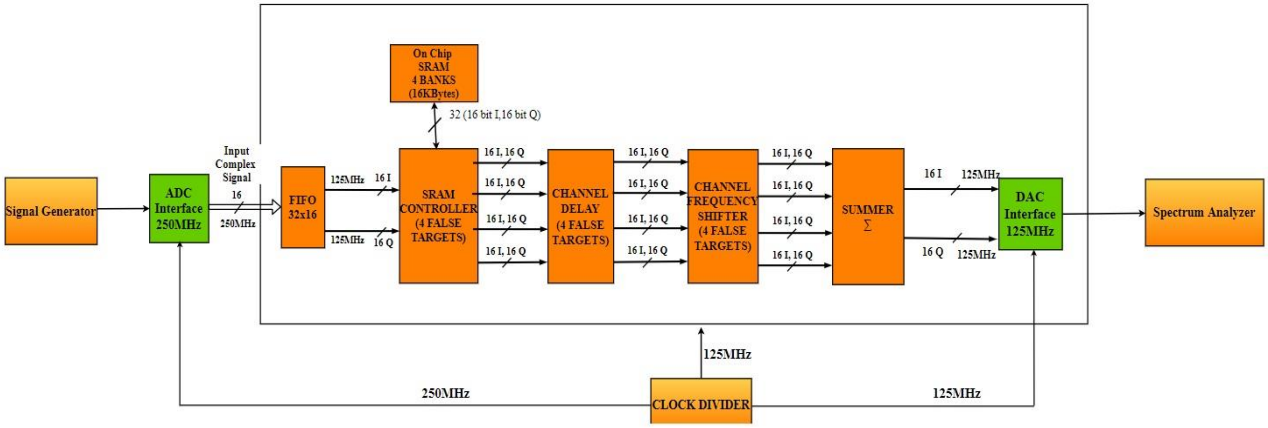

Fig.9: Block Diagram Of DRFM Based Radar Target Simulator

The DRFM is the heart of the radar target simulator.

- A signal generator is used to produce a test input signal with various patterns of voltage at a variety of frequencies and amplitudes. A common use is to test the response of circuits to a known input signal.
- The generated sine signal is sampled through an ADC interface to produce a 16-bit input complex signal.
- The sampled signal is further decomposed into I and Q components and stored in the on-chip SRAM memory module.
- The SRAM controller generated four false targets by passing the input signals through delay channel and frequency shifter channel.
- The time delayed and Doppler induced multiple signals are summed, converted to real signal and passed through DAC to generate the analog signal.
- The final output signal is fed to spectrum analyzer block to test and verify doppler module performance.
- The Spectrum Analyzer System displays the frequency spectrum of time-domain signals.
- The frequency spectrum of a signal is used to observe the overall spectrum of a modulated signal to see whether it is wide enough or too narrow, etc. and To find out whether a signal is on the right frequency, and not in another band for example.
- The final output false target signals appear at the radar receiver as time delayed, amplitude scaled and frequency shifted coherent replica of the original signal, thereby making it, from the radar's perspective, indistinguishable from other genuine signals.

In this way the targets are created or simulated in the radar target simulator. The radar target simulator can also be used to test or calibrate the radar performance and also used in the electronic countermeasure systems.

V SIMULATED OUTPUT RESULTS

4.1 DELAY MODULE RESULTS

The Delay module was synthesized in 28nm TSMC HPC library at rated Clock frequency of 400MHz and the Netlist was simulated without Standard Delay Format in QuestaSim Simulator. The four false targets were simulated with delay values of 16, 32, 64, 80 clock cycles to simulate range deception of 6m to 30 m range.

Delay values in terms of Clock of 2.5ns (400MHz)

Delay of false target1 :- 2.5ns x 16 = 40ns
Delay of false target2 :- 2.5ns x 32 = 80ns
Delay of false target3 :- 2.5ns x 64 = 160ns
Delay of false target4 :- 2.5ns x 80 = 200ns

Specification:-100µsec=15km range as per(R=CT/2)

False target 1 range 40ns = 6 m range
False target 2 range 80ns = 12 m range
False target 3 range 160ns = 24 m range
False target 4 range 200ns = 30m range

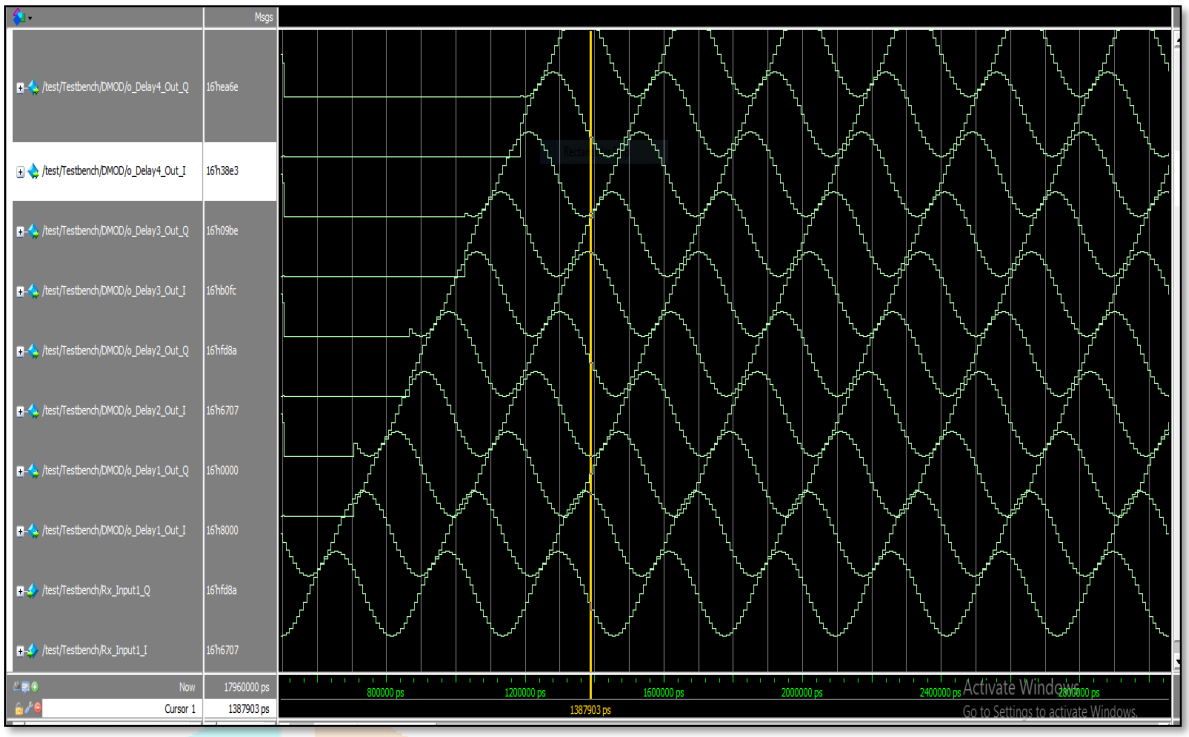

Fig.10: Simulation Results Of Delay Channel

4.2. DOPPLER MODULE RESULTS

The in-phase (real) signals of the four velocity false targets are summed to form single real bandpass signal. Similarly the quadrature-phase (imaginary) signals of the four VFT's are integrated to form single imaginary bandpass signal.

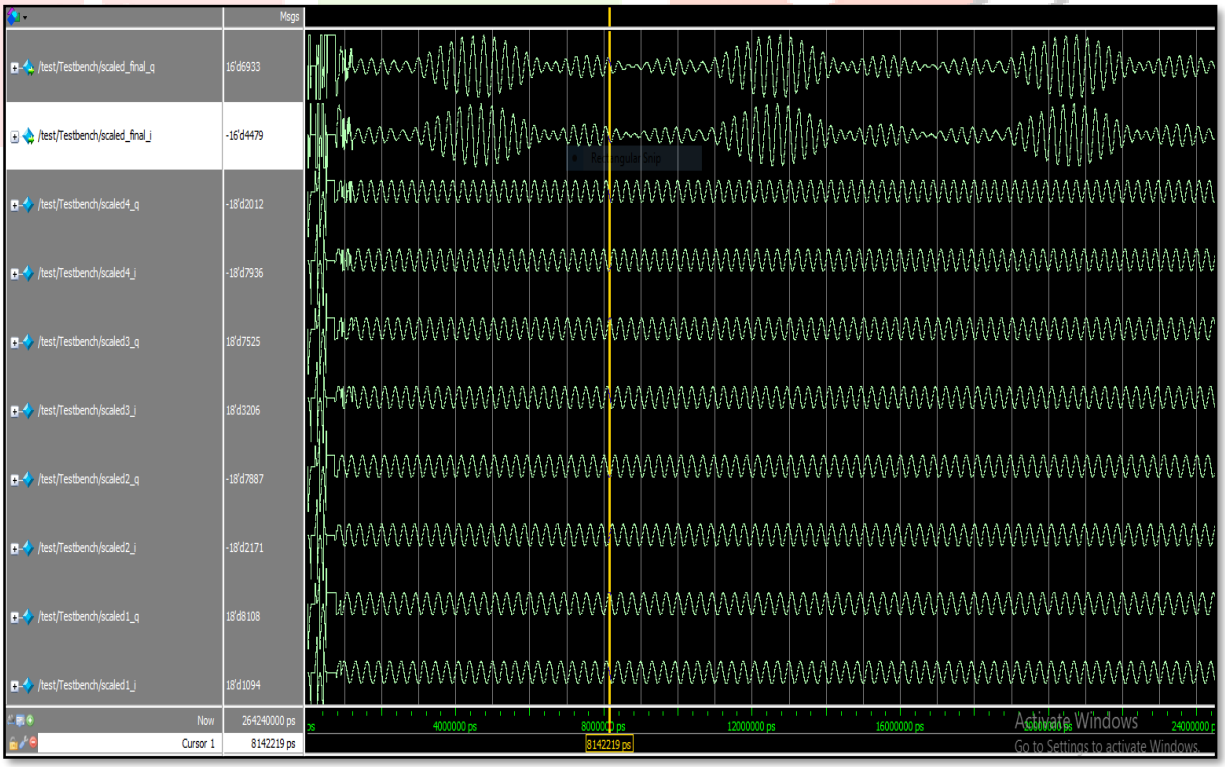

Fig.11: Simulation Results Of Doppler Channel

Doppler shifted spectral plotted for four false targets with frequency shift of 1MHz in each of the targets. The Center frequency chosen is 12.5MHz single tone

- False target1 :- 13.5MHz
- False target2 :- 14.5MHz
- False target3 :- 15.5MHz

- False target4 :- 16.5MHz

The autocorrelation between the frequency shifted signals can be assessed using the spectral plot. Spectral analysis studies the frequency spectrum contained in discrete, uniformly sampled data.

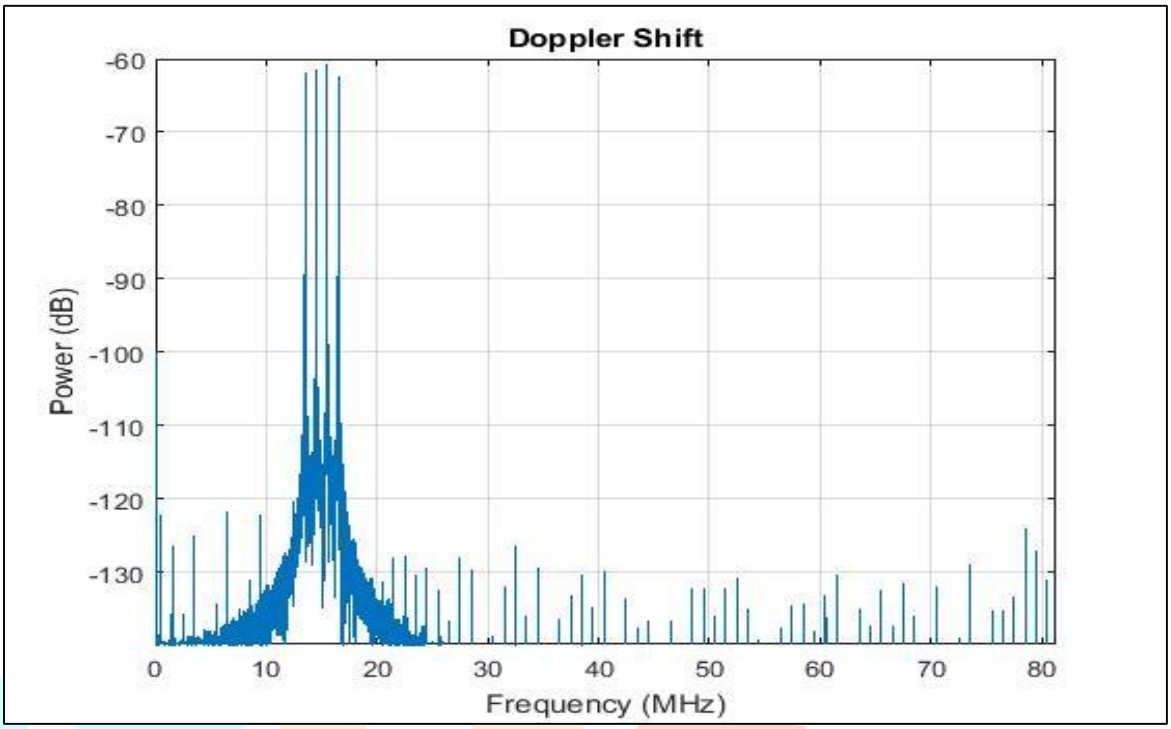

Fig.12: Spectral Plot Of Doppler Shifted Targets

VI CONCLUSION

Frequency shifts corresponding to various false target doppler shifts can be seen in the spectral plot of the doppler shifted targets Fig.12, along with time delayed false targets shown in Fig.10. These results exhibit the system is capable of inserting a false target into a received signal at a particular time delay and doppler frequency shift. Finally, the radar target simulator is designed to simulate or generate the false targets with the help of delay module and doppler module. Digital radio frequency memory with the above explained deception modules are designed and simulated in QuestaSim and MATLAB and the same is tested for results with various arbitrary time delays and at different frequencies. Finally, the output results are observed to be in coherent with the applied delay and frequency values.

REFERENCES

[1] S. J. Roome, "Digital radio frequency memory," Electronic & Communication Engineering Journal, pp. 147–153, August 1990.

[2] K. Olivier, J. E. Cilliers, and M. du Plessis, "Design and performance of wideband drfm for radar test and evaluation," Electronics Letters, vol. 47, no. 14, pp. 824–825, July 2011.

[3] M. Xie, J. Huang, Y. Jiang, and X. Fu, "Design and realization of drfm system based on fpga and dsp," in IET International Radar Conference 2015, Oct 2015, pp. 1–6.

[4] Olivier, K.; Gouws, M. "Modern wideband DRFM architecture and real-time DSP capabilities for radar test and evaluation", Electronics, Communications and Photonics Conference (SIECPC), 2013 Saudi International, Vol.3, No. 4, pp. 82-85, July 2013.

[5] Liu Kui, Yan Xue-long, Guan Shi-you, Zhao Zhi-qiang, "DRFM design for radar multi-target simulator based on FPGA" , Application of Electronic Technology, Vol.32, No.5, 2011, pp.52-55.

[6] Jiang Changyong, Gao Meiguo, Wang Zongbo, Fu Xiongjun, "Design of highspeed DRFM system", WRI World Congress on Computer Science and Information Engineering, vol. 3, IEEE, 2009, pp. 582–586.

[7] Michael B. Mesarcik , Daniel W. O'Hagan, Stephen Paine, "Low Cost FPGA based Implementation of a DRFM System", IEEE Radar Conference , Sept 2019.

[8] Wang Zongbo, Gao Meiguo, Li Yunjie, Jiang Haiqing, "Design and application of DRFM system based on digital channelized receiver", International Conference on Radar, September 2008.

[9] Sun Guoying, Yunjie Li, Gao Meiguo, "An Improved DRFM System Based on Digital Channelized Receiver", Image and Signal Processing Conference, Nov 2009.

[10] Mehmet İspir, Adnan Orduyılmaz, Mahmut Serin, Alper Yıldırım, Ali Cafer Gürbüz, "Real-time multiple velocity false target generation in digital radio frequency memory", IEEE Radar Conference (RadarConf), May 2016.