



Study of Power Efficient Dual Edge triggered Sense Amplifier flip-flop with its architectures

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Abstract: In synchronous or clocked sequential networks, clocked flip-flops are used as memory elements, which change their individual states in synchronism with the periodic clock signal. Therefore, the change in status of flip-flops and change in state of the entire circuit occurs at the transition of the clock signal. The key to the proper operation of a flip-flop is to trigger it only during a signal transition. A clock pulse goes through two transitions from 0 to 1 and the return is from 1 to 0. The positive transition is defined as the positive-edge and the negative transition as the negative-edge. The single-edge triggered flip-flop (SETFF) fetches the data either on the rising or the falling edge of the clock cycle, but dual edge triggered sense amplifier flip-flop (DETSAFF) utilizes both the edge of the clock signal. The clock gating is another popular technique to reduce the dynamic power consumption when the system is idle. We give a wide knowledge of the DETSAFF and study has been made on several DETSAFF architectures by reviewing several papers.

Index Terms - single edge triggered flip-flop (SETFF), dual edge triggered sense amplifier flip-flop (DETSAFF), clock gating, conditional precharge flip-flop (CPFF), conditional capture flip-flop (CCFF), conditional discharge flip-flop (CDFF).

I. INTRODUCTION

In very large scale integration system (VLSI), Clock system is a major source of all the power consumption. The clock system consists of a clock distribution network and flip-flops. Flip-flops are critical timing elements in sequential circuits which have a large impact on circuit speed and power consumption. Its performance is an important element to determine the performance of the whole synchronization circuit. Normally SETFF uses any one of the clock edges, another clock edges are idle position, but DETFF fetches data on both rising and falling edges of the clock cycle. Because both the clock edges in a dual edge triggered flip-flop (DETFF) are [1] active, the data throughput will be doubled while operating at half of the clock frequency of the SETFF. Nowadays, many low power DETFF structures have been proposed. Power efficient dual edge triggered sense amplifier flip-flop (DETFF) is classified into two main categories: master-slave DETFF and pulse triggered DETFF. The master-slave DETFF's are constructed by the parallel arrangement of positive and negative clock edge flip-flops. Pulse triggered DETFF has only one stage and are reduced complexity of the logic circuits. Here, we give brief knowledge of existing flip-flop architectures and performance of the new sense amplifier flip-flop circuits (hereinafter, referred to as a SAFF circuit).

II. CONDITIONAL PRECHARGE TECHNIQUE

Even though the present data output is the same as the previous data output, the internal node transition is occurring when the clock signal is applied to the synchronous logic circuit. This type of internal node transition is known as redundant event. Due to this redundant event, system performance is degraded and also it consumes more power. To reduce this redundant event, many popular techniques as well as their flip-flops have been proposed recently, such as conditional precharge flip-flop (CPFF), conditional capture flip-flop (CCFF) and conditional discharge flip-flop (CDFF). The Conditional precharge technique is one of the well-accepted techniques to reduce the power consumption when the system is idle. Conditional circuit is a heart of the conditional precharge technique [2]. It is used to disable the precharging paths of the internal transistors when the redundant event occurs.

III. CCFF VS CDFF

Conditional capture flip-flop (CCFF) and Conditional discharge flip-flop (CDFF) has two stages: one is a dynamic stage and another one is a static stage [3]. In the dynamic stage, discharge path will be controlled to reduce (or) eliminate the unwanted switching activity. The one big difference between CCFF and CDFF is the former flip-flop has a conditional circuit in the clock path (complementary) but the later flip-flop has an extra pull-down NMOS transistor. Due to this transistor, CDFFs faces somewhat complexity with high latency problem [6].

IV. CLOCK GATING TECHNIQUE

The clock gating technique is very popular technique which is used to disable or enable the global clock (CLK) depending upon the input changes. When D still stays the same value [5], the flip-flop enters into clock gating mode, the global clock (CLK) is enabled to control the internal clock (C). However, if D moves into another value, the global clock will be disabled and the internal clock pulse is applied into the flip-flop. Mainly AND gate is preferred to clock gating cell. The one input is global clock and the other input is the clock gating signal (CG). The output is used to control the internal clock pulse. The general block diagram of clock gating technique is provided in Figure.1.

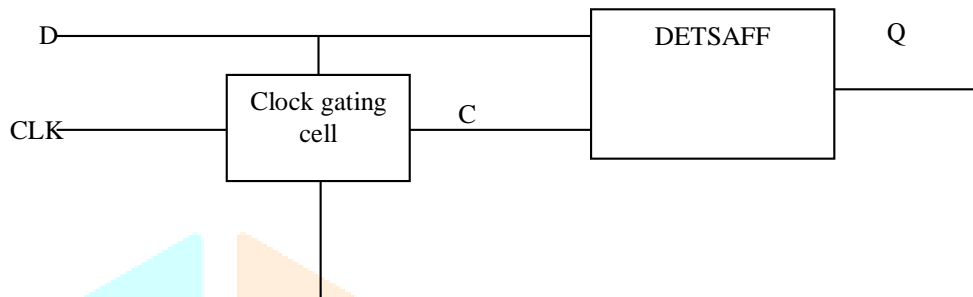


Figure 1: General block diagram of clock gating technique

V. REVIEW OF DETSAFF ARCHITECTURE

The timing elements (flip-flops and latches) are a basic element in the integrated circuit (IC). As a timing element in the IC, flip-flops are mostly used as storage elements which consume more power. The dual-edge triggering concept is one of the popular methods to reduce the power consumption. Because of both the clock edges in a dual edge triggered flip-flop (DETFF) are not idle, so data throughput will be high when compared with conventional single edge triggered flip-flop. Two main categories [1] of DETFF are (1) Latch-Mux and (2) pulse triggered flip-flops. The latch-mux are made up of two stages, one master and one slave. These two stages are arranged in the form of parallel, where one of them is transparent on any one levels of the clock and another stage one is again transparent on opposite levels of the clock. The second type, pulse triggered flip-flops again subcategorized into two: (1) Implicit and (2) Explicit. Both of the types have pulse generator which generates pulse.

The pulse generator generates pulse inside the flip-flop, means the type is implicit-pulse triggered flip-flop (IP-FF) whereas pulse is generated outside the system, means the type is explicit pulse triggered flip-flop (EP-FF). Even though EP-FF power consumption is more than IP-FF, EP-FF is widely used to clock sharing which distributes the power overhead of the pulse generator. The dual edge triggering concept is more difficult to embed in IP-FF whereas EP-FF is well-suited for dual-edge triggering technique. Various DETFF have been proposed to reduce the power consumption in low power application specific integrated circuit (ASIC) designs.

5.1 Static Output-Controlled Discharge Flip-Flop

The schematic diagram of static output-controlled discharge flip-flop (SCDFF) is provided [4] in Fig.2. The overall structure of SCDFF consists of dual pulse generator circuit and static latch structure. Here, the clock pulse is generated externally. This flip-flop is so called as explicit pulsed flip-flop (EP-FF). The static latch structure made up of two static stages. The external dual pulse is inserted into transistors m2 (first stage) and the m6 (second stage).

During the sampling period, the transistor m2 and m6 are turned on. In the first stage, the input D is inserted to drive the transistor m1 and m3. When D=1 and Q=0 (assumption), node X will be discharged through the transistor m2, m3 and m4. Due to this situation, automatically the output Q will move to high state by pull-up transistor m5 in the second stage. Node X still low state as long as D is high. The D input is used to drive the transistor m1 and m3 (in the first stage), m3 is going to be switched off position.

Finally the feedback path is opened and the node X will be recharged at some voltage. Now the inverted input D is applied into the pull down transistor m7 in the second stage, therefore the output Q will be discharged through the path m6 and m7. The unwanted discharging at node X will be controlled by one extra transistor, m4 which is driven by the output complementary controlled signal. The SCDFF is mainly used for low power VLSI design to reduce the unwanted switching activity.

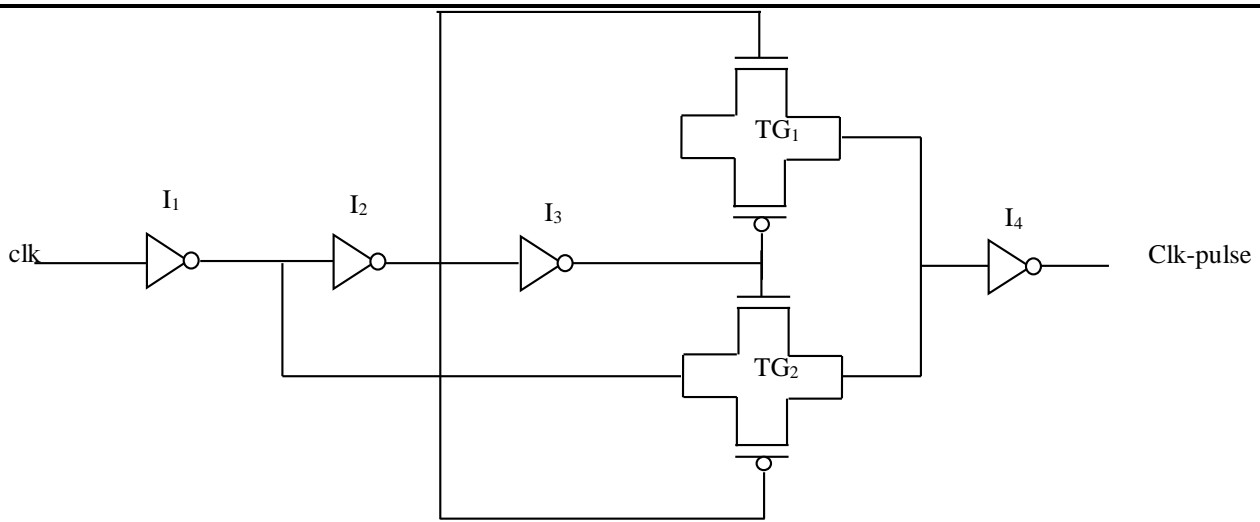


Figure 2 (a): Dual pulse generator

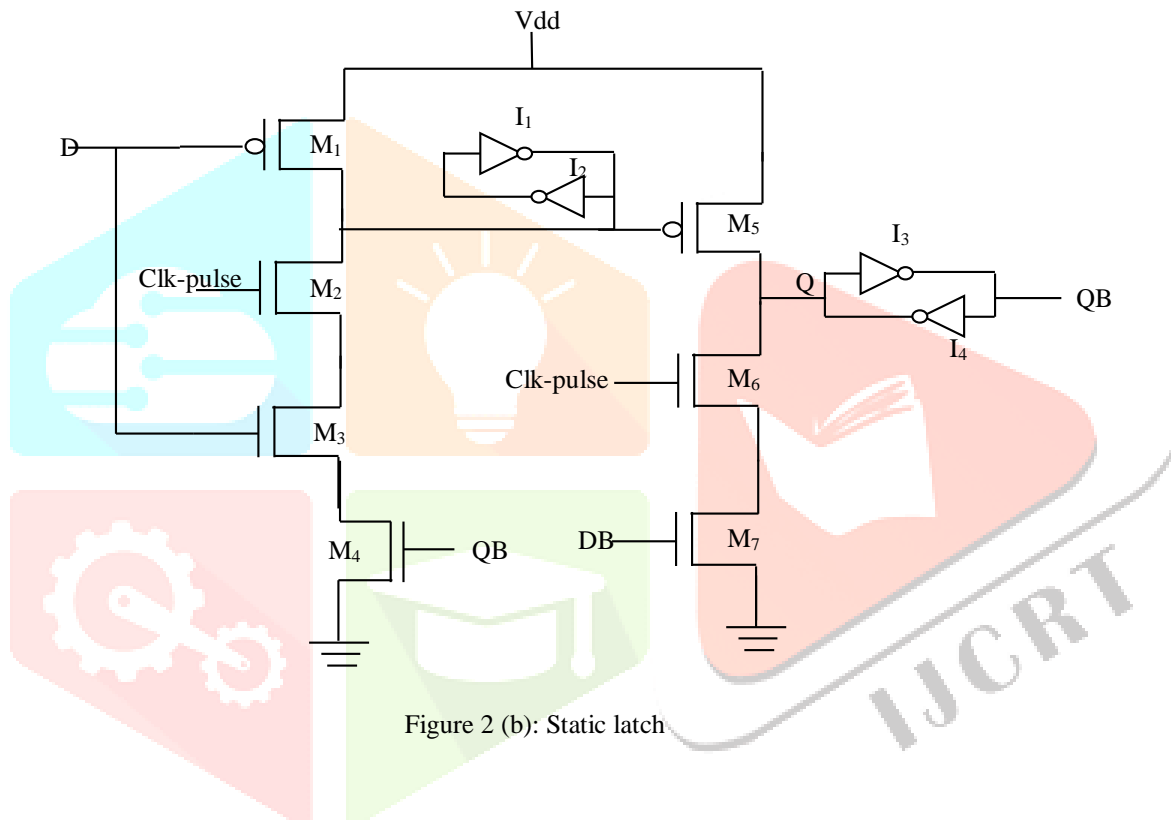


Figure 2 (b): Static latch

5.2 Dual-Edge Triggered Static – Pulsed Flip-Flop

Fig.3 shows a schematic diagram of dual-edge triggered static [7] pulsed flip-flop (DETSPPF). The DETSPFF consists of two parts, namely (1). Explicit pulse generation circuit (2).Static latch. The explicit pulse generator is made up of four inverters and two NMOS pass transistor. It is used to generate delayed and inverted signal, namely CLK2 and CLK3. The delayed clock signal CLK2 is inserted into the drain of the NMOS pass transistor N5 and at the same time, the gate of the N5 can be controlled by clock signal, CLK. The inverted clock signal CLK3 was applied into the drain of the other NMOS pass transistor N6 and at the time, the gate of the N6 can be controlled by inverted clock signal CLK1. These two signals generate a narrow sampling window at both the rising and falling edges of the clock as shown in figure.

During the sampling period, the pass transistor N1 and N2 are turned on to sample the data inputs. The data inputs D and DB are directly inserted to the static nodes SB and S respectively through the transistor N1 and N2. This helps for minimum delay. The floating of static nodes SB and S will be controlled by weak NMOS transistor N3 and N4. When the data input D is high, automatically static node SB will be discharged through the weak NMOS transistor N4. At the instance, the inverted data input will be low the static node S gets charged through the NMOS transistor P2 upto Vdd. During another sampling period, D may be low, the static node SB will be changed upto V- \ddot{d} d through the PMOS transistor P1. AT the same time the static node SB will be discharged through weak NMOS transistor N4. The DETSPFF is main used to eliminate unwanted transitions. Even though the next data input will be same as that of previous one, again transition occurs inside the circuit. So unwanted transition occurs.

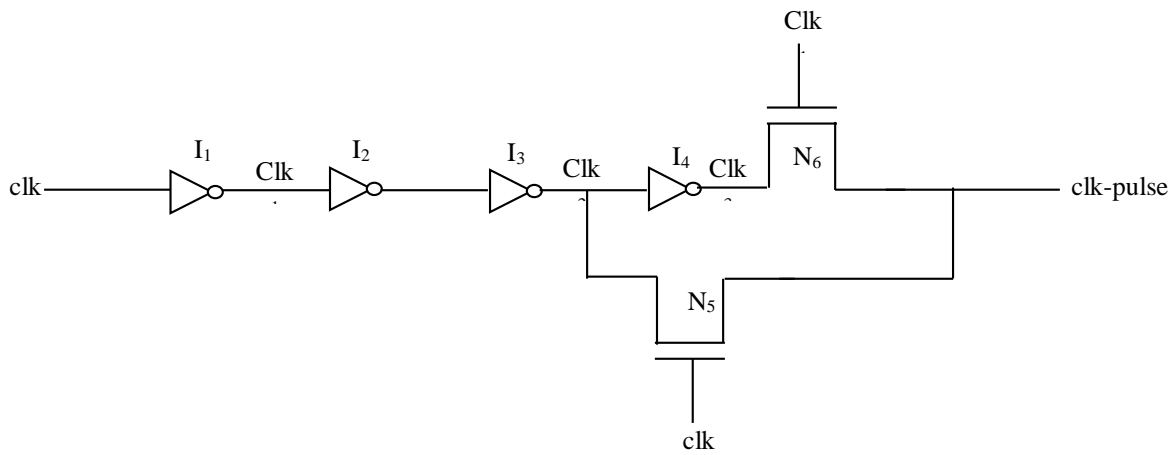


Figure 3 (a): Dual pulse generator

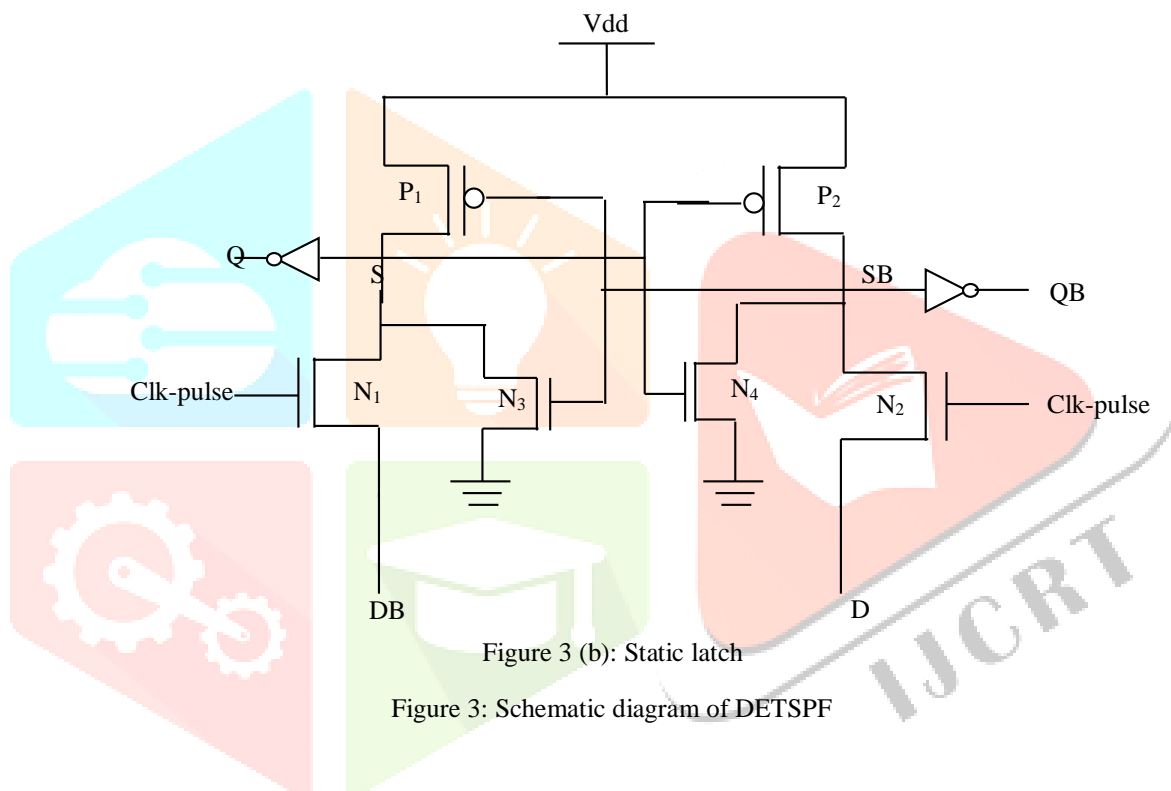


Figure 3 (b): Static latch

Figure 3: Schematic diagram of DETSPF

5.3 Adaptive Clocking Dual Edge Triggered Sense Amplifier Flip-Flop

The schematic diagram of adaptive clocking dual edge triggered sense amplifier flip-flop (ACSAFF) is shown in Fig.4. The main component of ACSAFF is (1) clock inverter chain (2). front end circuit (3). Latch. The clock inverter chain is used to generate delayed clock signals. The node NC is derived from the front end circuit which disables the clock inverter chain [8] when the data switching activity is low. Both CLK and CLK3 are high for a small time period on the CLK rising edge and similarly both CLK1 and CLK4 both are high for a small time period on one CLK falling edge. These delayed signals are applied into the front end circuit. When the data input D is different from the output Q, the node NC is charged through the transistor N5 and N6 (or) N7 and N8. The signal derived from node NC will turn on the transistor NIC1 and NIC2 of the clock inverter chain to create inverted and delayed signals CLK3 and CLK4 so that narrow sampling window is created on the rising (or) falling edges of the clock. During the narrow sampling period, the node SB (or) RB create the discharging path to the next component of ACSAFF, (i.e.) latch. When the output changes, the node NC will be pulled down through the transistor N2 and N1 (or) N3 and N4, at the same time node NC disables the clock inverter chain. If the input D is same as the output, Q, nodes SB and RB stay high and latch maintain its previous output. ACSAFF saves more power at low switching activity, but it requires more transistor to implement the adaptive clocking.

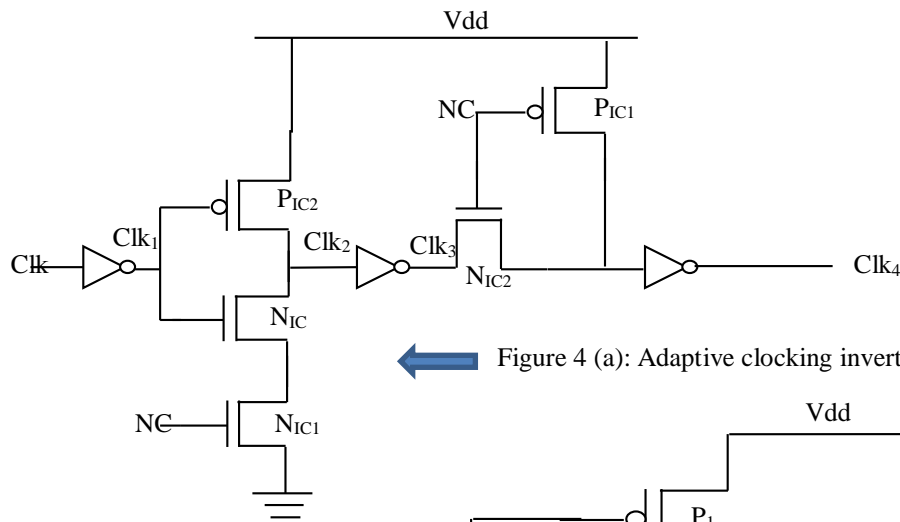


Figure 4 (a): Adaptive clocking inverter chain

Figure 4 (b): Front end sensing stage

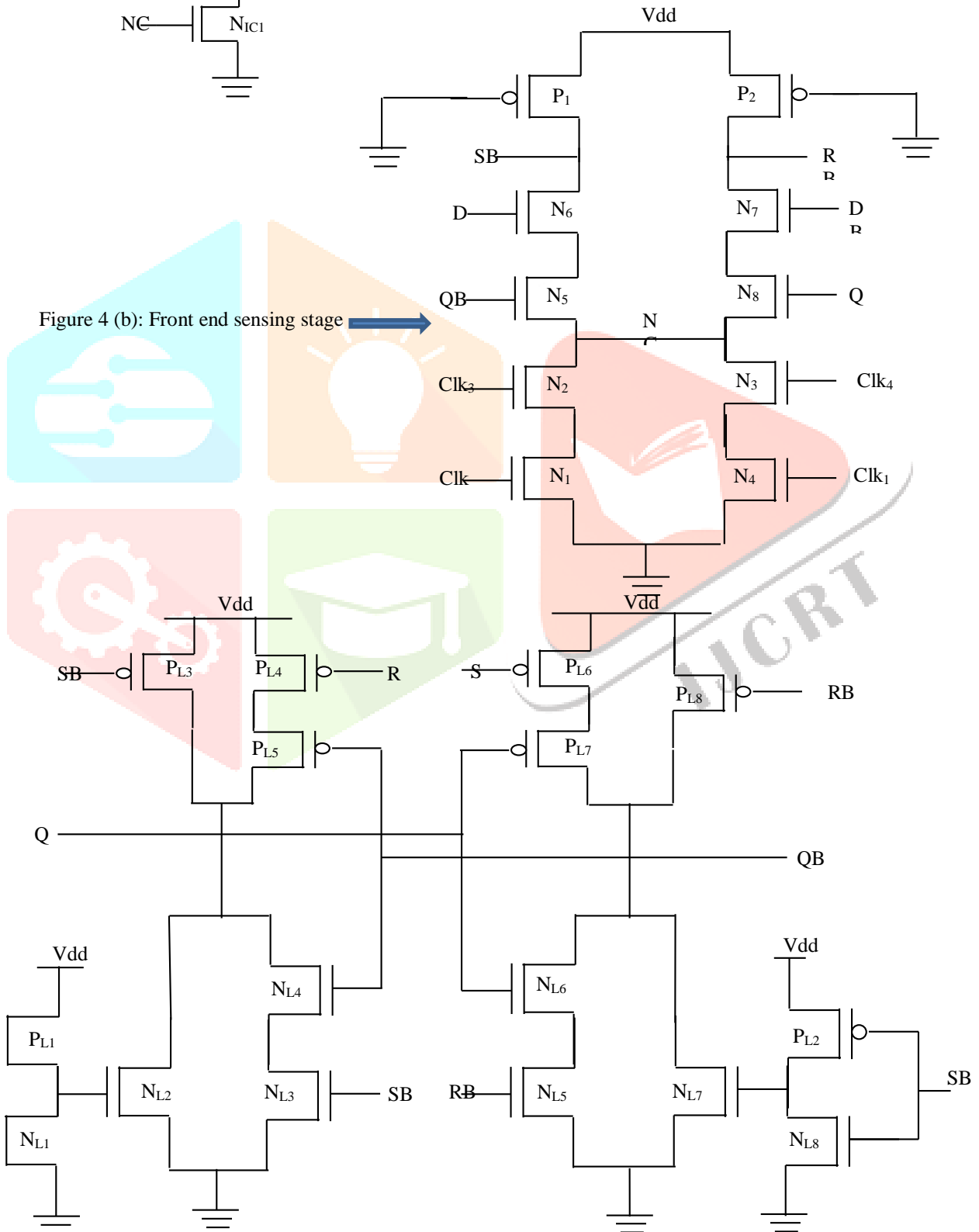


Figure 4: Schematic diagram of ACSAFF

5.4 Dual-Edge Triggered Sense Amplifier Flip-Flop

The schematic diagram [1] of dual-edge triggered sense amplifier flip-flop (DETSAFF) is given in Fig.5. There are three major parts for the DETSAFF: (1) dual pulse generator to generate the pulse signal at the rising and falling clock edges (2) sensing circuit based on the sense amplifier flip-flop (SAFF) (3) Latch. The DETSAFF is an explicit type because the pulse signal produces externally and then it is applied to the multiple flip-flop circuit. In the sensing circuit, when input D is low, the PMOS transistor SP₁ will turn on and the node SB is precharged upto V_{dd}(high). Similarly, when input D is high, the PMOS transistor SP₂ will turn on and the node RB is precharged upto V_{dd}(high). Here SP₁ and SP₂ are input controlled PMOS transition in the precharge path.

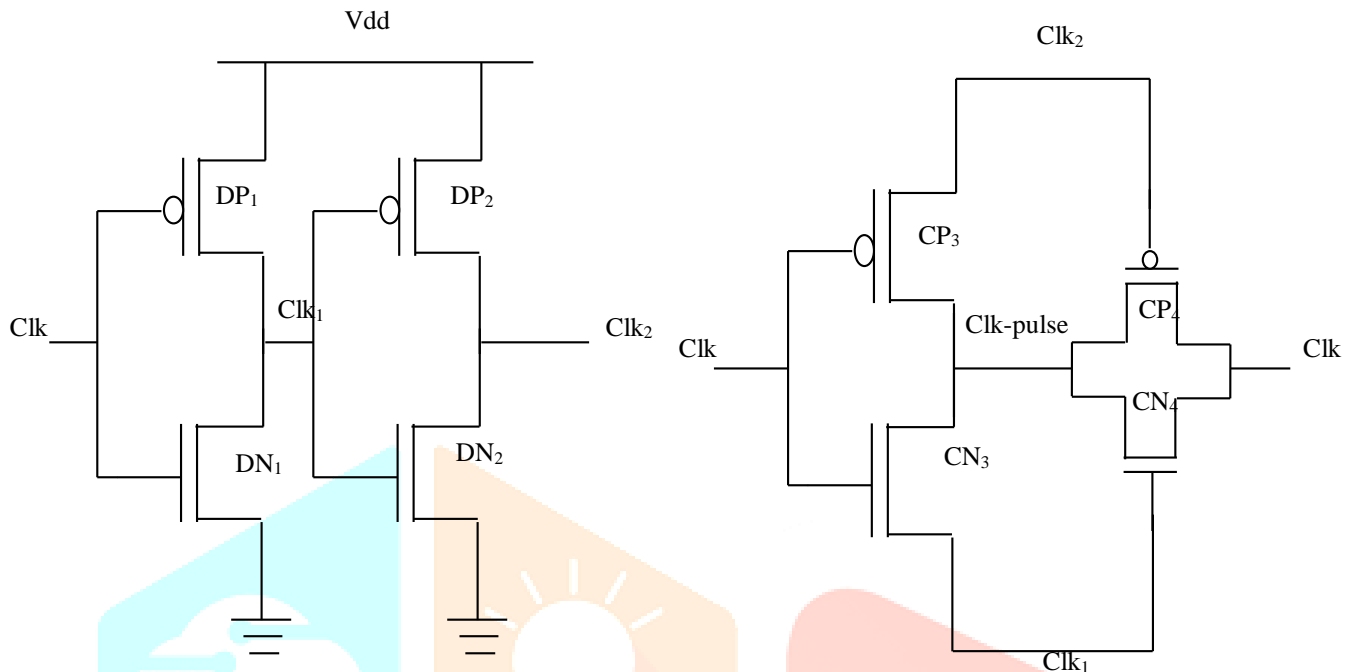


Figure 5 (a): Dual pulse generator

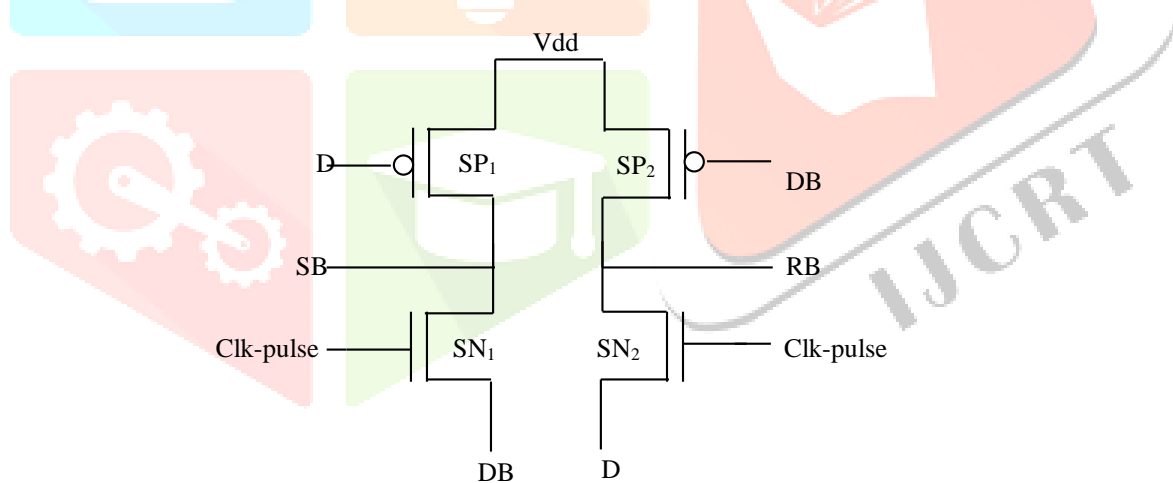


Figure 5 (b): Sensing stage

During the transparent period, if D is high, node SB is discharged through SN₁ to the low value of DB and node RB is precharged upto V_{dd}. Similarly, during the other transparent period, if D is low node, SB is precharged through SP₁ up to V_{dd} and node RB is discharged to the low state D. The signal derived from SB and RB are directly fed into the pull-up transistors LP₁ and LP₂ respectively. The data input (D) and inverted input (DB) are directly fed to the clk-pulse controlled NMOS pass transistor LN₁ and LN₂ respectively. The output node Q and QB will be charged by pull-up transistors and pass transistors. When the flip-flop is not a transparent, the output state still maintains the previous value with the help of inner transistors LP₃, LP₄, LN₃ and LN₄. Even though the data switching activity is low, the dual pulse generator produces clock-pulse which creates unnecessary transitions. Due to this, the DETSAFF consumes more power at low switching activities.

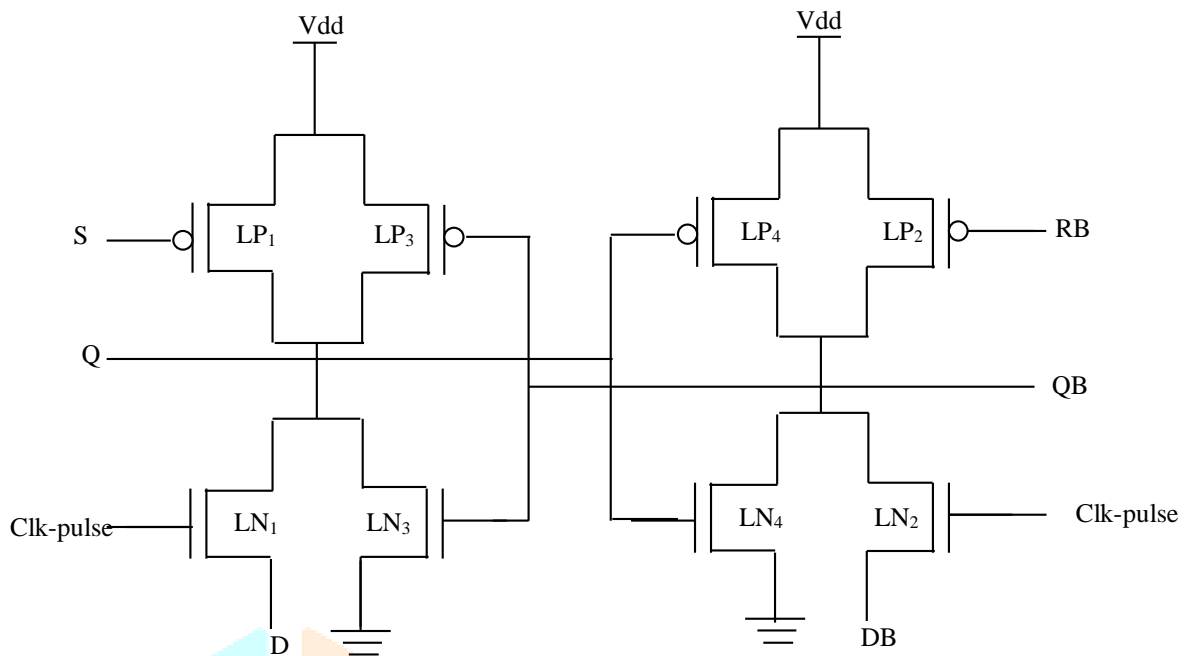
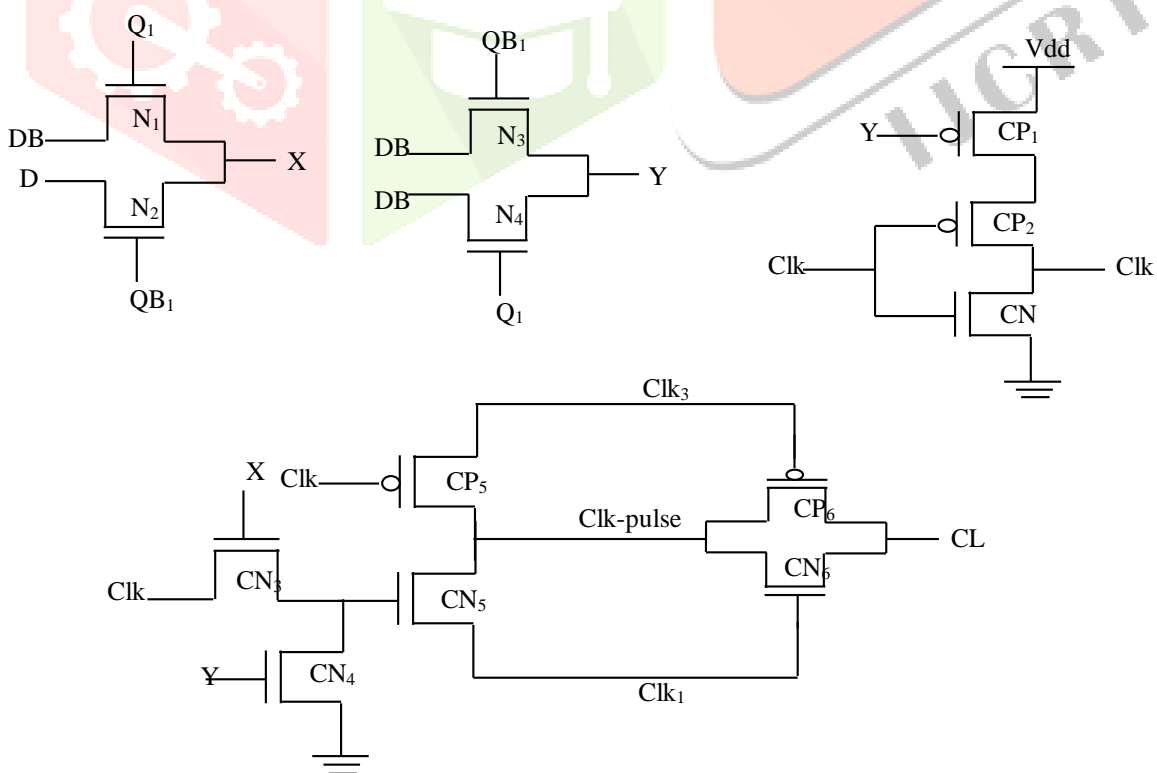


Fig.5 (c): Latch

Figure 5: Schematic diagram of DETSAFF

5.5 Clock Gated Sense Amplifier Flip-Flop

The clock gated pulse generator [1] is given in Fig.6. Here, the comparator is a major source to produce the two signals namely X and Y. The comparator input is differential inputs D and DB. The buffered outputs Q1 and QB1 act as control signals. These two signals (X & Y) are inserted into the gate of CN3 and CN4 respectively. If D is different from the output Q, the signal at node X will be high and the signal at node Y will be low. The NMOS transistor CN3 will be turned on and the clock signal passes through CN3 to CL. CL is called as gated clock. AT the same time, the inverted clock signal CLK1 is generated and which is inserted into the pass transistor CN6 and similarly the delay gated clock CLK3 is inserted into the pass transistor CP6. These two signals (CLK1 and CLK3) acts as a control signal for transmission gate (TG).



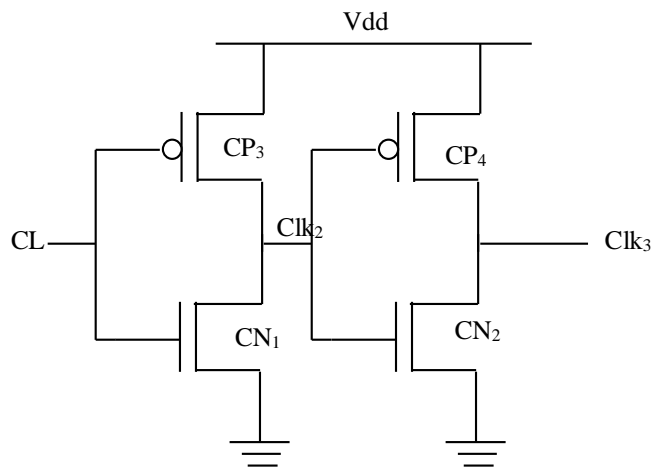


Figure 6: clock-gated pulse generator

The TG input signal is gated clock (CL). The pulse is generated at the rising and falling edge of the clock. When the input D still the same in next n cycles, the X will be pulled down to low and Y to high. So, the transistor CN3 is switched off and the clock is not passed to CL. The CL will be pulled down through the CN4 to the ground. Finally the clock signal is blocked and flip-flop stays opaque. The schematic diagram of clock gated sense amplifier flip-flop (CG-SAFF) is presented in Fig.7. The sensing stage is the same as DET-SAFF. In the latching stage, the big difference between DET-SAFF and CG-SAFF is the former need pulse signal, but the later does not require any pulse signal. The buffered differential outputs, Q1 and QB1 are generated and which are used to produce X and Y instead of using Q and QB.

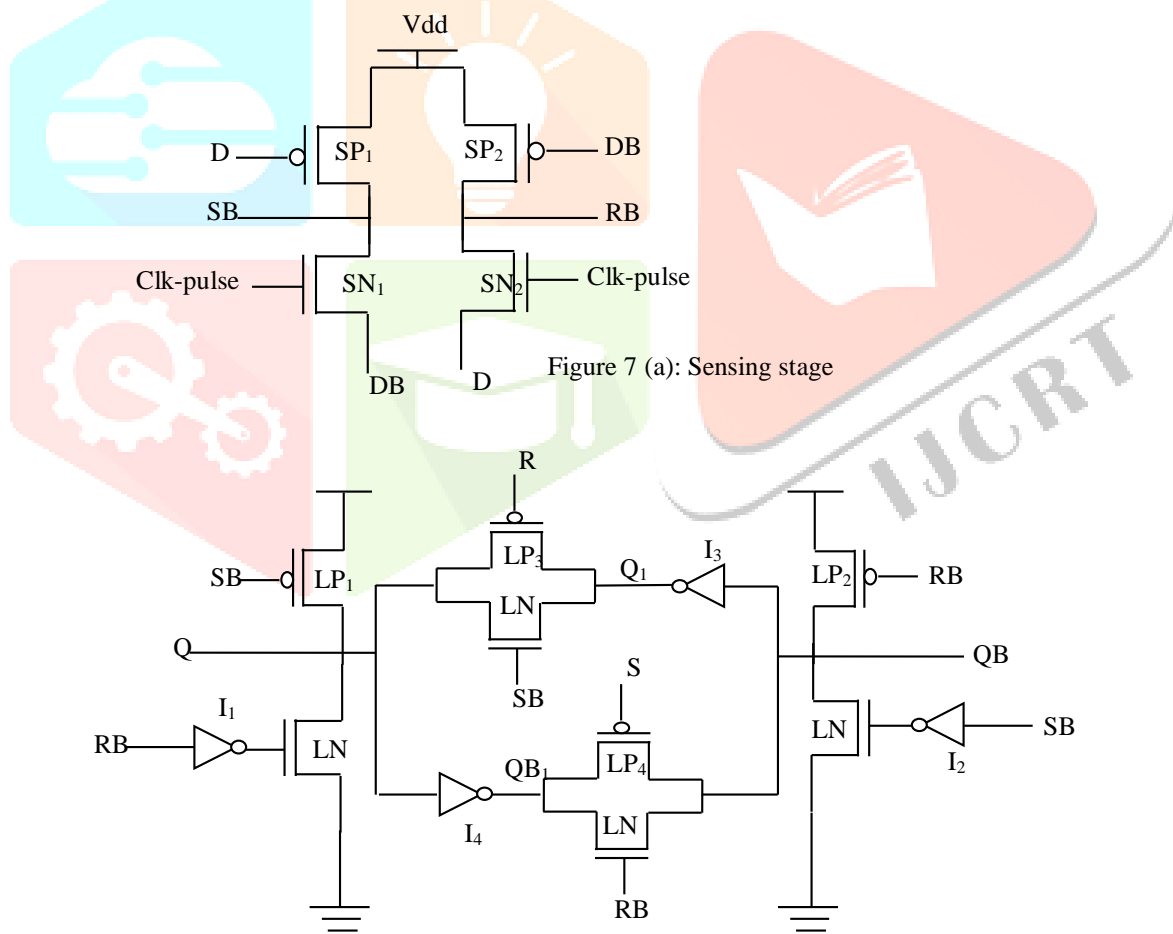


Figure 7 (a): Sensing stage

Figure 7 (b): Latching stage

Figure 7: Schematic diagram of CG-SAFF

VI. PROPOSED WORK

When the data input D stays previous value, CG-SAFF enters clock gating mode (i.e., the internal clock pulse is not applied to the flip-flop). The clock gating process is mainly used to avoid redundant internal transitions. Now D change from the previous value, flip-flop enters into non-gating mode. Due to the global clock out of phase with an internal clock pulse, the data error may be occurring because of asynchronous data sampling. Future work is to filter out the asynchronous data sampling.

VII. CONCLUSION

This paper gives a brief explanation on clock gating, dual-edge triggering concept, dual-edge trigger sense amplifier flip-flop and its schematic diagram. The main purpose of this paper is to study about the different DETSAFF and clock gating SAFF is mainly used to reduce unnecessary transitions.

REFERENCES

- [1] MyintWaiPhyu, Kangkang Fu, Wang Ling Goh and Kiat-seng Yeo, "Power-Efficient Explicit-Pulsed Dual-Edge Triggered sense-amplifier Flip-flops," IEEE Trans. Very Large Scale Integr.(VLSI) syst. Vol.19,no.1,January 2011.
- [2] N.Medovic,M.Aleksic,and V.G.Oklobdzija,"Conditional precharge techniques for power-efficient dual-edge clocking," in Proc.2002 Int.Symp. Low power Electronics Design (ISPLED 2002),2002,pp. 56-59.
- [3] B.S.Kong, S.S.Kim, and Y.H.Jun,"Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-state circuits, Vol.36, no.8 , pp. 1263-1271 , Aug.2001.
- [4] M.W.Phyu,W.L.Goh, and K.S.Yeo," A low-power static dual edge triggered flip-flop using an output-controlled discharge configuration," in Proc. IEEE Int.Symp circuits Systems (ISCAS 2005), may 2005,vol.3,pp.2429-2432.
- [5] X.Wang and W.H.Robinson," Asynchronous data sampling within clock-gated double edge triggered flip-flops," IEEE Trans. On circuits and systems-1: Regular papers, vol.60, No.9, September 2013, pp.2401-2411.
- [6] P.Zhao, T.K.Darwish, and M.A.Bayonmi," High performance and low power conditional discharge flip-flop," IEEE Trans. Very Large scale Integr. (VLSI) syst. Vol.12, no.5,pp.477-484, may 2004.
- [7] G.Aliakbar and M.Hamid," Dual edge triggered static pulsed flip-flops," in Proc. 18th Int. conf. VLSI Design 2005,Jan.2005,pp.846-849.
- [8] Y.T.Liu, L.Y.Chiou, and S.J.Chang," Energy-efficient adaptive clocking dual edge sense amplifier flip-flop," in Proc. IEEE Int.Symp.circuits systems (ISCAS 2006), may 2006,pp.4329-4332.
- [9] C-C.Yu," Design of low power double edge triggered flip-flop circuit," in Proc. 2nd IEEE conf. Industrial Electronics Applications (ICIEA 2007), may 2007,pp.2054-2057.
- [10] P.Zhaoetal.,"Low-power clock branch sharing double edge triggered flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) syst., vol.15, no.3, pp.338-345,Mar.2007.
- [11] G.Aliakbar and M.Hamid," Dual-edge triggered static pulsed flip-flops," in Proc. 18th Int. Conf. VLSI Design 2005, Jan.2005, pp.846-849.