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IMPROVED HIGH-SPEED LDPC ENCODER ARCHITECTURE FOR IEEE 802.3an STANDARD

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Abstract: With advancements in technology always there is need for development of portable and highly efficient communication systems and protocols. This paper describes the design of modified low density parity check encoder that can be employed in IEEE 802.3an 10-Gigabit Ethernet base station standard with required encoding rate. This modified encoder design adopts both general and Richardson Ubranke (RU) methods to achieve low complexity and efficient encoding. The advantage of this modified encoder is compatibility with all the types of recently developed decoder designs. There is no swapping of column or row required as both general and RU methods are involved in encoding process and also back substitution method is adopted for inverse multiplication process. ASIC implementation of the high-speed proposed encoder uses wave pipelining technique to reduce the critical path delay and uses the temporary shift registers to reduce memory storage. Implementation of high-speed encoder is reported with delay of **3.25ns** and power dissipation of 489.75mW with gpdk 180nm technology using wave pipelining technique.

Index Terms - Application Specific ICs, Codeword, IEEE802.3an 10Gb Ethernet Base Station, Parity check matrix, Low Density Parity Check Codes, Very Large Scale Integration Architectures.

I. INTRODUCTION

Low density parity check codes are the type of outperforming forward error correction block codes used in many of the advanced communication standards like DVBS2, IEEE 802.16e Wi-Max, 802.11an, 802.3an 10GB Ethernet base stations, WiFi etc. These codes are developed by Gallager in 1962 [1].Codes better perform compared to Turbo codes in several ways 1) Due to sparse parity check matrix decoding complexity can be reduced to show asymptotically better [2][3] and applicable for wide range of applications trading of between performance and complexity. 2) Message passing decoding is used, where all check node computation and all variable node computation can be done simultaneously. These codes supports fully parallel decoding architectures hence decoding speed can be better. Fully parallel and partial parallel decoding architectures are developed [4], where partial parallel decoding is to be proven better for hardware implementation [5-7]. Superior performance of LDPC codes is demonstrated for wide class channels which will very close to Shannon's limit [8].

The BER and decoding convergence performance of LDPC decoders has been considerably improved in [10]. The performance of quasi-cyclic(QC) LDPC decoders are reported for achieving high throughput, better convergence [11].To support various high data rate up to 1Gbps with standards such as IEEE 802.11an and 802.16e QC LDPC codes are used as error correction codes. To achieve high encoding throughput the number of clock cycles of process needs to be reduced. The QC LDPC design [9] support high data rate with minimum number of clock cycles. VLSI `implementation of such high throughput, memory efficient decoders [12, 13] has been developed to cope with varying wireless communication standards. The demand still exist for the development of highly efficient, portable and low power LDPC encoder and decoder architecture as technology is advancing. Decoding complexity of LDPC codes can be reduced considering min- sum, sum-product and also modifications to these decoding algorithms have been reported by many authors. Correspondingly the development of VLSI architectures is also reported. Aim of this paper is the development of high speed VLSI architecture of LDPC encoder (2048,1723) for IEEE 802.3an standard. This standard defines the data transmission in physical layer of 10 Gbits Ethernet base station over shielded or unshielded twisted pair of cables of 100m distance. As the encoding complexity of LDPC codes is generally very high and it is almost proportional to quadratic times the block length (n^2), researchers [8] have reported that

encoding complexity can be reduced to linear time(n) by applying the Gaussian elimination and converting the parity check matrix into lower triangular form and preprocessing of some of the computations using software without altering the information block length(k).The main reason of implementing high speed encoder here is to achieve high speed data transmission and reception to cope with advancement in technologies.

In this paper contents are organized as, section 1 describes the introduction of LDPC codes and scope of these codes for different applications. Section 2 focuses on basics and different encoding techniques can be used in the design of LDPC encoder. Section 3,4 deals with proposed encoder design and details about the applying wave pipelining technique to develop high speed LDPC encoder. In section 5, the results of the LDPC encoder is discussed and the performance of the proposed encoder is compared with various encoder designs of different IEEE standards. The section 6 concludes the proposed encoder design with propagation delay of 3.25ns and also addresses the future research issues.

II. RELATED WORK

Low Density Parity Check codes are belonging to type of forward error correction linear block codes characterized by (n,k) or $(n,w_c\,,w_r)$, where n is length of codeword bits, k is length of message bits, w_c represents the degree of column (number of nonzero elements of each column) and w_r represents the degree of row (number of nonzero elements of each row) of the parity check matrix. Code rate r is defined as k/n. In regular PCM, $w_c\,,w_r$ degree of check nodes and degree of variable nodes is fixed. In irregular PCM the check node and variable node degree are not fixed, based on this LDPC codes are identified as regular and irregular LDPC codes. Binary LDPC codes are represented by sparse parity check matrix H (containing very less number of 1s than 0s in rows and columns). For systematic codeword generation the H matrix must satisfy the equation (1).

$$CH^T = 0\ (mod\ 2) \tag{1}$$

Where, 'C' is the generated codeword. LDPC codes are also represented diagrammatically using Tanner graph with example of fig1.

$$H = \begin{bmatrix} c_1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ c_2 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ c_3 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\ c_4 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ c_5 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ & v_1 & v_2 & v_3 & v_4 & v_5 & v_6 & v_7 & v_8 & v_9 & v_{10} \end{bmatrix} \tag{2}$$

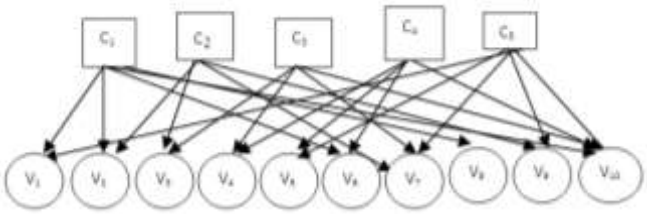


Fig.1 Tanner Graph of parity check matrix [10,5]

2.1 Basics of Encoder

Linear block codes are encoded normally using systematic generator matrix G multiplying with message bits as per equation (3)

$$C = S \times \mathrm{G} \tag{3}$$

Where ,'S' message bits which needs to be encoded. The systematic generator matrix G is in the form of equation (4), I_k is an identity matrix and P represents parity bits.

$$G = [I_k \ \ P] \tag{4}$$

LDPC codes are derived directly derived from sparse parity check matrix the encoding can be performed by converting the PCM (H) to generator matrix (G) then generating the codeword using equation (3). If the H matrix is not in systematic form then it has to be converted in to the systematic form as per equation (5)

$$H = [-P^T \ \ I_{n-k}\ ] \tag{5}$$

where, I_{n-k}defines identity matrix and P^T defines the transpose of the parity check matrix. Most of the researchers used general encoding method as multiplying message bits with generator matrix to generate codeword with encoding complexity proportional to (n^2) . To reduce encoding complexity Richardson and Urbanke (RU)[8], reformulated the PCM to lower triangular matrix and pre-computed the $P_1$and P_2 parity matrices then combined with message to form codeword (S,P_1,P_2) with almost linear encoding

complexity(n). Preprocessing of $P_1$and P_2 reduces encoding complexity but requires more memory space to store preprocessed data so this proposed encoder design combines both general method and RU method to achieve high speed and low encoding complexity.

2.2 Richardson Ubranke Method

Encoder complexity can be reduced by reorganizing the parity check matrix without changing the sparseness and properties of PCM. Richardson and Urbanke [8] converted the PCM to lower triangular form and divided the PCM matrix into A, B, C, D, T, E sub matrices maintained the sparseness of all the reformulated sub-matrices with small gap g as shown in fig.2.

$$H = \begin{bmatrix} A & B & T \\ C & D & E \end{bmatrix} \quad (6)$$

Where, T is lower triangular and all other sub matrices are sparse matrices.

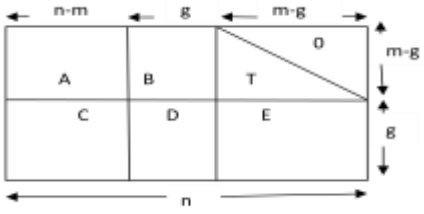


Fig.2. Lower triangular form of parity check matrix

Multiplying H matrix (6) with (7) to obtain new matrix H_t as

$$\begin{bmatrix} I_{m-g} & 0 \\ -ET^{-1} & I_g \end{bmatrix} \quad (7)$$

$$H_t = \begin{bmatrix} A & B & T \\ -ET^{-1}A + C & -ET^{-1}B + D & 0 \end{bmatrix} \quad (8)$$

Where, $\Phi = -ET^{-1}B + D$ should be nonsingular if not then swapping of the columns to generate nonsingular matrix. This swapping of columns makes the generation of non systematic encoder. Other way is to apply row swapping but it leads to degradation of performance of encoder with large value Φ. Using H_t parity check matrix, the parity bits $P_1$and $P_2$are derived, these are pre processed and kept ready for encoding without involving directly in the encoding computation. Consider 'S' is systematic message bits which need to be encoded to generate codeword $C^T = [S\ P_1\ P_2]$, by multiplying S^T with $H_t$results into

$$AS^T + BP_1^T + TP_2^T = 0 \quad (9)$$

$$(-ET^{-1}A + C)S^T + (-ET^{-1}B + D)P_1^T = 0 \quad (10)$$

$P_1$and $P_2$are calculated directly from (9)&(10)

$$P_1^T = -\Phi^{-1}((-ET^{-1}A + C)S^T \quad (11)$$

and $P_2^T = -T^{-1}(AS^T + B \quad (12)$

The computational complexity requirements of $P_1$and P_2 are summarized in the Table I. Some operations of calculation of parity matrices $P_1$and P_2can be performed in parallel shown in the flow diagram fig.3 to reduce the computational complexity.

Table I Calculation of parity matrices P_1 and P_2

Operation	Process Requirements	Computational Complexity
AS^T	(m-g)x(n-m) multiplication	O(n)
$T^{-1}(AS^T)$	(m-g)x(m-g) back substation	O(n)
$-E(T^{-1}(AS^T))$	(g)x(m-g) multiplication	O(n) P_1
CS^T	(n-m)x(g) multiplication	O(n)
$(-ET^{-1}A + C)S^T$	(n-m) back substitution	O(n)
$-\Phi^{-1}(-ET^{-1}A + C)S^T$	(g)x(g) dense matrix multiplication	$O(n^2)$
AS^T	(m-g)x(n-m) multiplication	O(n) P_2
BP_1^T	(m-g)x(g)	O(n)
$AS^T + BP_1^T$	(m-g) bit by bit addition	O(n)
$-T^{-1}(AS^T + BP_1^T)$	(m-g)x(m-g) back substitution	O(n)

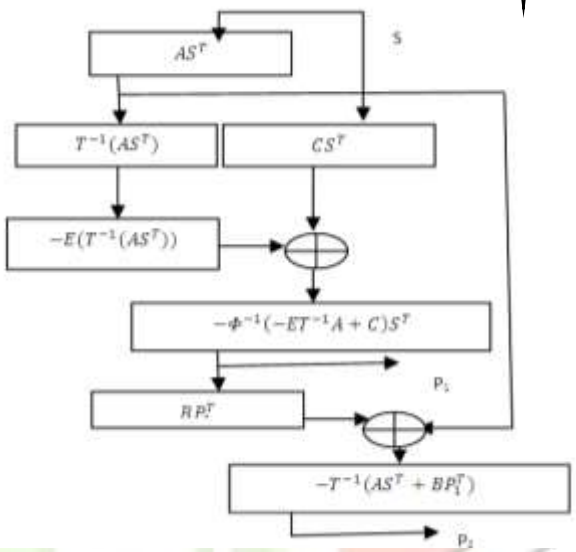


Fig3. Flow diagram of implementation of RU Encoder [10, 11]

III. ENCODER ARCHITECTURE

Encoder design using general method has drawback of more encoding complexity proportional to $O(n^2)$. Encoder design using RU method uses less encoding complexity almost linear to O(n) but large memory is required to store the preprocessed parity matrices P_1 and P_2 and also suffered from long critical path delay. To overcome these problems there is encoder design of (2048, 1723) IEEE 802.3 an Ethernet standard [14] proposed [15] which uses both general and RU methods. To calculate P_1 in RU method there is requirement of computation of Φ^{-1} provided Φ should be non singular, if not applying row and column swapping to convert it into nonsingular. This computation takes longer path and need more hardware so, G matrix multiplication general method sequential encoding is used for the computation of P_1 and storing in the GROM memory as shown in fig.4.Parity matrix P_2 can be calculated directly using $-T^{-1}(AS^T + BP_1^T)$ from RU method as per fig.4. This combined technique reduces critical path delay of RU method and also larger memory storage problem of general method.

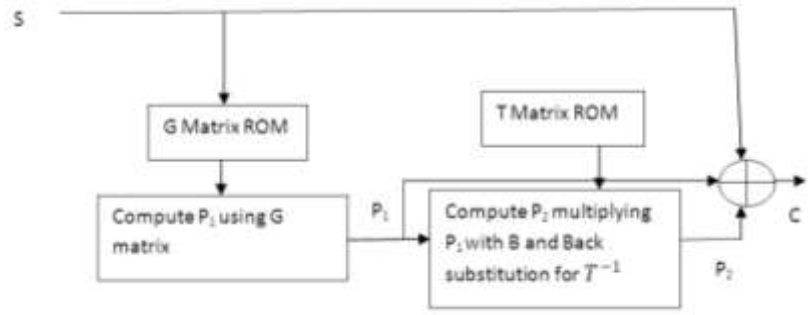


Fig.4. Block diagram of Hybrid Encoder [15]

In this hybrid encoder module, G matrix ROM stores the coefficients of G matrix and T matrix ROM stores coefficients of lower triangular T matrix. For computation of P_2, T^{-1} matrix multiplication is complex method, so to simplify process backward substitution is used. Consider the lower triangular T matrix with an example [15],

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ T_{2,1} & 1 & 0 & 0 \\ T_{3,1} & T_{3,2} & 1 & 0 \\ T_{4,1} & T_{4,2} & T_{4,3} & 1 \end{bmatrix} \mathrm{X} \begin{bmatrix} y_1 \\ y_2 \\ y_3 \\ y_4 \end{bmatrix} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} \quad (13)$$

$$y_1 = x_1 \quad (14)$$

$$y_2 = x_2 \oplus T_{2,1}\, y_1 \quad (15)$$

$$y_3 = x_3 \oplus T_{3,1}\, y_1 \oplus T_{3,2}\, y_2 \quad (16)$$

$$y_4 = x_4 \oplus T_{4,1}\, y_1 \oplus T_{4,2}\, y_2 \oplus T_{4,3}\, y_3 \quad (17)$$

Using this backward substitution technique P_2 can be computed, which in turn increases the critical path delay. With the hybrid encoder design calculation of P_1 and P_2 as

$$P_1^T = S \times G(k+1 : n-(m-g)) \quad (18)$$

$$P_2^T = -T^{-1}(AS^T + BP_1^T) \quad (19)$$

IV. PROPOSED ENCODER DESIGN

In (n, k) of (2048, 1723) LDPC encoder design[15], the efficient power reduction technique and memory storage issues are addressed very well to meet the requirements of IEEE 802.3an 10Gb Ethernet base station. Proposed high speed LDPC encoder is designed for same specifications with penalty of more number of logic cells and power utilization at the cost of obtaining high speed using wave pipelining technique.

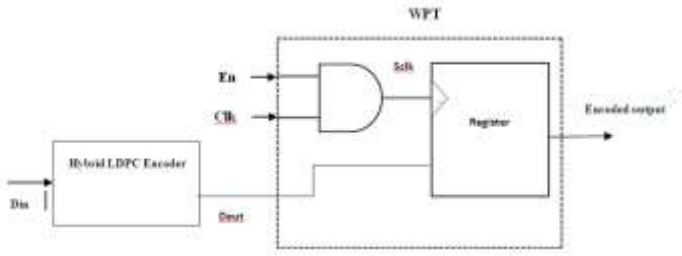


Fig.5. Proposed LDPC Encoder with Wave Pipelining Technique

The encoder design uses both the general and RU methods as in the hybrid model [15]. The encoded output is applied with wave pipelining technique to obtain high speed encoder suitable for high speed data transmission with required code rate.

4.1 Wave pipelining Technique

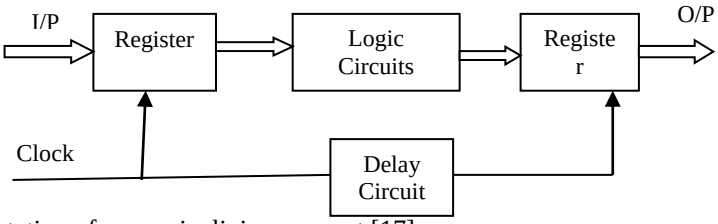
Wave pipelining is a present technique applied to obtain the high speed architecture for system without changing the system operation. This technique is introduced by Cotton [16]. According their observation that, data propagation delay through the circuit not only depend on longest critical path delay instead it depends on difference in the longest and shortest path delay along with overheads of system clock. This technique makes use of intermediate registers and exploits the delay of logic circuit to process the different data simultaneously as shown in fig.6 and 7. With wave pipelining technique the data propagation will be in the form of waves through logic circuits. Clock cycle time of wave pipelined system is calculated as in [16]

$$T_{clk} = (D_{Max} - D_{Min}) + T_{ov} \quad (20)$$

Where, D_{Max} and D_{Min} are maximum and minimum delay times and T_{ov} is system clock overheads in terms of setup and hold times of registers and skews. The clock region considered with wave pipelining is given by [17]

$$\frac{T_{Max}}{N} < T_{clk} < \frac{T_{Min}}{N-1} \quad (21)$$

Where, T_{Max} and T_{Min} maximum and minimum delay periods considered along with system clock overheads and skews and N is the required number of clock cycles to propagate data through the logic circuit block before the output is stored in storage register.



.Fig.6 Block diagram representation of wave pipelining concept [17]

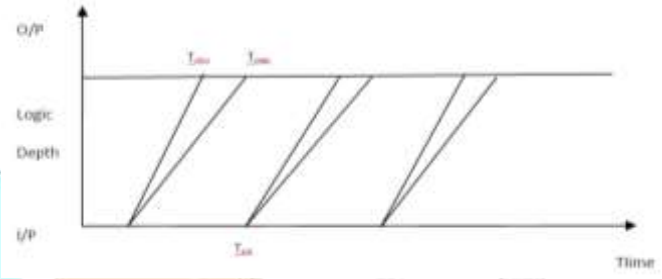


Fig. 7 Timing Diagram of waves [17]

In wave pipelined approach the better performance results are obtained if, T_{Max}=T_{Min}. This concept is applied for 6-GHz high speed pipelined 8 bit multiplier [17]. The design of high speed circuits called eSFQ(especially suitable for energy efficient pipelined circuits) with wave pipelined are developed [18] which are suitable for ultra low power high speed computing circuits. There is design of high speed low power ripple carry adder (RCA) using wave pipelining is proposed [19] without altering the configuration of the system just altering the routing paths of the data.

V. RESULTS AND DISCUSSION

The encoder (10,3,5) is designed with both the general method and RU method using Verilog code for ½ code rate. The results obtained with our flexible encoder architecture are as listed in the Table II [20].

Table II Propagation Delay of General and RU method [20]

ENCODER DESIGS	PROPAGATION DELAY(ns)
General Method	**3.259** (2.923 logic delay+0.336 route delay+89.7% logic used, 10.3% routing logic used)
RU Method	**2.003** (1.282 logic delay+0.721 route delay+64.0% logic used, 36.0% routing logic used)

The results obtained from Table II, shows that the encoding speed is increased for ½ code rate encoder with RU method with little trade off in the increase of hardware. With these results it is observed that, generator G matrix multiplication is used for encoding which slows down the speed of encoder. With RU method H matrix used which is converted into lower triangular matrix and calculation of Φ^{-1} and T^{-1}takes more resources which will increases critical path delay. In the proposed work, G matrix multiplication of general method is used for the computation of $P_1$and storing coefficients in the GROM memory and parity matrix P_2can be calculated directly using $-T^{-1}(AS^T + BP_1^T)$ from RU method as discussed in Fig.4&Fig.5. The backward substitution technique is applied for simplifying multiplications and inverse operations. The speed of the encoder can be further enhanced by applying wave pipelining techniques as discussed in section IV. The functional simulation results of encoder are as shown in Fig.8 and Fig.9.

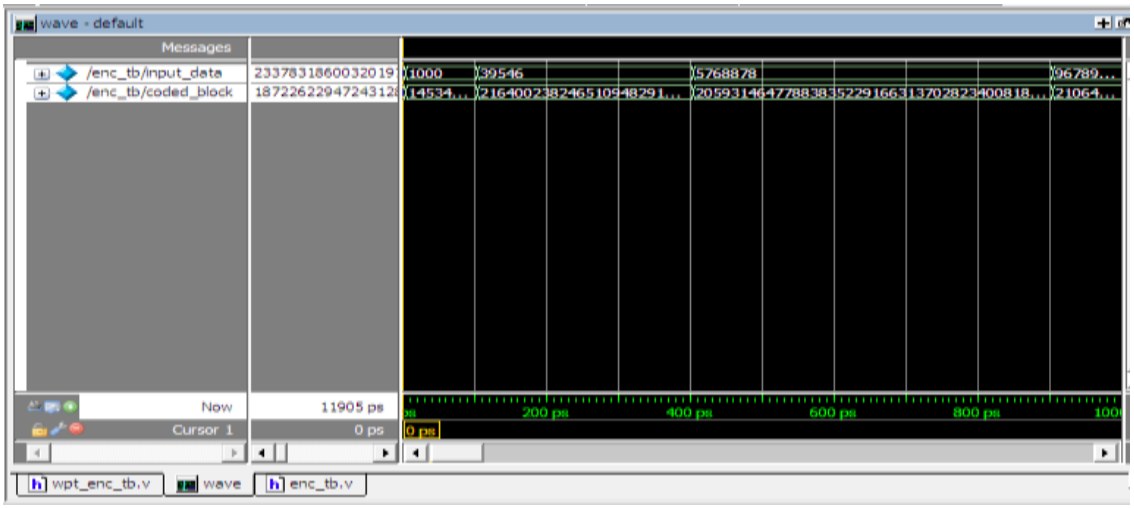


Fig.8. Simulation results of IEEE 802.3 an Encoder

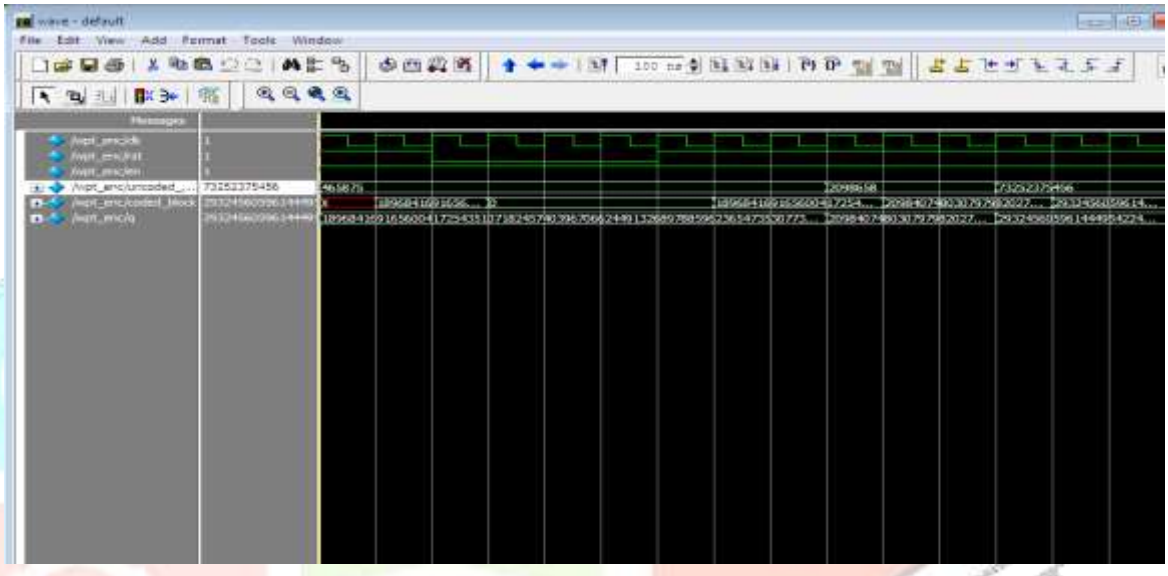


Fig.9. Simulation results of IEEE 802.3 an Encoder with wave pipelining

Table III ASIC implementation results of (2048, 1023) LDPC Encoder

Proposed Encoder Design	Area(cells)	Dynamic Power(nW)	Propagation Delay(ns)
With wave pipelining	1917655	489.75	**3.25**
Without wave pipelining	1699199	479.40	9.77

As there is always tradeoff between area, power and speed, with pipelining techniques the speed of encoding is increased thrice than without wave pipelined encoder at the cost of approximately use of 300000 more than standard cells and 200mW more power dissipation. The temporary registers are used for storing computed G and T matrices coefficients instead of using ROM memory directly. This resulted into avoiding the memory overflow situations. Implementing the proposed encoder with Vertex5 FPGA board also faces same memory overflow problem due to limited memory resources, hence attempts are made to implement the same encoder with ASIC implementation and obtained results are listed in Table III.

Table IV Implementation results of various LDPC Encoder designs of different IEEE standards

Work	Application IEEE Standards	Code Size	Code Rate	Technology	Area	Throughput
[15]	802.3an	(2048,1723)	---	Xilinx Vertex4 FPGA	11056 XOR +1620 AND Gates	----
[21]	802.16e Wimax	(2304,576)	1/2	Xilinx 3S1000	-----	50Mbps
[22]	DVB-T2	(6048, 5046)	5/6	Altera Stratix II C2 device	About 32k logic gates	28Gbps
[23]	802.16e Wimax	(2304,576)	1/2	Altera Stratix C5 device	5613 logic elements	4.984Gbps
[24]	802.16e Wimax	(2304,576)	½,2/3,3/4,5/6	Altera Stratix C2 device	--------	400Mbps
[25]	DVB-S2	Code length of 360	---------	Xilinx Vertex 5	--------	10Gbps
[26]	CMMB	Code length of 9219	1/2	Altera Stratix II C2 device	--------	34-59 Mbps
[27]	802.11n	Code length of 648	1/2	Xilinx Vertex 5	1164 Flip flops	12.12Gbps
Proposed	802.3an	(2048,1723)	5/6	ASIC 180nm	1917655 standard cells	13.25Gbps

The performance of LDPC encoder designs of different IEEE standards as discussed in literature and Table IV are not directly comparable as they have designed for different code rates, different block lengths and with either parallel or partial parallel architectures based on applications. The architecture design of [15] is uses RS based hybrid encoder with both general and RU techniques using back substitution techniques to implement the inverse equations. The reduced memory storage and critical path delay issues are addressed. With [21], Quasi cyclic encoder of IEEE 802.16e WiMax with block length of 2304 is developed considering recursive bidirectional parallel arithmetic methods to reduce the encoding complexity with throughput rate of 50Mbps.Bit wise matrix multiplication techniques are applied to design encoder with block length of 2304 with block size 576, throughput around 4098Gbps is achieved for IEEE 802.16e WiMax standard [23]. Multiple code rate encoder is designed for the same standard encoder resulting with 400Mbps[24]. The efficient encoder architecture [25] with throughput rate of 10Gbps is designed for DVB-S2(Digital Video Broadcasting)TV standard of block length of 360 bits. With [26], encoder architecture designed with FPGA implementation, code length of 648 bits achieving the throughput of 12.12Gbps for quasi cyclic codes of IEEE 802.11n.The speed of 10Gbps Ethernet base station at physical layer encoder has increased, supporting encoding frequencies starting from 1MHz, with encoding latency of codeword production within 30ns utilizing 27K gates [28].

VI. CONCLUSION

The channel coding is a vital technique used in cellular communication for the forward error correction codes for correction of noise present in the channels. For 5G communication, the LDPC codes are preferred over the Turbo codes, due to the development of energy efficient and highly flexible decoder architectures. LDPC decoders can be used up to 20Gbps downlink capability. In this work, attempts are made to design high-speed LDPC encoder (2048, 1723) for IEEE 802.3an standard with propagation delay of 3.25ns with 307.6MHz frequency. By using general and RU encoding methods along with wave pipelining technique, the speed of LDPC encoder could be achieved. From the study it is understood that the encoder designed may be the suitable candidate for 5G communication. The design of proposed encoder with ASIC implementation using gpdk 180nm technology, with wave pipelining uses more number of standard cells. Also more power is consumed than without the wave pipelining. These drawbacks of usage of large number of transistors and more power consumption can be addressed using appropriate VLSI techniques in future. Further improvements may be attempted to reduce the encoding complexity.

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