IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

COMPARATIVE ANALYSIS OF FAULT REDUCTION TECHNIQUES USING BIT SWAPPING LFSR AND CONVENTIONAL LFSR FOR TEST PATTERN GENERATION

M.Ramya[1], Dr.S.Sivanesskumar[2] , Mr.A.P.Prabakaran[3]

PG Student, Department of ECE, A.V.C college of Engineering[1]

Professor and Head, Department of ECE, A.V.C college of Engineering[2]

Assistant Professor, Department of ECE, A.V.C college of Engineering[3]

Mannampandal,Tamilnadu,India.

Abstract **:** The electronics industry has reached tremendous growth for the few decades, truly due to the rapid challenges for complex application in Very Large Scale Integration technologies. In many of the factories facing problems on testing the circuits withheld of low power consumption. The proposed system uses efficient Transition and Stuck-At Fault model for fault reduction for test pattern generation using LFSR and for low power consumption the system uses Bit Swapping LFSR to reduce the weighted switching activity and to reduce the number of transitions during normal and test mode operation. Necessary experimental results and Comparative analysis are presented to demonstrate the ability of the procedure to detect path delay faults with low power consumption using both conventional LFSR and BS-LFSR to detect the faults in benchmark circuits.

***Keywords*—VLSI, LFSR, BS-LFSR, Transition Fault Model, Stuck-At Model.**

I. INTRODUCTION

Testing of delay has become an important issue in the electronics industry for the post and pre-production tests due to the fast-growing and shrinking feature size of modern circuits. Traditionally a lot of delay fault model has been proposed. Hence the most successful fault model is the Path Delay Fault Model (PDFM). It detects small as well as large delay defects distributed along one path in the given circuit. Generally, combinational circuits may have faulty. In fast moves; test generation for all the circuits is not at all possible hence high-quality tests are needed especially for diagnosis.

The Bit Swapping Linear Feedback Shift Register (BSLFSR) is familiarized with upgrade the execution of the fundamental LFSR. The BS-LFSR configuration is basically focusing on decreasing of power dissipation by decreasing the overall switching activity in a conventional LFSR without compromising its capacity and performance. Power consumption is an essential criterion in VLSI Circuit designs which is required to improve the battery power dissipation.

The proposed technique uses a new TPG (Test Pattern Generator) to detect path delay faults using both Transition Fault Model and Stuck-At Fault Model using Low Power LFSR techniques, called the Bit Swapping Linear Feedback Shift Register (BS-LFSR) which is based on a simple bit swapping technique applied to the output of a LFSR. It reduces the average weighted switching activity during test operation by reducing the number of transitions. It combines with a scan-chain-ordering algorithm that reduces the switching activity in both the test cycle (capture power) and the Scanning cycles (scanning power).

II. RELATED WORK

Several techniques have been proposed to detect the fault and to reduce the power dissipation in test pattern generation. With a common Motto, they have established a fault model and Bit Swapping LFSR by using various techniques.

In [1], the author presents about low-transition linear feedback shift register (LFSR) that based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), combined with a LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduced the number of transitions that occurred at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. The BS-LFSR combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. Comparisons between the proposed design and other previously published methods show that the proposed design achieved better results for most tested benchmark circuits.

In [2], the authors describe an important application of linear feedback shift registers (LFSRs) with a generation of test vectors for digital circuits. A normal register configured to work as a test generator and, with the right choice of the tap sequence (XOR locations); the LFSR can generate all possible output test vectors. Furthermore, the pseudorandom behavior of the LFSR reduced the correlation between successive test vectors. However, this lack of correlation substantially increases the weighted switching activity (WSA) within the circuit-under-test (CUT). This often causes the power consumed during test mode operation. It is desirable to find a change to the LFSR structure that can re-order the outputs in a way that reduces switching activity without compromising the fault coverage. The main advantage of the proposed design combined with other low-power techniques for further savings in power consumption. A modified LFSR based on a new observation proposed to decrease the number of transitions in the CUT inputs.

In [3], the author says that the power dissipation during the testing cycle is more than that of the normal working of the chip. One reason is that as the chip size diminished the power dissemination of the circuit is likewise lessened. In BIST the LFSR used to produce the irregular patterns for testing a VLSI circuit. This paper describes a conventional linear feedback shift register, BS-LFSR and multiple WRTPG. In this paper, a qualitative analysis of different pattern generator architecture done based on delay and power. The Uniqueness of the work carried out in the field of BIST architecture for digital circuits so that testing of this circuit under test becomes easier with minimum power dissipation. These architectures will be used in the future for reversible logic so that power dissipation reduced. We observed a 70% improvement in the delay and a 5-6% improvement in the power analysis.

In [4], the author presents a novel idea for incorporating dual threshold voltage for Bit swapping LFSR (BS-LFSR) in order to get high power-efficient pattern generators for built in self-test (BIST) based VLSI architecture. In order to reduce the transition power due to high switching activity in test vector generation, the Bit-Swapped LFSR based pattern generators used. Bit swapping LFSR will generate random test sequences with low switching but the average power still remains high, for this reason, an alternate design methodology proposed. In the proposed design a convenient reduction in power attained by providing dual-threshold voltages to BS-LFSR architectures. As per the implementation, results observed that the leakage power of the circuit reduced and this ATPG circuit implemented in the circuit .However, the hardware implementation of the same Instead of dual-threshold a variable threshold BS-LFSR will be used in the future for further reduction in leakage power and hence a reduction in static power.

In [5], the authors Discusses about data path compression methods which were based on an LFSR. The basic approach used random seeds were initially modified and fed into the LFSR and it produced target faults. It was also detected path delay faults of undetectable path delay in the set of target faults which was in the same circuit hence it used a metric that measures the comparison between target and detected path delay faults and computed seeds which increases the value of the metric. The advancement of the method is it found seeds for detecting target faults even if the test cubes which was not compressed into seeds and this was achieved without computing new test cubes, instead of that LFSR was replaced in the circuit. Based on the metric, the quality of the test set is increased as it generated more seeds.

III. PATH DELAY MODEL

The previous system procedure selects the LFSR based on the test cubes which are required to detect the target faults, hence it becomes more complex as more fault models and more test cubes, needs to be compressed and another approach is used in that instead of computing the test cubes, compacting them and the compute seeds. Hence both rely on the fact which detects target faults is not unique and it is not required to match the given test cube perfectly.

The Path delay model is the most important to detect the targets for test generation procedure. When the criteria for path selection evaluated at the gate level, during the path selection process it is able to detect the path delay faults. It is not recommended for complex conditions, in this condition the brief procedure that accepts a set P of path delay faults, and replaces every undetectable path delay fault $p \in P$. In that detectable path delay fault r this is similar to p as possible. The Path delay model has some demerits (1) Path delay faults are important to detect associated with long paths and many of these faults are undetectable. (2) It could not be able to compress the given test for a path delay fault. (3) When the circuits have a large number of paths from inputs to outputs, hence the number of sub-paths becomes unmanageable. (4) Requirements for a memory storing the paths are very large. (5) Replacement is required for a large number of path delay faults.

The path delay fault is associated with the path is referred to as from the below fig 1 a-c-e-g and a rising transition at its source an in 4 input circuit. The Input b, d and f have constant values. A rising transition occurs at the input at time point t1 and the transition propagates along path a-c-e-g. When the circuit is fault-free, the value of the output g is 1 at the required time point t2. If we have path delay in the circuit in the path a-c-e-g, the value of the output g remains 0 at t2.

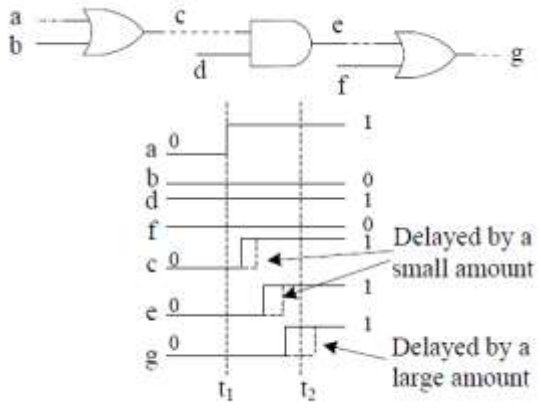

Fig 1: Path Delay Fault Model

III. PROPOSED METHODOLOGY

A. TRANSITION FAULT MODEL

The transition fault model captures delay defects on slow-to-rise transition or a slow-to-fall transition at a specific line in the circuit. In general transition faults are used for its simplicity in modeling scheme which can able to spot the defects and that will affect the delays at the input or output of the gate circuits. Under scan based test circuit, these faults are combined with an extra delay which is very large enough to cause the delay of any path through the fault site to exceed the clock period.

A slow-to-rise transition fault at line c is a 3 input circuit and Input b and d have constant values. The value of the input a change from 0 to 1 at time point t1, hence the rising transition occurs at line a. The transition propagates through the circuit, when the circuit is fault free, the value of the output e is to be 1 at the time point t2, here t2-t1 is the clock period and also due to the slow-to-rise transition fault at line c, the value of the output e remains o at the time period t2.

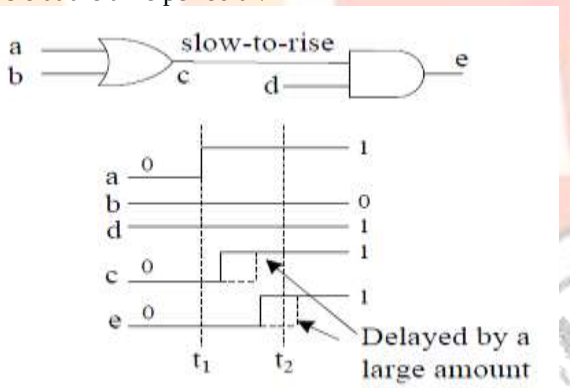

Fig 2: Transition Fault Model

B. STUCK-AT FAULT MODEL

Single stuck line is one of the fault model used in digital circuits and it is also used in post manufacturing of testing and not for design testing. Actually the model assumes one line or one node in the digital circuit is may stuck at logic 0 (Low) or logic 1 (High).when the line is stuck is called as fault.

Digital Circuit can be divided into two types as explained below:

1. Gate level or combinational circuits which contain no storage memory.
2. Sequential circuits which contain storage memory.

These faults model is applies to gate level circuits, or a block of sequential circuit which can be able to separated from the storage elements as mentioned above. A gate-level circuit would be completely tested by applying all possible inputs and checking which gave the right outputs, but it is completely impractical: For example an adder suppose to add two 32 bit numbers, require 264 = 1.8*1019 tests, taking 58 years at 0.1 ns/test.

The stuck-at fault model assumes that only one input will be faulty on one gate at a time, assumes that if more are faulty, a test which can detect any single fault, can easily find multiple faults in the circuit. Each of the faults is called a single stuck-at-0 (low) or a single stuck-at-1(high) fault, respectively.

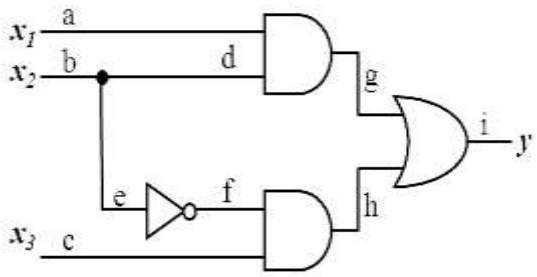

Fig 3: Stuck-At Fault Model

In the above circuit diagram contains 3 input lines are x1, x2, x3 and 1 output line y. Here Any line can be Stuck-at-0 (SA0) and Stuck-at-(SA1) respectively. Consider the fault types are k=2. The fault sites n: 9 and the single faults are 2x9=18 faults can occurs.

$x_1x_2x_3$	000	001	010	011	100	101	110	111
y	0	1	0	0	0	1	1	1
a SA0	0	1	0	0	0	1	0	0
a SA1	0	1	1	1	0	1	1	1
b SA0	0	1	0	1	0	1	0	1
b SA1	0	0	0	0	1	1	1	1
c SA0	0	0	0	0	0	0	1	1
c SA1	1	1	0	0	1	1	1	1
d SA0	0	1	0	0	0	1	0	0
d SA1	0	1	0	0	1	1	1	1
e SA0	0	1	0	1	0	1	1	1
e SA1	0	0	0	0	0	0	1	1
f SA0	0	0	0	0	0	0	1	1
f SA1	0	1	0	1	0	1	1	1
g SA0	0	1	0	0	0	1	0	0
g SA1	1	1	1	1	1	1	1	1
h SA0	0	0	0	0	0	0	1	1
h SA1	1	1	1	1	1	1	1	1
i SA0	0	0	0	0	0	0	0	0
i SA1	1	1	1	1	1	1	1	1

Fig 4: Truth Table for Fault free behavior and behavior of all possible stuck-at faults

C. BIT SWAPPING LFSR

The proposed BS-LFSR for Test Patter Generation to detect and minimize the fault in the testing circuit with low power consumption and it is based on new observations, hence the number of transitions are produced at the output of a BS-LFSR. Conventional LFSR is modified into bit swapping LFSR, which generates pseudo random pattern with less number of transitions between 0 and 1, which occurs in conventional LFSR. As internal switching activity is reduced hence causing less power dissipation in CUT and enhance its performance. To achieve low power dissipation, the proposed BF- LFSR introduced the stacking technique to reduce leakage current.

Two cells in an n-bit LFSR are considered to be adjacent if the output of one cell feeds the input of the second directly (i.e.,without an intervening XOR gate). Each cell in a maximal-length n-stage LFSR (internalor external) will produce a number of transitions equal to $2n-1$ after going through a sequence of $2n$ clock cycles. The sequence of 1s and 0s that is followed by one bit position of a maximal-length LFSR is commonly referred to as an m sequence. Each bit within the LFSR will follow the same m-sequence with a one-time-step delay. The m-sequence generated by an LFSR of length n has a periodicity of $2n - 1$. It is a well-known standard property of an m-sequence of length n that the total number of runs of consecutive occurrences of the same binary digit is $2n-1$.The beginning of each run is marked by a transition between 0 and 1; therefore, the total number of transitions for each stage of the LFSR is $2n-1$. This is can be proved by using the toggle property of the XOR gates used in the feedback of the LFSR.

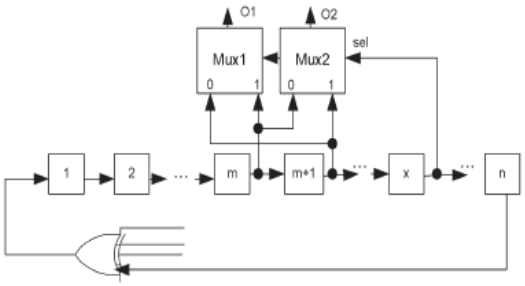

Fig 5: Bit Swapping Arrangement for an LFSR

LFSR outputs of m, m+1									Multiplexers outputs O_1, O_2						
States			Next states			transition			states		Next States		transition		
c_1	c_2	c_n	c_1	c_2	c_n	c_1	c_2	$\sum$	O_1	O_2	O_1	O_2	O_1	O_2	$\sum$
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			0	0	1	0	0	0			0	0	0	0	0
0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	1
			1	0	1	1	0	1			1	0	1	0	1
0	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1
			0	0	1	0	1	1			0	0	1	0	1
0	1	1	1	0	0	1	1	2	0	1	0	1	0	0	0
			1	0	1	1	1	2			1	0	1	1	2
1	0	0	1	1	0	0	1	1	0	1	1	1	1	0	1
			1	1	1	0	1	1			1	1	1	0	1
1	0	1	0	1	0	1	1	2	1	0	1	0	0	0	0
			0	1	1	1	1	2			0	1	1	1	2
1	1	0	1	1	0	0	0	0	1	1	1	1	0	0	0
			1	1	1	0	0	0			1	1	0	0	0
1	1	1	0	1	0	1	0	1	1	1	1	0	0	1	1
			0	1	1	1	0	1			0	1	1	0	1
∑Transitions						8	8	16					8	4	12

Fig 6: Truth Table for Possible and Subsequent States for Cells C1,C2 and Cn

IV. BENCHMARK CIRCUIT

The ISCAS'89 benchmarks have a set of 31 digital sequential circuits. The mentioned benchmarks were distributed on tape to participants of the Special Session on Sequential Test Generation, Int. Symposium on Circuits and Systems, May 1989, and are partially characterized in F. Brglez, D. Bryan, K. Kozminski in "Combinational Profiles of Sequential Benchmark Circuits", Proc. IEEE Int. Symposium on Circuits and Systems, pp. 1929-1934, May 1989. Each of the circuit is described in to two files as mentioned below: (1) A generic gate-level netlist with a list of equivalence collapsed faults. (2) A simple translator is included to read and write the netlist. Here no schematic diagrams.

- ✓ S27 implies Testing
- ✓ S208 implies Fractional Multiplier
- ✓ S298 implies Traffic Light Controller

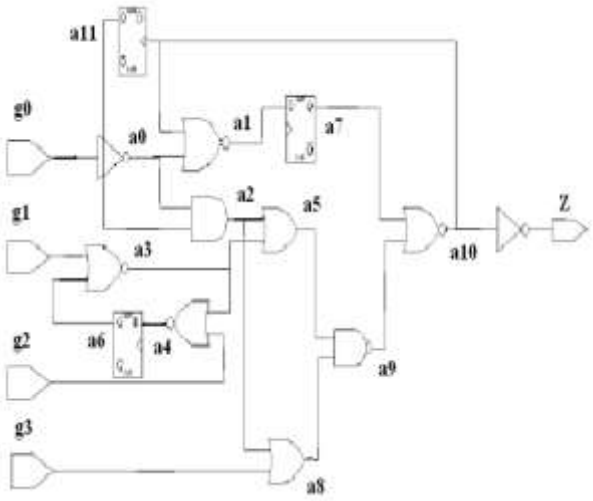

Fig 7: S27-Testing for Transition and Stuck-At Fault model

Based on the above S27 Testing circuit, we have generated simulation output for both the transition fault model and stuck-at fault model. The above S27 Testing circuit implies fault detection in the circuit based on the transition fault model and stuck-at fault model techniques.

A. S27 -Testing

S27 benchmark circuit is the standard sequential circuit for testing. Here we are used S27 benchmark circuit for a testing of the circuit. We are applying test vectors as inputs to the S27 benchmark circuit. Here I0, I1, I2, I3 are input of this below specified circuit. Generally S27 circuit have three scan circuits and then its scan inputs are 2^3=8.

Scan-in-state inputs are s0, s1, s2 and its scanned out denoted as s. LFSR register values initially we considered as "1010".We note that it is unspecified in the two un scanned state variables which implies can be used as scan-in state. In that more specified values under, more faults are to be detected. Actually, to obtain a shorter test from the given test of length, we assume search for the highest time unit which has unspecified values on all the unscanned since it is selected from the unspecified on the un scanned state variables. For a full-scan circuit, all the tests will be a length of two, due to the fact of all the states are fully-specified.

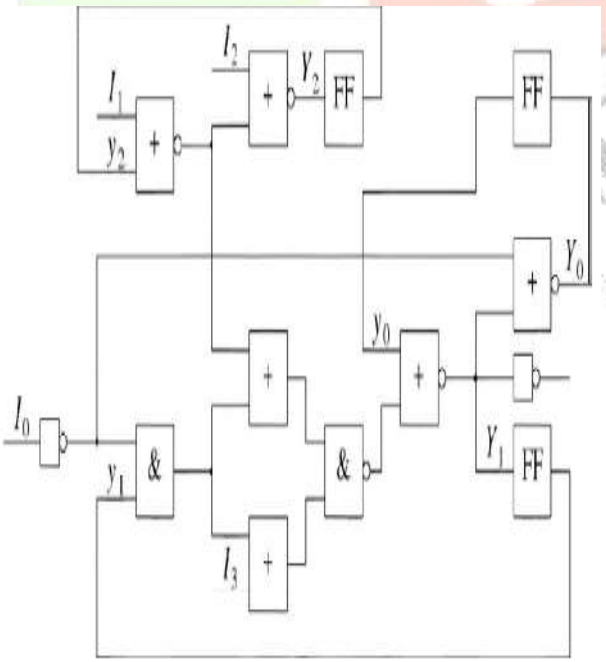

Fig 8: S27 Benchmark Circuit

u	Lfsr(u)	I value	o/p of s27
0	101 011 100 100	1 0 0 1	X
1	010 101 110 010	1 1 1 0	X
2	001 010 111 001	0 0 1 0	X
3	100 101 011 100	1 1 0 1	1
4	010 010 101 110	1 0 0 1	1
5	001 001 010 111	0 0 0 1	1
6	100 100 101 011	1 1 0 0	0
7	110 010 010 101	1 0 0 1	0
8	111 001 001 010	1 0 0 0	0
9	011 100 100 101	1 1 0 1	0
10	101 110 010 010	1 1 0 0	0
11	010 111 001 001	1 1 0 0	0
12	101 011 100 100	1 0 0 1	0
13	010 101 110 010	1 1 1 0	0
14	001 010 111 001	0 0 1 0	0
15	100 101 011 100	1 1 0 1	1

Fig 9: Output of S27 Benchmark Circuit

VI SIMULATION RESULTS

A. SIMULATION RESULTS FOR CONVENTIONAL LFSR

The following result for the Transition and Stuck-At Fault Model using Conventional LFSR are successfully simulated by using ModelSim Simulator. The result shown in Transition Fault Model by giving variable parameters such as Clk,reset,fa,fa1,fa2,z,z1,z2, etc and the Output is identified in tmp_ram Parameter and the final value is 11111.The result shown in Stuck-At Fault Model by giving variable parameters such as Clk,reset,fa,fa1,fa2,z,z1,z2, etc and the Output is simulated using Fault Simulator in tmp_ram Parameter and the final value is 11111.

I. SIMULATION OUTPUT FOR TRANSITION FAULT MODEL FOR CONVENTIONAL LFSR

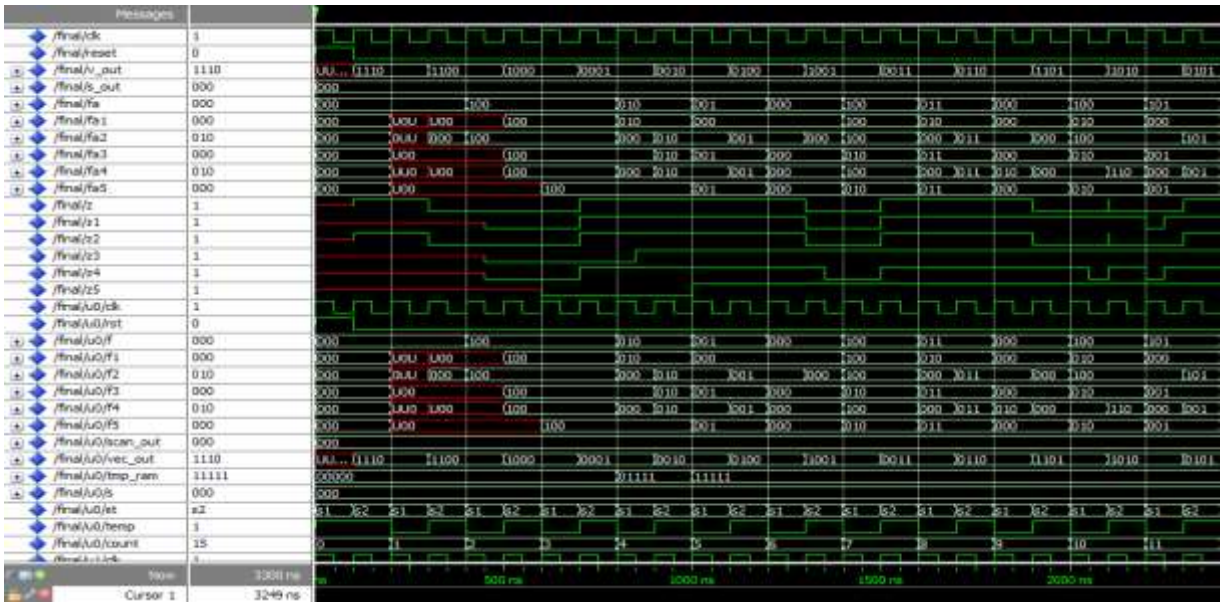

Fig 10: Simulation Output for Transition Fault model for Conventional LFSR

II. SIMULATION OUTPUT FOR STUCK-AT FAULT MODEL FOR CONVENTIONAL LFSR

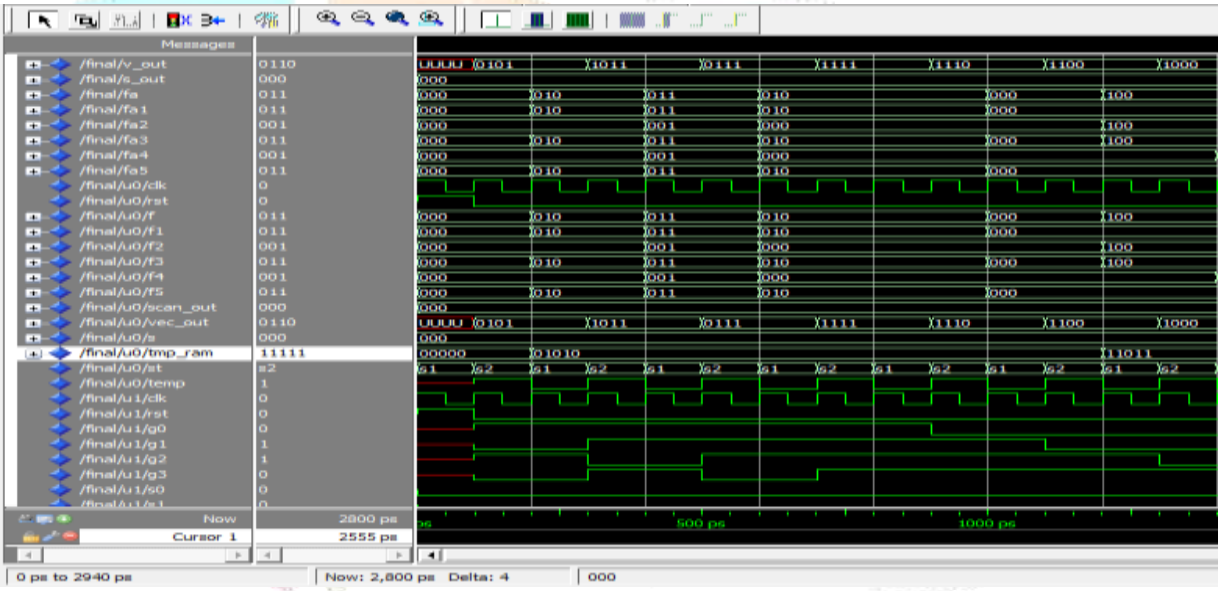

Fig 11: Simulation Output for Stuck-At Fault model for Conventional LFSR

B. SIMULATION RESULTS FOR BIT SWAPPING LFSR

The following result for the Transition and Stuck-At Fault Model are successfully simulated by using ModelSim Simulator. Bit-swapping LFSR reduces the transition which occurs in test pattern by using multiplexer. The fault coverage is improved by using observation point insertion which controls the internal path for propagating faulty values. The result shown in Transition Fault Model by giving variable parameters such as Clk,reset,fa,fa1,fa2,z,z1,z2, etc and the Output is identified in tmp_ram Parameter and the final value is 11111.The result shown in Stuck-At Fault Model by giving variable parameters such as Clk,reset,fa,fa1,fa2,z,z1,z2, etc and the Output is simulated using Fault Simulator in tmp_ram Parameter and the final value is 11111.

I. SIMULATION OUTPUT FOR TRANSITION FAULT MODEL FOR BIT SWAPPING LFSR

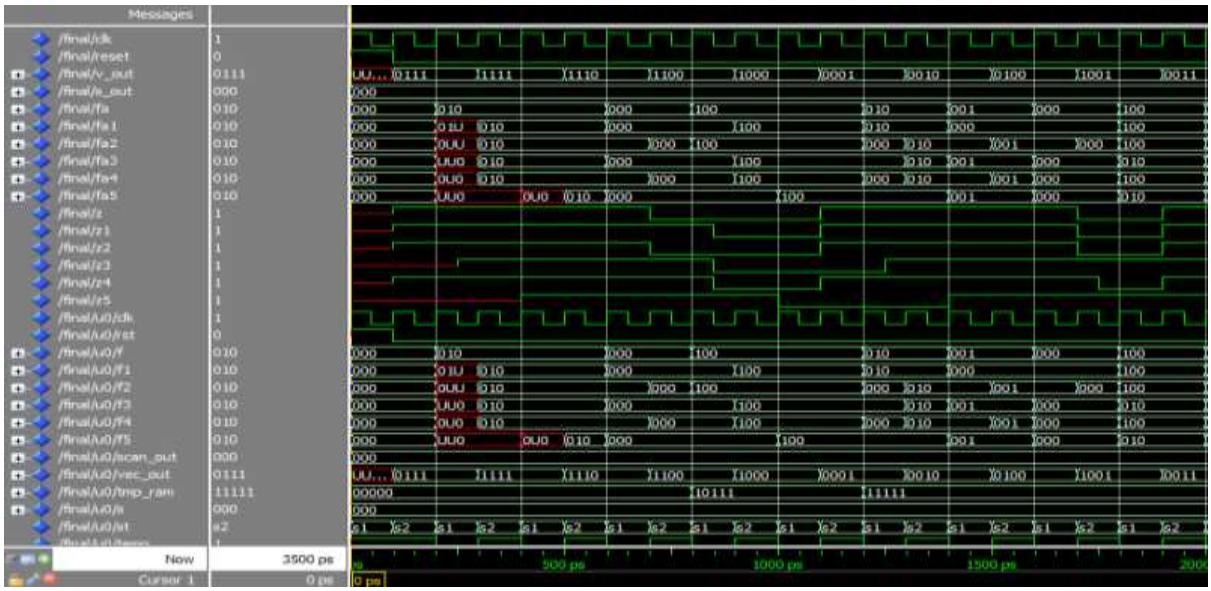

Fig 12: Simulation Output for Transition Fault model for Bit Swapping LFSR

II. SIMULATION OUTPUT FOR STUCK-AT FAULT MODEL FOR BIT SWAPPING LFSR

Fig 13: Simulation Output for Stuck-At Fault model for Bit Swapping LFSR

VII COMPARATIVE ANALYSIS

A. COMPARATIVE TABLE BETWEEN CONVENTIONAL LFSR AND BIT SWAPPING LFSR

The following table shows the comparison result for various benchmark circuit using Conventional LFSR and Bit-Swapping LFSR. Bit-swapping LFSR along with observation point insertion results in improved fault coverage for stuck-at and path delay faults. The proposed method also results in low power consumption compares with existing method.

Circuits	S27 LFSR	S27 BS-LFSR
Gates	10	10
FFS	3	3
PIs	4	4
Pos	1	1
LFSR	4	4
Total Seeds	8	6
Eff Seeds	4	3
Path Targ	8	8
Path Det	6	8
S-a-f Targ	5	5
S-a-f Det	4	5
Power(mW)	125.43	117.14

Fig 14: Comparative Table between Conventional LFSR and Bit-Swapping LFSR

B. POWER RESULTS ANALYSIS FOR CONVENTIONAL LFSR AND BIT SWAPPING LFSR

I. POWER RESULTS ANALYSIS FOR CONVENTIONAL LFSR

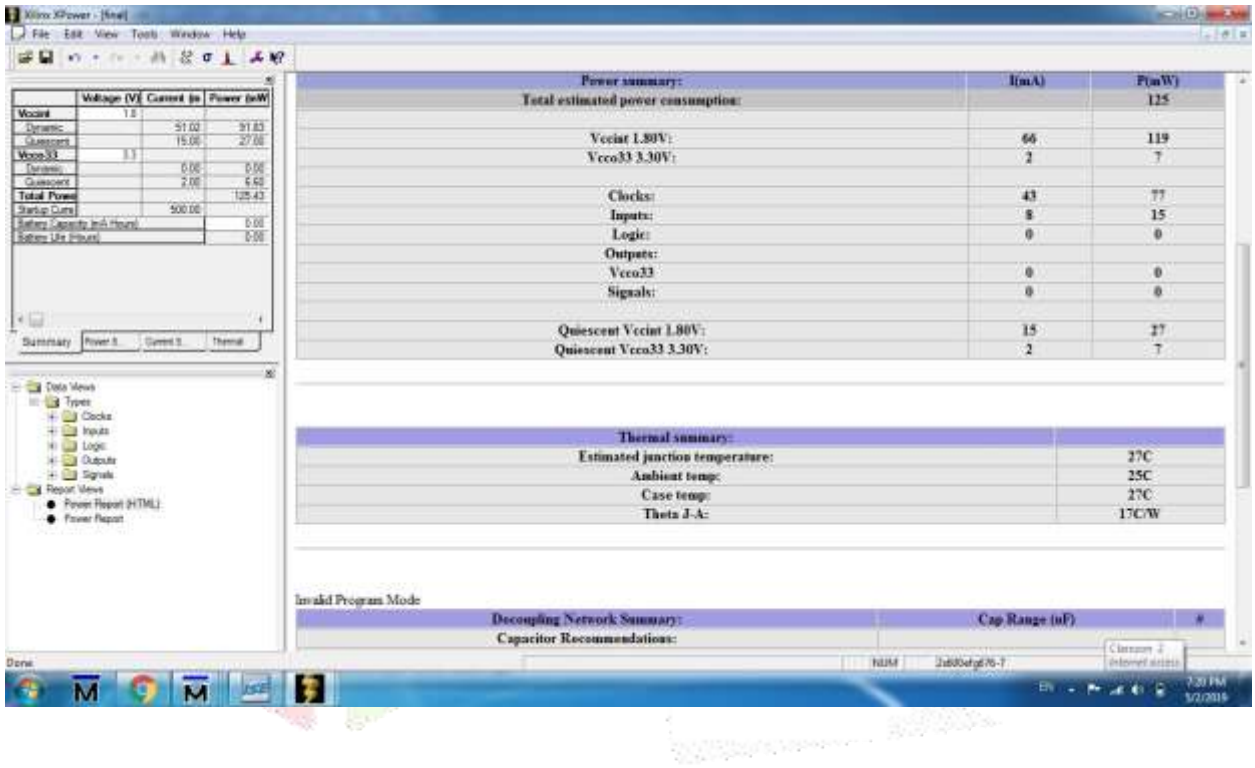

Fig 15: Power Results for S27 Circuit with Conventional LFSR

I. POWER RESULTS ANALYSIS FOR BIT SWAPPING LFSR

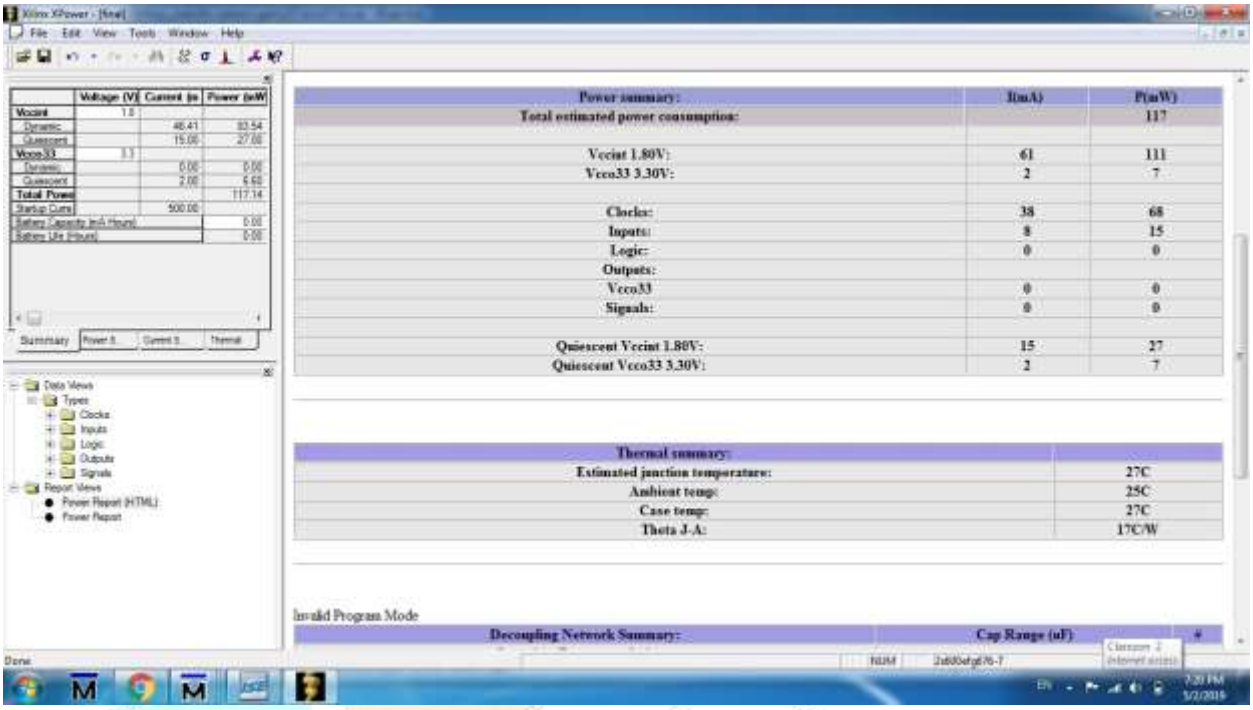

Fig 16: Power Results for S27 Circuit with Bit-Swapping LFSR

VIII CONCLUSION

Bit Swapping LFSR Based Test generation for Transition fault model and stuck-at fault model is successfully tested in S27 Benchmark Circuit. In our project we have used Sequential Circuit to Rising and falling transitions; based upon the transitions may result in changes in the delay faults in Transition Fault Model. Basically, it captures delay defects on slow-to-rise transition or a slow-to-fall transition at a specific line in the circuit and we have also used Stuck-At Fault model which is used for fault simulators and ATPG tools. Here the results show that faults are detected as well as simulated efficiently for the test pattern generation using BS-LFSR. The number is transitions in BS-LFSR is reduced by 50% for the swapped outputs compared to the conventional LFSR.As the number of transitions decreases the power consumption also reduced and efficiency will be increased.

IX FUTURE WORK

In future, techniques like test point insertion, fault injection technique can also be tried to improve the fault coverage for undetectable faults.

REFERENCES

[1] Abdallatif S.Abu-Issa and Steven F. Quigley “Bit-Swapping LFSR and Scan-Chain Ordering: A Novel Technique for Peak and Average Power Reduction in Scan-Based BIST” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL.28,NO.5,May 2009

[2] A.S.Abu-Issa and S.F. Quigley “Bit-Swapping LFSR for Low Power BIST” IEEE Electronics Letters, VOL.44, NO.6,March 2008.

[3] Abhilash Bagalkoti, Ramakrishna S, Rajashekar B S, Suhas B Shirol, Priyatamkumar ”Design and Implementation of 8 bit LFSR,Bit-Swapping LFSR and Weighted Random Test Pattern Generator : A Performance Improvement”International Conference on Intelligent Sustainable Systems (ICISS),2019.

[4] Dhanesh P, Jayanth Balaji “Dual Thershold Bit-Swapping LFSR for Power Reduction in BIST” IEEE International Conference on Advanced Computing and Communication Systems (ICACCS),2015.

[5] Irith Pomeranz “LFSR-Based Test Generation for Path Delay Faults” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Journal,DOI:10.1109/TCAD.2018.2812120,2018.

[6] Irith Pomeranz”A Compact Set of Seeds for LFSR-Based Test Generation from a `Fully-Specified Compact Test Set” IEEE Computer Society Annual Symposium on VLSI,Journal,DOI:10.1109/ISVLSI.2016.20,2016.

[7] Irith Pomeranz “LFSR-Based Generation of Multi cycle Tests” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Journal, DOI 10.1109/TCAD.2016.2587687,2016.

[8] Miroslaw Puczko “Low Power Test Pattern Generator for BIST” European Union,2015.

[9] Nicola Nicolici, Bashir M. Al-Hashim ”Multiple Scan Chains for Power Minimization during Test Application” IEEE Transactions on Computers, VOL. 51, NO. 6, June 2002.
[10] Nan-Cheng Lai, Sying-Jyan Wang, and Yu-Hsuan Fu ”Low-Power BIST with a Smoother and Scan-Chain Recorder Under Optimal Cluster Size” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL.25,NO.11,November 2006.
[11] Patrick Girard” Survey of Low Power Testing of VLSI Circuits” IEEE Design & Test of Circuits, Journal, Page No. 82-92, May-June 2002.
[12] Seongmoon Wang”A BIST TPG for Low Power Dissipation and High Fault Coverage” IEEE Transactions on Very Large Scale Integration (VLSI) Systems,VOL.15,NO.7,July 2007.
[13] Seongmoon Wang and Sandeep K. Gupta” LT-RTPG: A New Test-Per-Scan BIST TPG for Low Switching Activity” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, VOL.25,NO.8,August 2006.
[14] Saraswathi.R ,Manikandan.R ”Design of LFSR using Low Power Test Pattern Generator” IEEE International Conference on Networks & Advances in Computational Technologies (NetACT),July 2017
[15] Sathesh Kumar.G , V. Saminadan,”Low Power LFSR for BIST Applications”,IEEE Second International Conference on Intelligent Computing and Control Systems (ICICCS),2018.