IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

A Novel Power Efficient Division Architecture Using Reversible Computing

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Abstract- *Color Space Conversion is an integral part of various computer vision applications such as face detection, object detection and surveillance systems. To achieve ease in processing, feature extraction, compression and storage of image and video data color space conversion technique is required. If computation is performed on gray images, which has 8 bit wide pixel, rather than color images, which has 24 bit wide pixel the resources required for real time implementation of all these applications will be reduced. Reversible logic has received a great deal of attention from many researchers over recent years for its enormous potential for application in quantum computing and nanotechnology due to its ability to reduce power consumption, which is the main requirement in low power VLSI design. A color space conversion scheme using reversible logic gates is presented here. Color-to-gray scale conversion using reversible logic aims at embedding the chromatic information of a full color image into its gray scale version such that the original color image can be reconstructed in the future when necessary. Color Channel averaging method is implemented in this paper. By converting RGB to Gray scale using reversible logic it helps to increase the operation speed and reduce the storage space. Implementation of color space converter using reversible logic nullifies the internal energy dissipation as it provides a computation that does not result in information loss. The implementation of reversible logic circuits for converting RGB to Gray scale was done and the functionality verification was done on Spartan xc3s400 FPGA platform. The results are evaluated in terms of hardware utilization and power for FPGA.*

Keywords-Reversible Divider, Color Channel Averaging, Spartan xc3s400 FPGA

I. INTRODUCTION

Nowadays, power consumption presents an essential issue when designing embedded video applications. Mobile electronic devices face fundamental challenges related to energy constraints as a result of their sizes and weights. This fact has pushed designers to search for new methods to have low-power consumption for image and video processing applications[12].

In the present era of power hungry devices, quantum technology has emerged as a promising technology. The main theory behind which the quantum logic is based on, is the law of conservation of energy. Law of conservation of energy states that energy can never be created nor destroyed; rather it can only be transformed from one form to another. The fundamental law of conservation of energy is incorporated in the design of systems, to be precise, the circuits in quantum logic/ quantum technology. Quantum technology has shown promising results in power consumption of a circuit. Theoretically it is proved that the quantum logic circuits does not consume any power for internal computations.

Efficient conversion in color space especially RGB to gray scale color space conversion plays a key role in reducing the computational complexity and cost for algorithms that find application in computer vision. The reduction in computations is achieved by reducing the color channels. The main challenges involve preservation of details of color, luminance and edge.

Reversible logic design circuit is motivated by its applications in low-power electronic design. It has recently attracted significant attention. A reversible circuit should have these features:

- Use minimum quantity of reversible gates.
- Produce minimum number of garbage.
- Use minimum constant inputs.

In this paper, we propose to use color channel averaging method using Reversible Logic Divider which would perform the conversion of RGB to Grayscale image using minimum area, power and delay. The same is to be verified on Spartan-3 FPGA.

This paper is organized as follows. Section II presents the literature survey based on the work carried out in project. i.e., topics related to different type of reversible logic circuits using Adders, multiplier, divider, Multiplexers, ALU and various image processing applications using reverisble logic. The basic details reversible logic gates, division, applications and advantages of reversible circuits are presented in Section III. Section IV discusses the objectives, detailed methodology of the architecture on the average color channel method and the proposed Reversible divider. Section V presents the simulation and hardware implementation results carried out using Xilinx and FPGA Platform. Finally, conclusion and the future scope of the project is presented.

II. LITERATURE SURVEY

In modern computational technologies, a major challenge is the design of devices with smaller size, low power dissipation, and high speed. In order to achieve better optimisation in power dissipation, size and speed, it is necessary to find a technological change. Researchers are trying to find ways and means by introducing many architectural and behavioural changes in the available technologies. One such possible solution is to design digital circuits based on reversible logic and implement them in quantum cellular automata (QCA). In a multiplication process, partial product generation and the addition of partial products are the major factors contributing to the propagation delay. In this paper, Urdhwa Triyakbhyam based Vedic multiplier using reversible logic is proposed by A. Kamaraj et al.[1]. Vedic multipliers result in faster partial products with less number of steps. Ripple carry adders are used for adding the partial product results to obtain the final product. The multiplier modules are constructed using fault-tolerant reversible KMD gates and hence, the proposed multiplier is a fault-tolerant Vedic multiplier. The designed multiplier is realised in QCA. In the proposed reversible Vedic multiplier[1], quantum cost is reduced up to 72 %, garbage output is reduced up to 87 %, constant input is reduced up to 87 % and the number of gates are reduced up to 57 % compared to the existing conventional and Vedic multipliers.

In digital circuits power dissipation can be significantly reduced using reversible logic. It is becoming prominent in applications involving quantum computing and low-power design. A new reversible full/half adder using combination of Feynman (CNOT), Toffoli (CCNOT) and Fredkin (CSWAP) gates is proposed. Aditya et al.[2] proposed reversible full/half adder is found to be efficient in reducing constant inputs (ancilla bits), garbage outputs, number of transistors and gate count. The proposed full adder shows 47% reduction in power dissipation, 33% in constant inputs, 50% in garbage outputs and 67% in number of transistors in comparison with similar work present in literature. The energy saving factor of the proposed full-adder is found to be 2.01.

Conventional Complementary metal oxide semiconductor circuits (CMOS) dissipate energy in the form of bits of information. This dissipation of energy is in the form of power dissipation and plays a very important role as far as low power design is considered. Today, most digital circuits are being designed using Reversible Logic. Design based on Reversible Logic helps in reducing heat dissipation, allowing nearly energy free computation, allowing higher circuit densities and enabling better testing of faults. A novel design for a Reversible 8-bit ALU is proposed by Deeptha et al.[3] . The 8-bit ALU is designed by cascading 1-bit ALUs. The two major units of a 1-bit ALU are the control unit and the adder unit. For the control unit, the Control Output Gate (COG) has been used and for the adder unit the Haghparast and Navi Gate (HNG) has been used. The most significant aspect of this paper[3] is that as compared to other papers, this ALU design has reduced gate count, and transistor count. The propagation delay was found to be significantly lesser at a value of 5.52ns when compared with the value of 8.29ns for an existing design. Simulation and verification of the proposed design was performed using Cadence 180nm technology software tool.

Multiplexing is the generic term used to designate the operation of sending one or more analogue or digital signals over a common transmission line at dissimilar times or speeds and as such, the scheme we use to do just that is called a Multiplexer. In digital electronics, multiplexers are similarly known as data selectors as they can “select” each input line, are made from individual Analogue Switches encased in a single IC package as conflicting to the “mechanical” type selectors such as standard conservative switches and relays. In today era, reversibility has become essential part of digital world to make digital circuits more efficient. Ashima Malhotra et al.[4] proposed a new method to reduce quantum cost and power for various multiplexers. The results are simulated in Xilinx by using VHDL language. In [4] they have presented the reversible multiplexers using MFRG gates. The proposed reversible multiplexers are better than the existing designs in terms of hardware complexity and quantum cost.

The proposed Multiplier and canny edge detection by Sujatha et al. [5] is coded using VHDL synthesized and simulated using Xilinx ISE 14.5i tool. The face recognition is performed using Matlab 2012.The face image is a physiological biometrics used to identify a person for variety of applications. The novel concept of converting two face images of a person into single image using steganography is introduced. The multiplier for edge detection of face image in [5] is designed based on the new concept techniques of reversible logic, MUX and Vedic multiplication. The resize of face images and Gaussian filter are used in preprocessing unit. The coefficient of DWT and LBP of face images are fused and applied to SOM input. The final features are obtained from the output of SOM. The final features of face database and test face images are compared using ED to compute performance parameters. It is observed that the performance parameters of proposed method are better compared to existing methods. In future, SOM may be replaced by Support Vector Machine (SVM) and implemented on hardware for real time testing. It is observed that the performance of the proposed method is better compared to existing methods.

Power crisis is a vital problem in today’s world. In recent years, the growing market of electronic systems suffers from power dissipation and delay removal problem. Shachchidanand Nagagach et al.[6] proved that the one-to-one mapping between the inputs and outputs of reversible circuit drastically reduces the power consumption and delay consumed of a circuit. There are four major design parameters of reversible circuits. First is the gate count which is the number of gate are used in the circuit. Second is the quantum delay. Third is the number of ancilla inputs which are constant inputs which are used to maintain the reversibility of the device. Fourth is the number of garbage outputs i.e. output signals which are not used as inputs to other gates and are only there to maintain reversibility. In this paper[6] the survey of design central processing unit is based on reversible gate and parameter.

The simulation result of proposed DWT & IDWT structure by Kowsalya et al.[6] using various adders have been evaluated and effective comparison is given. In order to verify the proposed DWT & IDWT architecture, the functional simulation has been carried out using Xilinx 14.7. the ASIC implementation of proposed design has been carried out using cadence EDA tool. The synthesis and design for testing is realized using “cadence genus” & the physical design implemented using “cadence innovus”. In order to justify the proposed functionality we simulated the same algorithm using matlab. For the matlab simulation the standard test image lenna of size 1024 *1024 has been studied. The input and output of the image during simulation is tabulated. Further the

efficiency of the algorithm is evaluated using the image quality metrics AD, MD, PSNR, NCC, SC, NAE and MSE. The corresponding values of each image quality measures are also tabulated. The average difference of the original and output images are zero and mean square error is less. The proposed design of DWT and IDWT architectures are synthesised and tested using design for testing. The lifting and Haar wavelet transform based DWT & IDWT architectures using reversible and irreversible logic gates have been proposed in this paper, in which the comparison between the reversible and irreversible architectures of the DWT & IDWT have been made. The DWT architecture using reversible logic has a lesser delay than the irreversible logic gates based DWT architectures and it has been proven with results. The tested image quality of the output image is equal to the input image.The scaling of the proposed architecture is possible. The N*N high-quality images also can be processed using the proposed architecture with high efficiency. The watermarking using proposed DWT & IDWT also implemented and verified in the paper [6].. Based on the entire contribution of our work, proposed architecture requires dataflow control units for its efficiency.The clock performance should be improved.

A reversible encoder/decoder circuit for image steganography proposed by BikashDebnath et al.[7] is at nanoscale. This is not only effective in terms of low power dissipation but also focuses on the important aspects of a reversible computing. Feynman gate is used as a basic element to achieve the proposed designs. A secure Nanocommunication process for image steganography is clearly depicted in this paper. The proposed encoder/decoder has 0.335 μm2 device density that confirms 28.33% reduction over traditional CMOS-based implementation. To reduce the circuit complexity, a GIis considered. Several possible defects are explored to achieve fault free implementation. The proposed encoder/decoder circuit in[7] dissipates very low energy. Though the input to the encoder/decoder circuit is considered as a sequence of 8 bits, the circuit can be used for high number of bits in sequence. The functional efficiency of the circuit is analysed at different temperatures and its accuracy is measured. One of the important features of this steganographic circuit is that it possesses a non-deterministic aspect and inherent resistivity againstpower analysis attack, which enhances the security of the hidden data.

Reversible Logic is an emerging technology; it has hellocious applications in various fields. Reversible logic implementation reduces loss of entropy because of bit manipulations. Conservative reversible logic gate obeys reversible logic rules and also satisfies the property that there is equal number of 1s in the outputs as in the inputs. In this work, modified design of SCRL (Super Conservative Reversible Logic) gate for the design of reversible quantumcircuit is presented. Pradeep et al.[8]proposed a SCRL Integrated Qubit gate has 1 control input which swaps n-1 depending on control input. Barrel shifter forms an integral component of many computing systems. As an example of using the proposed SCRL gate to design efficient reversible quantum circuits, the design of reversible barrel shifter with zero ancilla inputs and zero garbage outputs is illustrated.

Emerging technologies in VLSI, enables tointegrate huge devices on single unit area to build lower power portable devices. In order to build low power systems there is a need for new technology which adapts logic that conserves energy anddissipates no power. Reversible circuits are designed using reversible gates in which number of outputs is equal to the number of inputs and thereis a one to one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Krishnaveni et al.[9] proposed a method where each module and sub-modules of HMMD converter based on reversible logic is designed using reversible gates. In this we had tried to optimize the parameters such as area, number of constant inputs, garbage outputs, power and delay associated with the circuit. The experimental results obtained by implementing HMMD converter in CADENCE EDA 90nm technology in[9] shows the considerable reduction in power, area and delay in comparison with the HMMD converter designed using conventional gates.

Srikanth et al.[10] brings out a 32X32 bit reversible Vedic multiplier using "UrdhvaTiryakabhayam" sutra meaning vertical and crosswise, is designed using reversible logic gates, which is the first of its kind. Also they have proposed a new reversible unsigned division circuit in [11]. This circuit is designed using reversible components like reversible parallel adder, reversible left-shift register, reversible multiplexer, reversible n-bit register with parallel load line. The reversible vedic multiplier and reversible divider modules have been written in Verilog HDL and then synthesized and simulated using Xilinx ISE 9.2i. This reversible vedic multiplier[11] results shows less delay and less power consumption by comparing with array multiplier.The design of 32x32 bit Vedic multiplier and a divider is logically verified using XILINX 9.2i. Based upon the simulation results discussed, the multiplier has 35.557ns improvement in delay and 3.43 mW improvement in power, hence reversible vedic multiplier is high speed and low power multiplier.

III.REVERSIBLE LOGIC APPROACH

3.1 Basics of Reversible Circuit Design

Design and implementation of reversible circuits has to comply with a set of rules that differentiates it from the conventional combinational circuits.

- Number of Inputs = Number of Outputs
- Circuit has to be logically reversible - unique mapping between input and output.
- Circuit has to be physically reversible - circuits are backward deterministic.
- Fan-out is not permissible in reversible circuits.
- Feedback paths should not exist in reversible circuits.

The design parameters and constraints to be considered while designing reversible circuits are:

1) Quantum cost - The number of elementary quantum gates required to implement a function.
2) Garbage Output - The output bits added to a reversible functional block to achieve reversibility.
3) Ancilla Input - The input bits added to a reversible functional block to achieve reversibility.
4) Gate Count - The number of reversible gates used in the reversible functional block

3.2 Reversible Approach to division

In a fixed point division, inputs are divisor V and dividend D, and outputs are quotient Q and remainder R such that D = Q × V + R. In every step i, the divisor V is shifted i bits to the right which represents 2-iV. If 2-iV is less than partial remainder Ri, then quotient bit qi is set to 1 otherwise it is set to 0. Then a new partial remainder Ri+1 is calculated as follows Ri+1 = Ri – qi×2-i×V which is equivalent to Ri+1 = 2Ri – qi×V. There are two approaches to perform division operation.

3.2.1 Restoring Division

In restoring approach, at every step, the operation Ri+1 = 2Ri – V is performed. If subtraction result is negative, the partial remainder is restored to the correct value by performing the addition operation Ri+1 = Ri+1 + V.

3.2.2 Non-Restoring Division

In non-restoring approach, if subtraction result is negative, the partial remainder is not restored immediately. It is based on the inspection that a restoring step of the form Ri = Ri + V followed by the next partial remainder calculation step Ri+1 = 2Ri – V can be combined into a single operation Ri+1 = 2Ri + V. Thus, if the quotient bit qi = 1, then the next partial remainder is calculated by performing a subtraction. On the other hand, if the quotient bit qi = 0, instead of restoring the partial remainder, the next step is calculated by performing the addition of the divisor to the partial remainder. If the last quotient bit is 0, then the partial remainder is negative due to trial subtraction. Therefore, an essential correction step is to restore the remainder by adding the divisor.

3.3 Advantages of Reversible Logic

- Landauer has shown that for irreversible logic computations, each bit of information lost, generates kTlog2 joules of heat
- Bennett showed that kTln2 energy dissipation would not occur, if a computation were carried out in a reversible way
- Whenever a logic operation is performed, the computer erases information. All these logic operations are irreversible dissipating a lot of heat.
- The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit.
- As Moore's law continues to hold, processing power doubles every 18 months.
- Reversible logic operations do not erase (lose) information and dissipate much less heat.

3.4 Applications of Reversible Gates

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance .it include the area like

- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.

IV.PROPOSED SYSTEM

4.1 Objectives

- To convert RGB to Grayscale image conversion by color channel averaging method using Reversible Logic Circuit.
- To verify implementation of reversible logic using Spartan-3 xc3s400 FPGA Platform.
- Finally testing the RGB to Grayscale conversion in MATLAB.

4.2 RGB to Gray-Scale Conversion Circuits Using Reversible Logic

Complex image processing algorithms like computer vision tasks, demands a high performance and low-power RGB to gray-scale conversion circuits to reduce the computational load on the channel. Several methods have been proposed in the past for efficient color space conversion from RGB to gray-scale. Widely used methods include averaging the values at each color channel, desaturation of color space, weighted sum method and other color-to-gray approaches. We are using the Color channel averaging method as the main color-space conversion schemes for RGB to gray-scale conversion that are used to realize the reversible hardware in this paper.

4.3 Color Channel Averaging Method

Averaging is the most common gray-scale conversion technique.

Gray Component = R + G + B /3 ---------- (1)

This method is considered to be the simplest method as it is easy to implement and optimize the hardware.

4.3.1 Block Diagram of reversible color channel averaging circuit

Block Diagram of the reversible color channel averaging circuit is as shown in Fig 4.1.

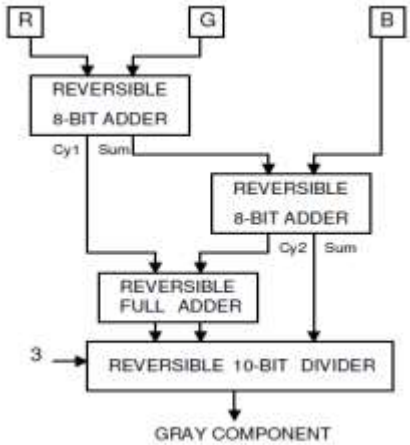

Fig. 4.1 Block Diagram of Reversible Color Channel Averaging

4.3.2 Block Diagram Description:

The following are the circuits used in the Reversible Color Channel Averaging:

- 8-bit reversible adder for calculating sum of R and G components(result will be 9 bits)
- 8-bit reversible adder to add B component to the sum of R and G(result will be 9 bits)
- Reversible full adder to add the carry generated from two 8-bit adders
- Reversible Divider circuit with 10 bit dividend and divisor.

4.4 Reversible Adder

The full adder circuit used, is the reversible adder which has minimum gates and depth. The full adder circuit is as shown in Fig. 4.2.

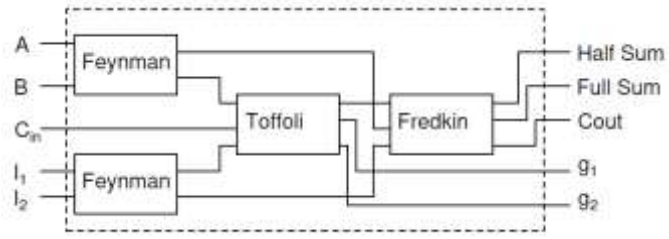

Fig 4.2. Reversible Full Adder

8-bit reversible adder is implemented using 8 reversible full adders. A Full adder has a GC of 4, AI of 2, GO of 3 and QC of 12

4.5 Reversible Divider:

A fixed point divider is employed in the proposed architecture as shown in Fig. 4.3.

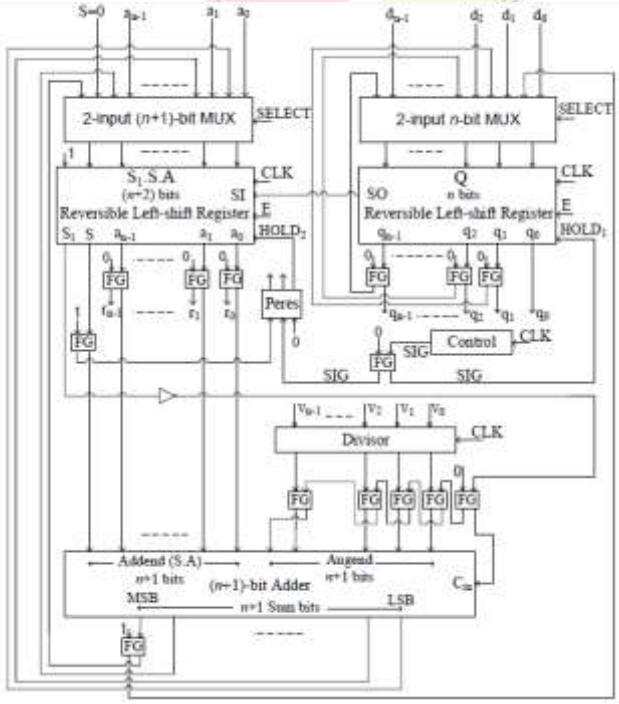

Fig. 4.3 Reversible Divider Block Diagram

4.5.1 Components of the Proposed Reversible Divider

The following are the components to design reversible sequential division hardware:

- Reversible multiplexers (MUXs),
- Registers,
- Parallel-in parallel-out (PIPO) left-shift registers and
- Parallel adder are required

4.5.2 Block Diagram Description

Fig. 4.3 shows the proposed reversible design of nonrestoring division circuit for positive integers. It has two PIPO reversible left-shift registers: one is n+2 bits named as S1.S.A and other is n bits named as Q. It also contains an nbit reversible register to store the divisor. Initially S = 0, A (an-1an-2…a0) = 0, D (dn-1dn-2…d0) = dividend, V (vn-1vn-2…v0) = divisor and SIG = 0. When the division operation is completed, register Q (qn-1qn-2…q0) contains the quotient and A (an-1an-2…a0) contains the remainder. If SELECT = 1 then 2-input (n+1)-bit MUX selects S = 0 and A (an-1an-2…a0) = 0, and n-bit MUX selects dividend D (dn-1dn-2…d0). During the clock pulse when E = 1 and HOLD2 = 0, the input S1 = 1 and output data from (n+1)-bit MUX are loaded into S1.S.A, and when HOLD1 = 0, outputs from n-bit MUX are loaded into Q in parallel. When E = 0, both S1.S.A and Q act as left-shift registers. Initially, the value of S1 is not important, it is important only after the left shift of S1.S.A.Q (S1.S.A.Q means SO of register Q is connected to SI of S1.S.A), thus the value of S is shifted to S1 which is used to select the operation to be performed on S.A and V. If S1 is 1 then S.A+V is performed, otherwise, S.A–V is computed. Addition or subtraction is performed using (n+1)-bit reversible parallel adder. The complement of the most significant bit (MSB) of the sum is loaded into q0 bit position of register Q and (n+1)- bit sum is loaded into S.A during next clock pulse when SELECT is 0. It requires 2n+1 clock pulses to store the value of quotient into register Q.After 2n+1 clock pulses, Control outputs a high signal SIG. This signal is connected to HOLD1 input of Q register. Thus Q stores the quotient indefinitely. AND operation of (S, SIG) which can be implemented using Peres gate is connected to HOLD2 input. If S is 0, then remainder restoration is not required, HOLD2 will be high and A will store the remainder indefinitely. If S is 1, then remainder restoration is necessary. During 2n+1 clock pulse, as S1 is 1, restoration is performed by adding V with S.A. During the next clock pulse, the correct value of remainder is loaded into S.A when E is 1. After remainder restoration, S must be 0. This results HOLD2 to be high and A will store the remainder indefinitely.

V.RESULTS AND DISCUSSIONS

The proposed system is implemented using Xilinx. The wave window of the Color Channel Averaging is shown in the Fig.5.1. Below:

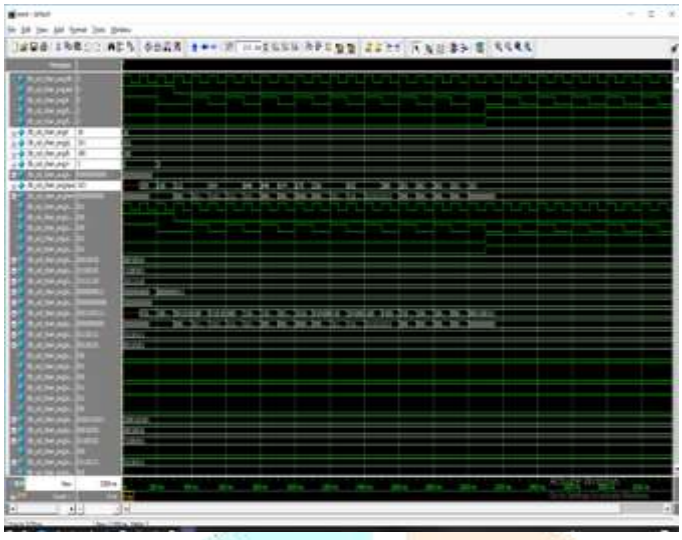

Fig 5.1 Color Channel Averaging Wave Window

The wave window of the 10 bit Reversible Divider is shown below in the Fig 5.2.

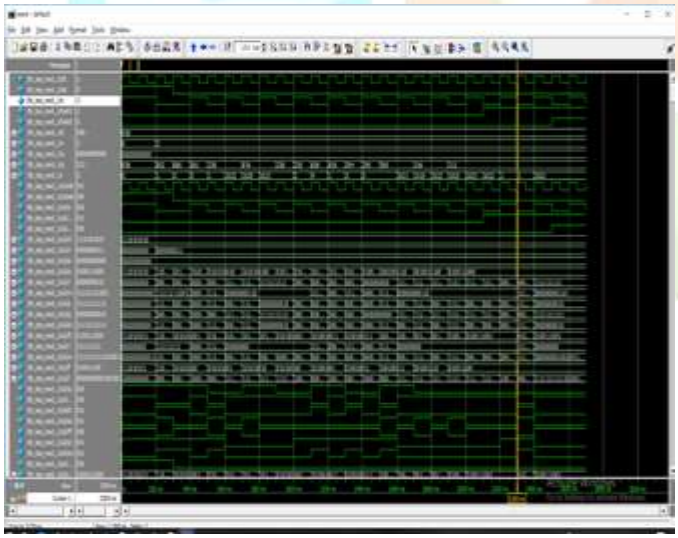

Fig 5.2 10 bit Reversible Divider Wave Window

Using the Architecture of Reversible Color Channel Averaging the synthesis report about the timing summary and timing details that are obtained are shown in the Fig.5.3.

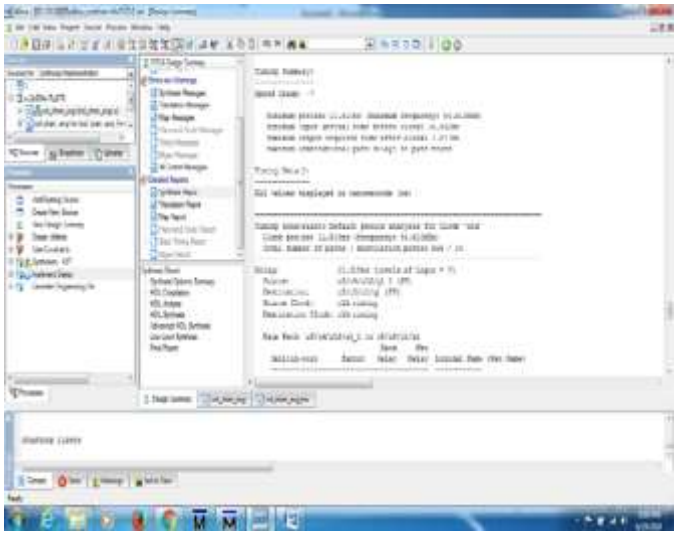

Fig 5.3 Synthesis Report on Reversible Color Channel Averaging

Design overview summary of logic utilization and logic distribution are shown in the Fig 5.4 below.

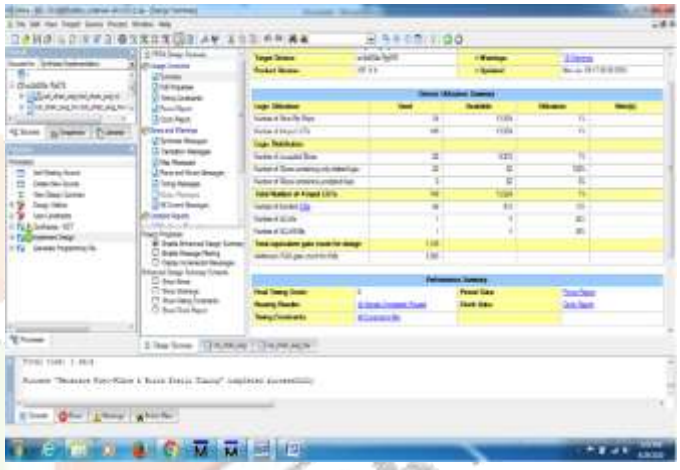

Fig 5.4 Summary on Device Utilization on Color Channel Averaging

The power report obtained on color channel averaging is shown in the fig 5.5. below.

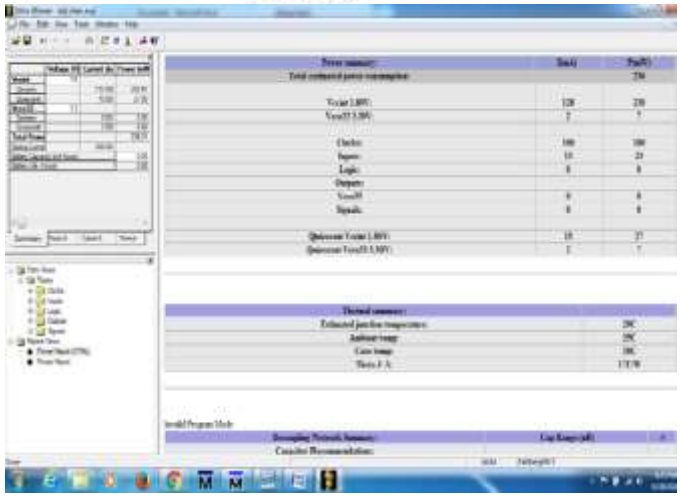

Fig 5.5. Power Report on Reversible Color Channel Averaging

The synthesis report about the timing summary and timing details that are obtained using 11-bit reversible division circuit is shown in the Fig.5.6 below.

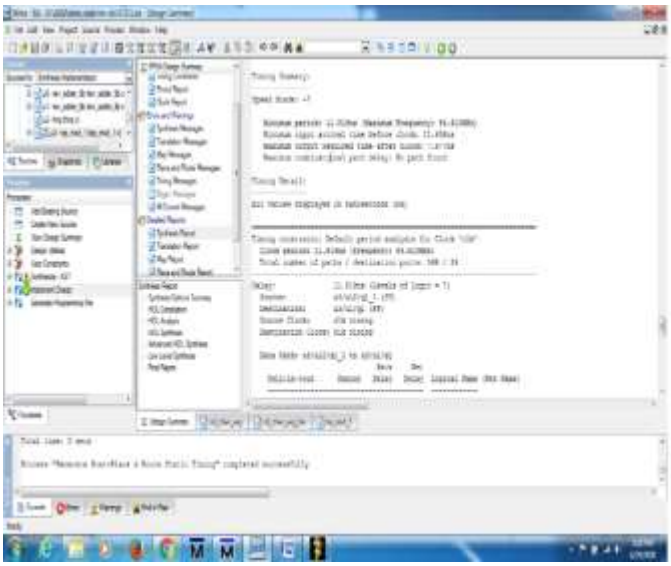

Fig 5.6 Synthesis Report on 11-bit Reversible Division Circuit

Design overview summary of logic utilization and logic distribution of 11-bit reversible division circuit is shown in the Fig 5.7 below.

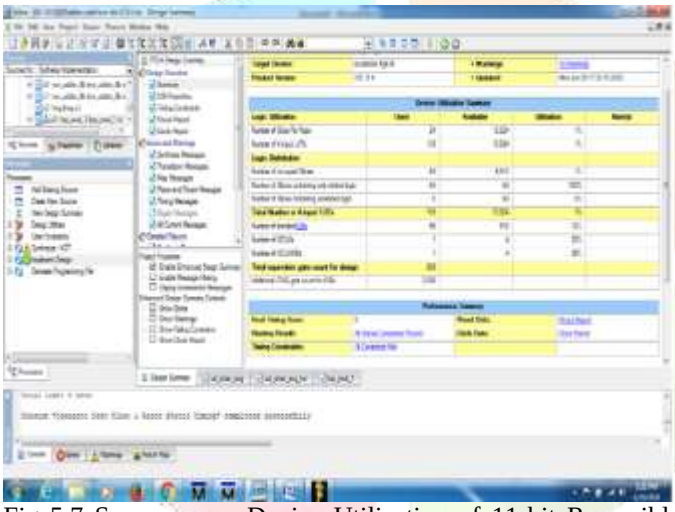

Fig 5.7 Summary on Device Utilization of 11-bit Reversible Division Circuit

The power report obtained on 11-bit Reversible Division Circuit is shown in the fig 5.8 below.

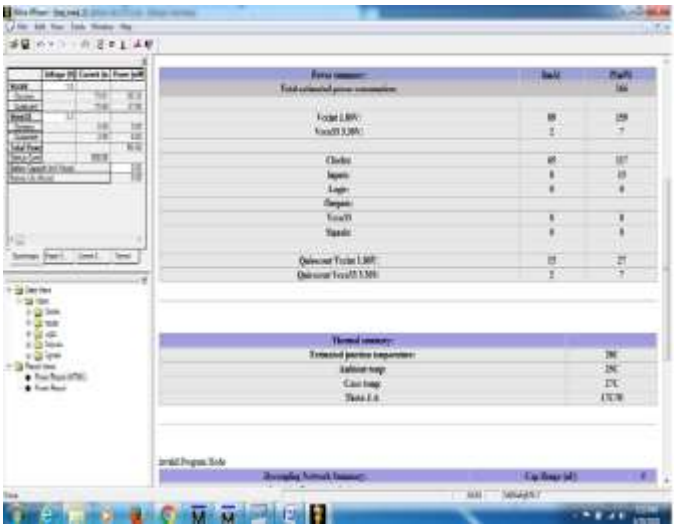

Fig 5.8 Power Report on 11-bit Reversible Division Circuit

Reversible logic implementation was done to extract the delay and quantum cost of the proposed architectures. The QC, AI count and GB count for individual blocks and for complete color channel averaging are given in Table I below.

Table I: Reversible logic parameters for individual blocks in color channel averaging

Color Channel Averaging				
Design Block	***GC***	***AI***	***GO***	***QC***
Full Adder	4	2	2	12
8-Bit Adder	32	16	22	86
Divider	197	115	128	610
Complete color channel averaging module	250	149	178	770

Functional verification of the proposed architectures for RGB to Gray scale color space conversion using reversible logic was done using Spartan-3 FPGA. The above simulations design was done using Verilog Hardware Description Language. Fig 5.9 below shows the example of an image which is converted from RGB to gray in Matlab after applying Reversible Logic Divider.

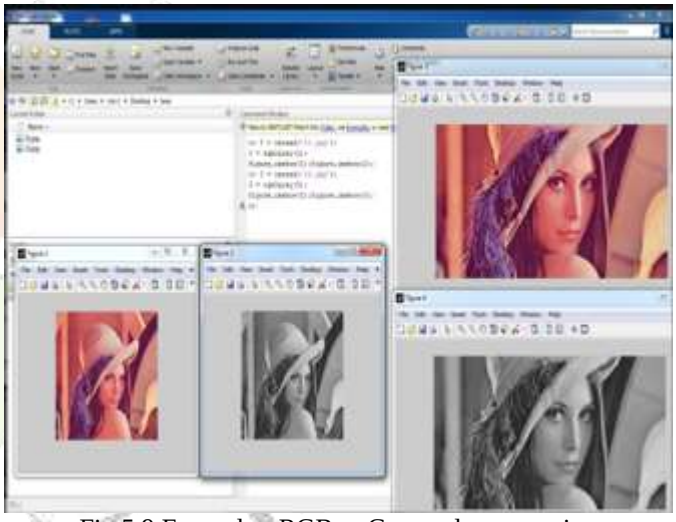

Fig 5.9 Example - RGB to Grayscale conversion

VIII. CONCLUSION

This paper proposes the architecture for a reversible logic based color space conversion unit for RGB to Gray scale conversion. This work uses an efficient approach for designing reversible divider circuit using the new reversible logic blocks. In implementing reversible division hardware, our main focus is in terms of quantum cost, garbage outputs, constant inputs and hardware complexity. It should be a promising step towards high speed and low power design and regularity in this era. Appropriate method for converting the RGB to Grayscale was suggested inorder to establish their efficiency. The architecture namely color channel averaging method was proposed using reversible divider circuit, namely a multiplexer, a register, and a PIPO left shift register. The accuracy of functional block for conversion unit was tested by using FPGA using Verilog Hardware description language. It is seen the Quantum cost for color channel averaging method is 104% more than color space desaturation method.GC of color channel averaging is 92% more when compared to color desaturation method. Color space desaturation shows a 34% reduction in Slice LUT and dissipates 34:4% less power when compared to color channel averaging method. The method

was verified thoroughly and can be the starting blocks for image processing blocks using reversible logic. Based on the evaluation results, particularly the performance characteristics of the proposed designs, recommendations are proposed for further improvements to the reversible circuits that would cause better performance and reliability.

Future Scope

The proposed designs can be extended to any arithmetic unit and low power reversible multipliers and dividers. It points to the fact that the proposed circuits have the lesser garbage outputs, constant inputs, hardware complexity and they also have a minimum quantum cost to improve power dissipation than that of existing designs. The circuits in an energy efficient reversible logic design are cost effective when evaluated with respect to technology independent realizations. It establishes the fact that the reversible circuits and gates can be widely used to design low power VLSI design, quantum computers, large reversible systems and nanotechnology. In future work, we will describe the applications of the presented reversible universal blocks in QCA design. At present the proposed circuit works for positive integers. An interesting suggested future work could be to develop reversible divider for signed and floating point numbers.

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