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IMPLEMENTATION OF ADDER AND SUBTRACTOR USING PROM

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Abstract: A Look-Up Table (LUT) in the FPGA chip is the main subsystem in a configurable logic block. If the power management techniques are applied in the LUTs, when implementing the design in FPGAs, there would be a very low overall power. This research focuses mainly on the design of LUTs using PROM circuits. In order to incorporate these LUTs, half adder, full adder, half subtract and full subtractor circuits are selected with the PROM concept All standard CMOS and pseudo-nMOS type technologies are designed for LUTs. Compared to conventional CMOS approach, pseudo-nMOS focused LUTs provide less space and low power. An adder design based on pseudo-nMOS produces 564.5µm2 design area, which is less than 765.5µm2 generated by conventional CMOS full adder LUT. This study shows how the PROM in a FPGA architecture can function as a Look-Up Table Because engineers most carefully design circuits with circuit design, layout architecture, etc., Software defined Analog Circuits are the best to provide low power, high speed, and small size at the expense of design transfer time. But with the current consumption of semiconductor technology, even high-speed FPGAs with more flexible features are being produced. Use dynamic and domino logic forms, this work can be expanded further. FPGA interconnections will also be built to further reduce the total power dissipation.

Index Terms **- Look up table(LUT), Programmable read only memory(PROM), Metal oxide semiconductor(MOS),carbon metal oxide semiconductor, high speed FPG.**

I. INTRODUCTION

According to Moore's law, the number of transistors become double as soon as in eighteen months approximately.So the electricity dissipation in a machine will be massive and the reliability may also come down. So designers are still running towards higher designs so that you can eat less energy at the cost of performance or area [1]. A high priced cooling mechanism requirement is another cause for low energy designs. By modifying circuits in a device or sub-systems one mightalso gain low power dissipation. Same isn't always relevant to the batteries, for the reason that battery technology is not advanced as like semiconductor. Due to the explosive in nature, designers are always concentrating to layout novelcircuitsfor better results.[2,3].

FPGAs are the most widely utilized semiconductor processors in industry. ASICs are functioning well since engineers start designs from base by including all the design specifications such as power, speed and area. But, along with more expensive CAD tools, the design life cycle time is too high. FPGAs resolve these disadvantages and even improve the efficiency of the new trend in semiconductor technology [4,5]. This research focuses on implementing PROM with examples of the adder circuit. The designs adders / subtractor circuits are considered to be performed and tested. LUT can also be equipped with devices such as transmitting gates, transistors and multiplexers. The design uses pseudo-nMOS and traditional CMOS types [6]. A traditional CMOS which is a ratioless logic utilizes transistors in turn field. For better results, other types of CMOS logic style such as dynamic logic, domino logic, compatible jump-transistor and communication gate can also be used. for adders, it is also possible to implement a twin circuit principle to achieve equivalent rise and fall drop. This study explores the operation of the adder circuit using LUT model with a pseudo-nMOS logic type model [6,7].

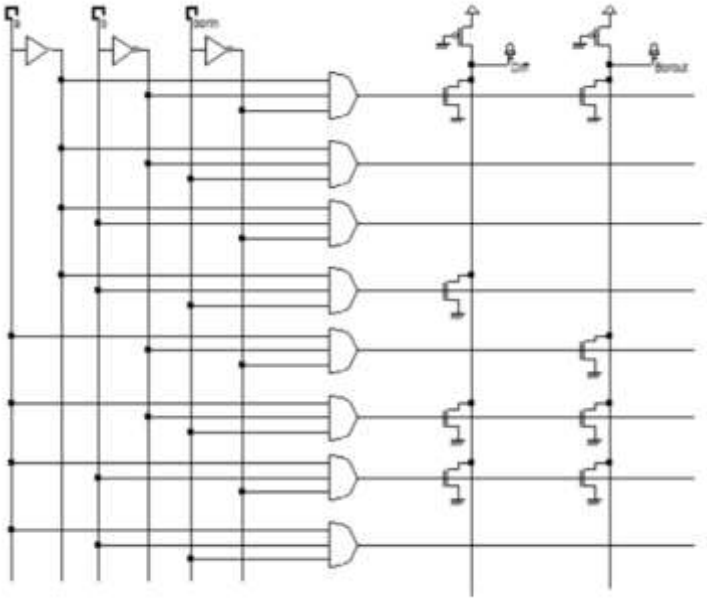
II. DESIGN OF SUBTRACTOR USING PROM

Similar to adders, half of and complete subtractor circuits are implemented using PROM concept10. Adders and subtractors play a important function in computing applications[6]. This sort of Filed-Effect Transistors (FET) programmable array are the maximum powerful in the issue of area. Due to the pseudo-nMOS good judgment, the wide variety of transistors are reduced almost half of count as compared to the traditional logic style[7,8].Psuedo nMOS logic style has the main benefit of having less range of transistors to carry out the required function

as compared with static CMOS fashion. For example, N input good judgment gate Requires 2N wide variety of transistors while in the pseudo-nMOS only N+1 transistors are required [9,10].

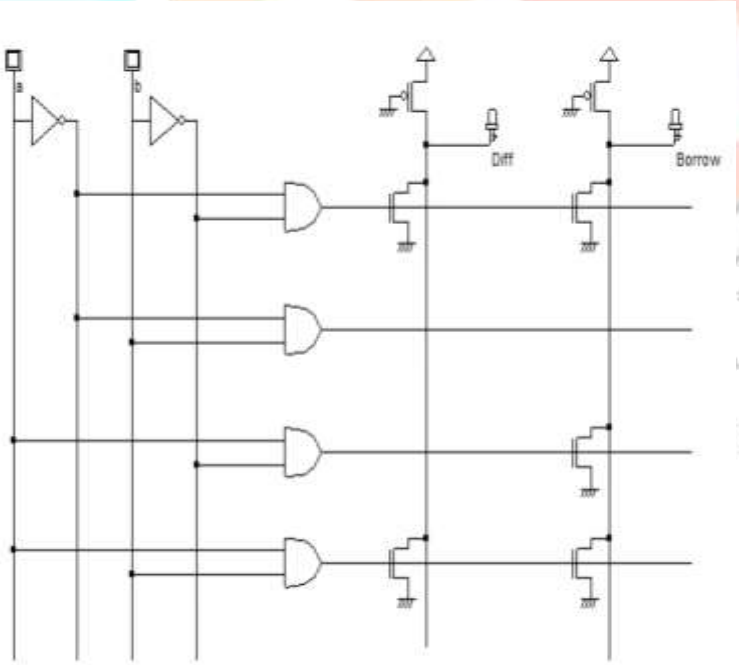
FULL SUBTRACTOR

Full subtractor consists of 3 inputs and 2 outputs called as difference and borrow. For designing full subtractor Using PROM first we need to know the design of full subtractor. The truth table, circuit diagram is as follows:



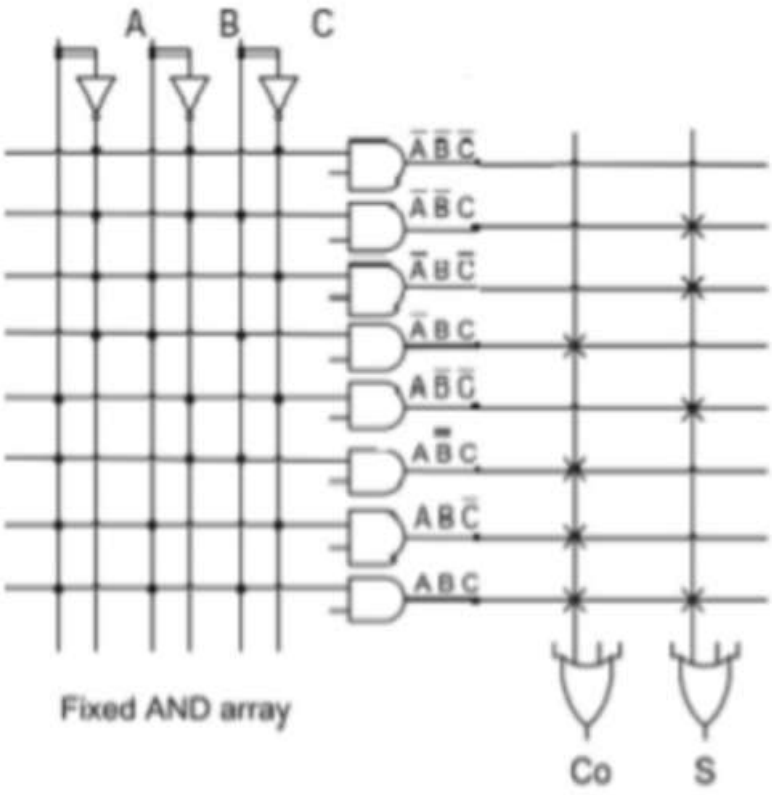
HALF SUBTRACTOR

Half subtractor consists of 2 inputs and 2 outputs called as difference and borrow. The truth table and circuit diagram of half subtractor is given below

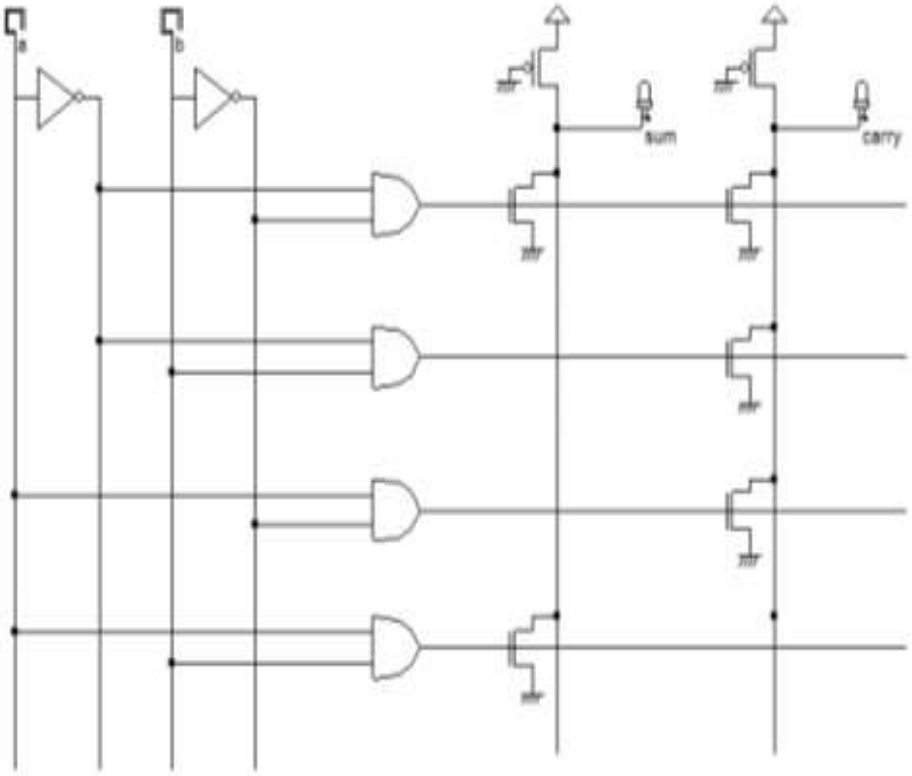


III. DESIGN OF ADDER USING PROM

Full adder has 3 inputs A,B,C and two outputs called sum and carry. The truth table for full adder is give below



Half Adder has 2 inputs and 2 outputs called sum and carry . The truth table and the circuit diagram as shown below



IV. LITERATURE REVIEW

Circuits and Systems addresses both procedure technology and tool modeling. Power dissipation in CMOS circuits, several sensible circuit examples, and low-strength techniques are discussed. Low-voltage issues for virtual CMOS and BiCMOS circuits are emphasized. The ebook also provides an in depth look at of superior CMOS subsystem layout. A low-energy design method is presented with various power minimization strategies on the circuit,logic, architecture and algorithm levels.[1].For both introductoryand superior publications in VLSI design, this authoritative, comprehensive textbook is tremendously reachable to beginners, yet gives unheard of breadth and intensity for more skilled readers. The Fourth Edition of CMOS VLSI Design: A Circuits and Systems perspective gives large and in-intensity coverage of the entire field of cutting-edge CMOS VLSI Design. The authors draw upon substantial enterprise and classroom enjoy to introduce todays most superior and powerful chip layout practices. They present extensively up to date coverage of every key element of VLSI layout, and light up the present day design challenges with 65 nm manner examples [2].Combined with person observe in related studies regions and participation in huge device design projects, this news letter provides the idea for a graduate course-collection in incorporated systems. MOS gadgets and circuits are considered in conjunction with integrated system fabrication, facts and manipulate waft in systematic structures, the implementation of included device designs, the evaluation of an LSI computer system, the design of the OM2 data direction chip, architecture and design of machine controllers, the design of the OM2 controller chip, system timing, incredibly concurrent systems, and the physics of computational systems[3].Newenergy economical ways of planning s witches and routing interconnects within FPGA mistreatment novel variants of Dynamic Threshold MOS (DTMOS) rather than ancient NMOS pass junction transistor primarily based switches and interconnects. the additional required transistors are often simply shared, in electronic device primarily based routing design of FPGA, keeping space overhead to be minimum. in depth junction transistor level HSPICEsimulation supported Berkeley prognosticative Technology Model (BPTM) for 65nm device at in operation frequency of 300MHz shows a median twenty three.35% improvement in power delay product (PDP) of straightforward switch (NMOS pass transistor) and a median thirty two.83% improvement within the PDP of Virtex-II FPGA routing interconnects over standard approaches. Since FPGA consists of thousands of electronic device primarily based routing interconnects, thus general improvement within the PDP is critical.[4]. Static and dynamic power dissipation in FPGAs is dominated by means of that fed on within the interconnection fabric, making low-energy interconnect a mandatory feature of future low-energy FPGAs. In this paper, we proposed new FPGA routing switch designs that can be programmed to operate in high-pace, low-electricity or sleep mode. Leakage in low-electricity mode is reduced via 36-40% vs. High-pace mode dynamic power is reduced via up to 28%. Sleep mode offers leakage discounts of 61%. An alternate version of transfer design offers leakage reductions of 28-30% in low electricity vs. High-speed mode, and has a 36% smaller area overhead. We confirmed that the timing slack in ordinary FPGA designs permits the bulk of switches to perform in low energy mode. The switch designs require simplest minor changesto a traditional FPGA routing switch and feature no impact on router complexity, making them clean to install in present day commercial FPGAs [5].

CONCLUSION

From this paper we can conclude that the adder & subtractor can also be implemented using prom logic. It helps a lot to improve the quality and the power consumption is very less when compared with the original adder circuit and subtractor circuit. These circuits are used in many devices. Mostly these circuits had used the CMOS for the better quality. From this we can analyse the working of subtractor and adder clearly.

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