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Comparison of various 3-bit DEM Structures using 130nm CMOS Technology

¹B.L.V.S.S. Aditya

(M. Tech),

Electronics and Communication Engineering,

MVGRCE(A),

Vizianagaram, Andhra Pradesh,

India.

²Mr. A. Ashok Kumar,

M. Tech, (Ph.D),

Electronics and Communication Engineering,

MVGRCE(A),

Vizianagaram, Andhra Pradesh,

India

Abstract: For their ability to have higher resolutions and operating speeds, current steering DACs (CSDAC) are most preferred to be used in mixed-signal designs. To improve the static and dynamic linearity in such DACs, compensation techniques such as dynamic element matching (DEM) were introduced, which can be achieved by random swapping of connections between the unary current sources of the DAC. DEM techniques mitigate the amplitude and timing mismatches in a DAC and improve its performance. Various DEM techniques such as GRTC, RRBS and Nested Segment were designed for 3-bit resolution in 130nm CMOS technology and their performances were compared. Due to its deterministic approach and the elimination of random counters, the nested segmented DEM technique provides a better performance compared to other DEM techniques. A reduction of 15.84% in delay and 21.126% in power can be observed in the nested segment structure, compared to GRTC and RRBS techniques respectively. The elimination of random number generators can also reduce the area required for the DEM implementation.

Keywords: DAC, CSDAC, DEM, GRTC, RRBS, CMOS

I. INTRODUCTION

The prominence of mixed-signal VLSI designs has increased in the recent times due to their ability to implement both analog and digital blocks on a single die. These designs are mostly used for consumer related and real time applications such as mobile phones. The analog and digital blocks in a mixed signal design have their own flows, which help in analyzing the entire block that defines the design. Due to well established and detailed abstraction, digital flows are preferred more than the analog.

1.1 Digital to Analog Converters (DACs):

DACs are electronic circuits that convert input digital signal into an electrical signal output. The inputs are accurately defined in terms of bits 0 and 1. The output is observed as a continuous signal i.e., a sequence of values. DACs can be used in various systems, including communication transmitters that are related to real time applications [7]. There are various types of DAC architectures such as the Resistor String, Resistor Ladder, Charge Division, Current Division and Current Steering DACs, out of which the CSDACs are most preferred for their higher speed of operations [2], [7].

II. CURRENT STEERING DACs

CSDAC architecture comprises of a current division network and a reference current replicator that combine the binary weighted currents and a Current-Voltage (I-V) converter to provide the desired analog output. Most of the CSDACs are used in direct digital synthesis, video applications and upstream cable transmissions [1], [3]. To improve the performance of these DACs, i.e., improving linearity and to minimize code dependent errors, compensation techniques can be used. Of all the available compensation techniques, dynamic element matching is most preferred for their ability to provide noise shaping, less hardware complexity and minimized mismatches.

2.1 Dynamic Element Matching (DEM):

Dynamic element matching is nothing but dynamically re-arranging the switching sequence of the unary DAC cells that are randomly selected using the switching mechanism [3], [4]. The output is obtained by adding the currents from the least binary weighted sources. Conventional DEM based DACs provide higher linearity at lower resolutions only. To overcome this drawback and to achieve higher linearity at higher resolutions, other DEM techniques such as Segmented DEMs were introduced. In this technique, the unary sources

in a DAC are grouped into several segments such as LSB, ULSB and MSB and are controlled using individual DEM blocks. The remaining LSB units are designed using binary weighted current sources and are directly controlled by digital inputs. These DEMs have less complex architecture and provide easier switching between the cells, resulting in less mismatch.

DEM techniques are generally classified into Stochastic and Deterministic [3], based on the approach of their matching. Stochastic DEMs select the unary current sources by generating a control sequence randomly. Deterministic DEMs generate the control signal using a rotary fashion. Based on these approaches, three DEM techniques – Grouped Random-rotation Thermometer Code (GRTC) [5], Random Rotation based Binary-weighted Scheme (RRBS) [6] and Nested Segment [1] were taken under consideration and their performance characteristics were compared. Of these techniques, GRTC and RRBS fall under the stochastic approach while the Nested Segment structure is a deterministic approach.

III. DEM ARCHITECTURES

3.1 Grouped Random-rotation Thermometer Code (GRTC) DEM:

GRTC performs DEM by rotating each sequence of the unit current source array randomly. The randomness of the GRTC depends on the type of pseudo-random number generator (PRNG). The GRTC circuit consists of multiplexers for bit rotation and a PRNG for providing control to the multiplexer (**Fig-1**). It suppresses harmonics caused by element mismatches and distortion tones. The circuit is less complex and has better performance in speed and power consumption. [5]

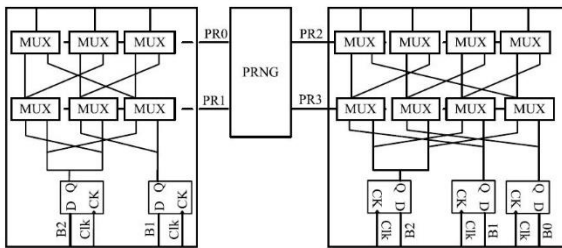


Figure-1: GRTC DEM Block Diagram

3.2 Random Rotation based Binary-weighted Scheme (RRBS) DEM:

A Random-rotation based Binary weighted Scheme rotates the sequence of current sources randomly to form new current cell groups. Unlike conventional binary weighted DACs, RRBS DEM based DACs are insensitive to mismatches. The design comprises of a 3-bit rotator and 3 random number generators that drive the rotator through some logic gates (**Fig-2**). It doesn't require any binary-thermometer decoders. Timing skews between current sources can be minimized as the mismatches between parasitic components will be smaller in RRBS. It can achieve higher resolution and speed simultaneously. [6]

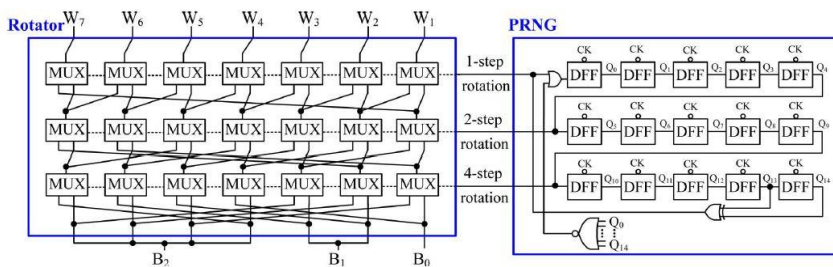


Figure-2: RRBS DEM Block Diagram

3.3 Nested Segment DEM:

The nested segmented DEM is divided into 3 parts i.e., LSB, ULSB and MSB segments corresponding to l, u, m-bits respectively. The MSB segment of m-bits has a sub array consisting of 2^m blocks. Each MSB sub-array contains 2^u ULSB sub-arrays which in turn consist of 2^l LSB sub-array blocks. In total, the nested segmented DEM consists of (2^l-1) unary current sources and l-bit binary weighted current sources. The nested segmented DEM technique mainly consists of 3-blocks Control Signal Rotator, Bit Signal Rotator and Delay Equalizer. [1]

3.3.1 Control Signal Rotator:

The control signal rotator is excited by a pre-determined control input which is shifted through the multiplexer blocks to provide a control output. The output signal determines the MSB array to be chosen among the DAC architecture.

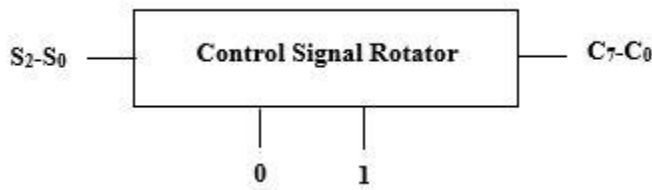


Figure-3: Control Signal Rotator Block

3.3.2 Bit Signal Rotator:

The bit rotator employs a multi-level right shifting technique. A barrel shift operation is carried out by the multiplexers that are excited by their specific control signal.

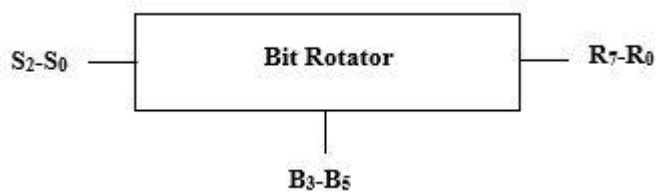


Figure-4: Bit Signal Rotator Block

3.3.3 Delay Equalizer:

The delay equalizer is a digital block that compensates the delay introduced by the bit signal rotator. Delay is introduced in the initial bits by using inverters as delay blocks.

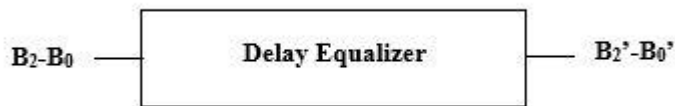


Figure-5: Delay Equalizer Block

Apart from these blocks, a switch driver can also be used to take the input from the DEM blocks and drive it to the current sources to run the DAC and provide the desired output. All these blocks combine together to form a nested segmented DEM block that has various advantages over conventional DEMs such as availability of more MSB array without area penalty and improved dynamic performance.

IV. SIMULATION RESULTS AND COMPARISON

In this section, three DEM techniques of 3-bit resolution were compared for their delay and power measurements, in CMOS 130nm technology. The RRBS DEM provides a high speed of operation but with more power consumption while the GRTC DEM consumes less power but more delay.

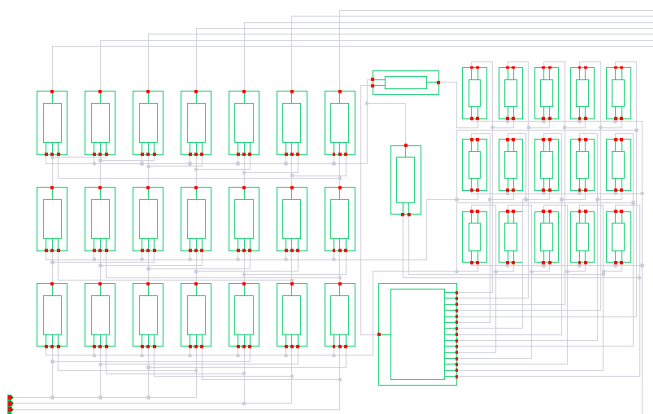


Figure-6: RRBS DEM Circuit

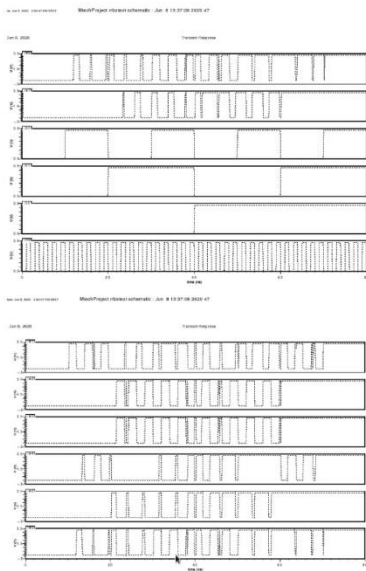


Figure-7 RRBS DEM Waveforms

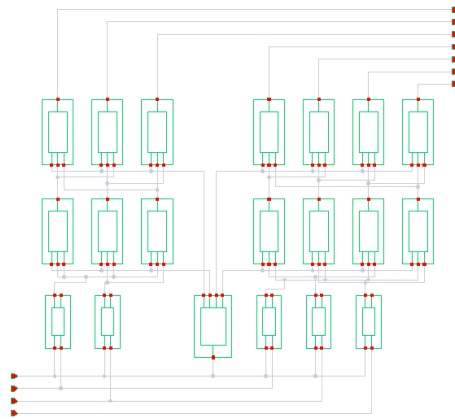


Figure-8: GRTC DEM Circuit

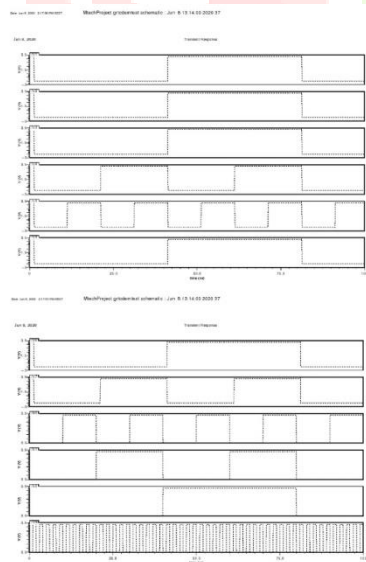


Figure-9: GRTC DEM Waveforms

Compared to both the techniques, the nested segment provides moderate performance in both power and delay measurements as shown in **Table-1**. The delay is reduced by 15.84% compared to the GRTC and the power consumption is reduced by 21.126% compared to the RRBS. Along with these improvements, the usage of the PRNGs in GRTC and RRBS DEMs would result in higher area occupancy when the blocks are sent for fabrication. To overcome this, the nested segment structure with better power and speed of operations along with its deterministic approach is chosen.

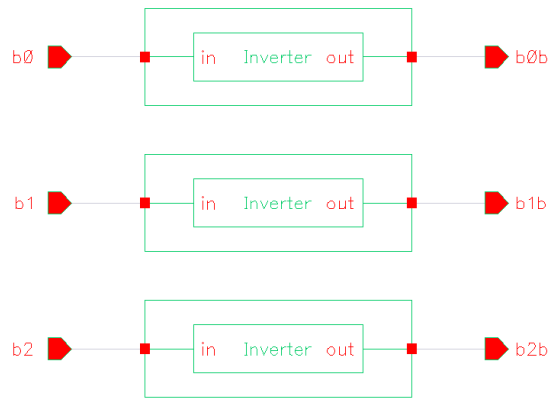


Figure-10: Delay Equalizer Circuit

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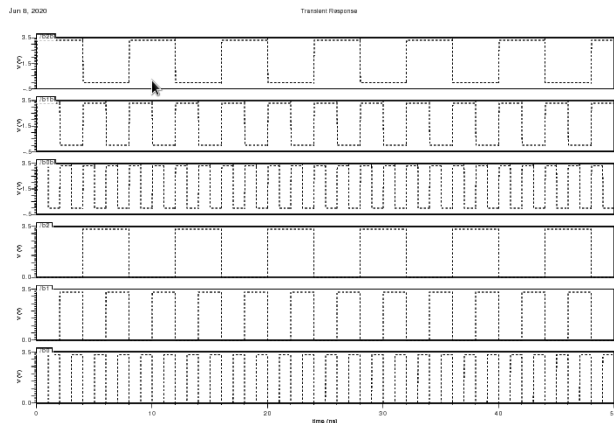


Figure-11: Delay Equalizer Waveforms

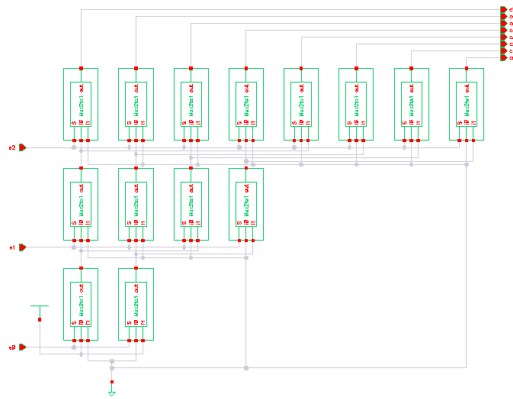
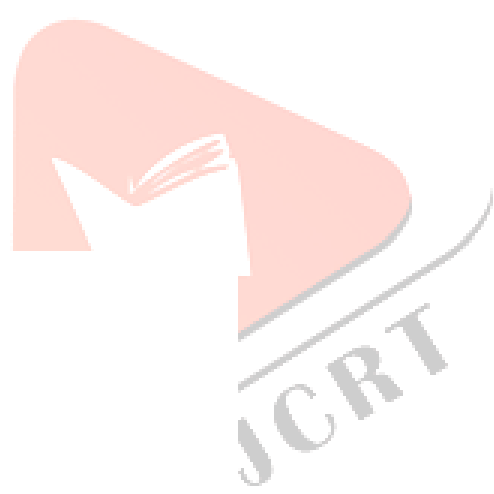


Figure-12: Control Signal Rotator Circuit



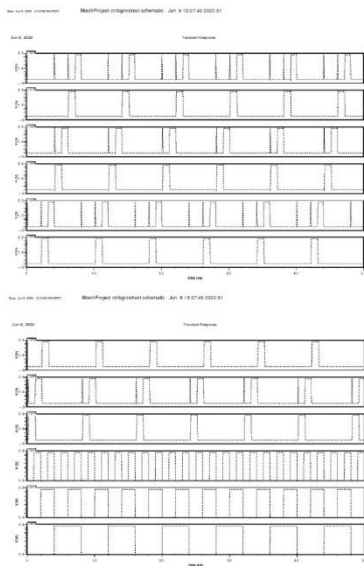


Figure-13: Control Signal Rotator Waveforms

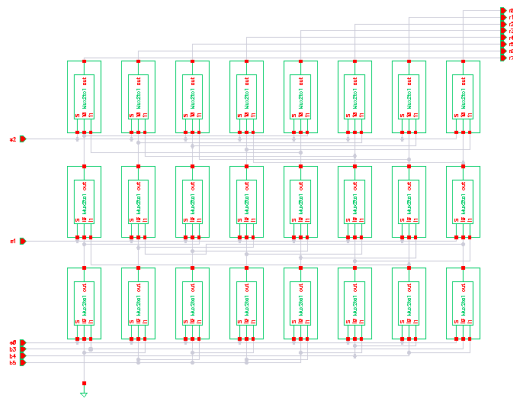


Figure-14: Bit Rotator Circuit

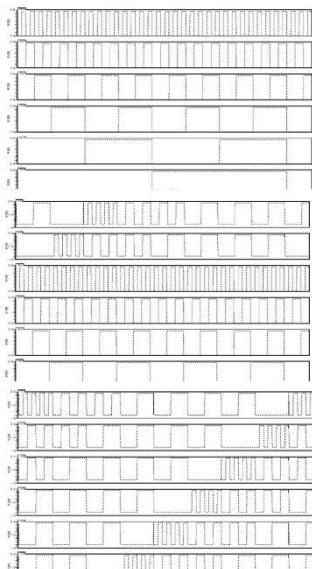


Figure-15: Bit Rotator Waveforms

Table-1: Comparison of Power and Delay Parameters for various 3-bit DEM blocks:

Technique	RRBS	GRTC	Nested Segment		
			Control Signal	Bit Signal	Delay Equalizer
Delay	-197.9×10^{-12}	-1.207×10^{-9}	-191.2×10^{-12}	-180.7×10^{-12}	-5.839×10^{-12}
Avg. Power	4.314×10^{-3}	403.5×10^{-6}	911.4×10^{-6}	1.029×10^{-3}	18.27×10^{-6}

V. CONCLUSION

In this paper, various DEM techniques were designed in 130nm CMOS technology using Cadence Tool and their performances were compared. Due to its high speed of operation and deterministic approach, Nested segment structure was considered most prominent. The nested segment structure can be extended to higher bits to allow the implementation of higher resolution CSDACs with more MSB area possibility. Along with this, to overcome the extinction of the Moore's Law, these DEM blocks can be implemented in other FET technologies such as CNFETs and GNRNFTs to improve the speed of operation and power consumption.

VI. REFERENCES

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