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A Study of Neutral Point Voltage and Common Mode Voltage Control in Multilevel SPWM Technique

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Abstract: Conventional 2-level PWM inverters generate high dv/dt and high frequency common mode voltages which is very harmful in electric drives applications. It may damage motor bearings, conducted electromagnetic interferences, and malfunctioning of electronic equipments. Due to capacitor voltage unbalancing, neutral point potential also varies from zero. This paper presents a simple method to control the harmonics, common mode voltages and neutral point potential variation in neutral point clamped (NPC) inverters using different structures of sine-triangle comparison method such as Phase Disposition (PD), Phase Opposition Disposition (POD), and Common Mode Voltage off-set voltage addition method. Simulation results confirm the effectiveness of these simple methods to control common mode voltages. Neutral point potential variation is limited to less than 2% of dc capacitor voltage using a simple closed loop PI regulator.

Index Terms **- Common Mode Voltage, Harmonics, Multilevel Inverter, Neutral Point Potential Control, Diode Clamped Multilevel Inverter.**

I. INTRODUCTION

Recently, multilevel inverters have been found wide spread acceptability in medium and high voltage applications. Multilevel inverters have the advantage of producing high voltage high power with improved power quality of the supply. It also eliminates the use of problematic series-parallel connections of switching devices. However, multilevel PWM inverters generate common mode voltages as in the case of conventional 2-level inverters. The problem of common mode voltage generation in multilevel inverters has been studied extensively during last decade [1-5]. Common mode voltages are generated due to shaft voltages, circulating leakage currents through parasitic capacitance between motor windings, rotor and frame. The number of current spikes and magnitude of common mode voltage is determined by dv/dt and number of commutations. Several methods have been suggested for solving this problem. Some methods are based on additional circuit like filters. Other methods use advanced modulation strategies avoiding the generation of common mode voltages. But, these methods work at higher switching frequency, thus increasing the losses [1]-[3]. Various multilevel inverter control techniques, using sine-triangle comparison, for harmonic reduction have been reviewed in [4]. But the issue of common mode voltage control was not covered. Opportunities of harmonic reduction in cascaded multilevel inverters were investigated in [5-6] using carrier based PWM techniques. Conventional multilevel SPWM techniques generate a significant amount of common mode voltage which may be around the dc voltage level.

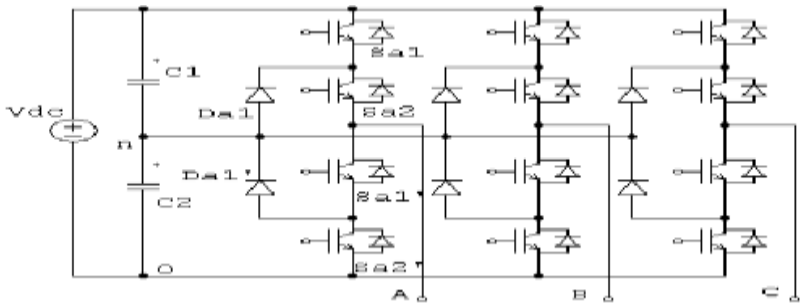

Fig. 1. Structure of 3-phase, 3-level diode clamped inverter.

Another problem which NPC inverter faces is neutral point potential (NPP) variation due to voltage unbalancing between two capacitors. Due to the variation in NPP, excessive high voltages may be applied across switching devices. Several methods have been investigated to control the NPP variation and neutral point current [7-10]. A neutral point voltage regulator has been modeled and designed in [10]. But it works at 5 kHz switching frequency resulting in high switching losses. In this paper, a NPP regulator is presented which works at low switching frequency of 2 kHz. This paper also investigates the possibilities of using different multilevel SPWM techniques such as Phase Disposition (PD), Phase Opposition Disposition (POD) and Common Off-set voltage addition method (Bias method) to reduce the common mode voltages in 3-level diode clamped inverter. Results show drastic reduction in THD using modified SPWM methods. At the

same time common mode voltages are also controlled up to nearly half of the magnitude as compared to conventional multilevel SPWM methods.

II. OPERATION OF 3-LEVEL SPWM

Fig. 1 shows the very popular topological structure of diode clamped 3-phase, 3-level inverter considered here for study. The switching states of the inverter are shown in Table I for one leg. It gives the output pole voltage $V_{AO,}$ output line voltage V_{AB} and switch state. Switch state '1' means 'on' and '0' means 'off'. This switching pattern can be achieved by means of different multilevel control strategies such as square wave switching, sine-triangle comparison method (SPWM), space vector modulation (SVM), selective harmonic elimination technique, hysteresis current control, sigma-delta modulation etc. Of these methods, sinusoidal pulse width modulation (SPWM) is the simple and cost effective method to implement, therefore considered here.

TABLE I
Switching states of 3-level diode clamped inverter

V_{AB}	Output Pole Voltage (V_{AO})	Switch States			
		Sa1	Sa2	Sa1	Sa2
$-V_{dc}/2$	0	0	0	1	1
0	$V_{dc}/2$	0	1	1	0
$V_{dc}/2$	Vdc	1	1	0	0

SPWM technique is again subdivided into following categories:

- Phase Disposition (PD) method,
- Phase Opposition Disposition (POD) method,
- Phase Shifted (PS) method,
- Hybrid method,
- Third Harmonic Injection (THI) method.

Basic principles of pulse generation for 3-level PD and POD SPWM techniques are shown in Fig. 2 and 3. Fundamental frequency three-phase sinusoidal reference waves v_r, v_y and v_b are compared with two high frequency triangular carrier waves 'carrier 1' and 'carrier 2'. Each intersection gives rise to the control pulses for switching devices of inverter. The reference sinusoidal waves can be represented by,

$$v_r = V_m \sin(\omega t)$$
$$v_y = V_m \sin(\omega t - 120^0) \quad (1)$$
$$v_b = V_m \sin(\omega t - 240^0)$$

PD and POD SPWM techniques have been selected for study without and with addition of common mode voltage off-set as shown in Fig. 2 to Fig. 5. Common mode voltage or zero sequence voltage in output voltage of inverter can be represented by,

$$V_{cm} = (v_r+v_y+v_b)/3 \quad (2)$$

Where, v_r, v_y and v_b are the phase voltages of inverter. This voltage is around 150-200 volts (peak) in conventional 2-level inverters for a dc voltage of 200 volts. To reduce it, following common mode off-set voltage is to be added,

$$V_{offset} = -[\min(v_r, v_y, v_b) + \max(v_r, v_y, v_b)]/2 \quad (3)$$

Therefore the new reference or modulation wave becomes,

$$V^* = v(r, y, b) + V_{offset} \quad (4)$$

Where, v(r, y, b) is given by equation (1). Fig. 4 and Fig. 5 give the reference 3-phase waves as obtained from equation (4). The 'max', 'min', one phase voltage v_r and off-set voltage signals, as obtained from equation (3) and (4), are shown in Fig. 6 for PD SPWM case.

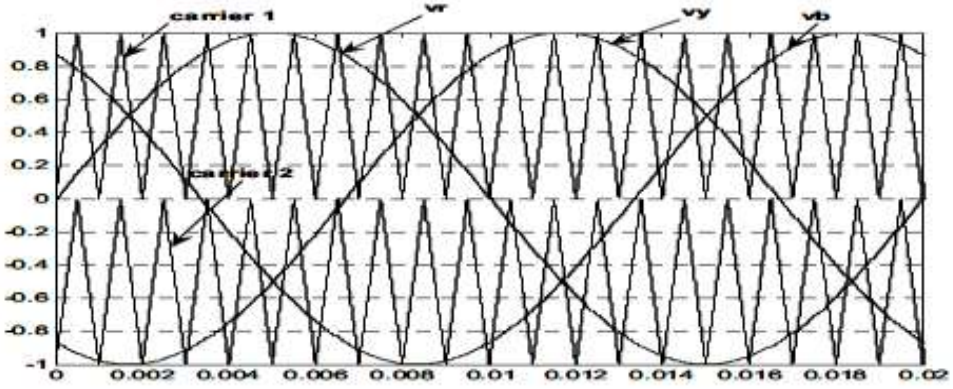

Fig. 2. Modulation and carrier waveforms with PD SPWM technique.

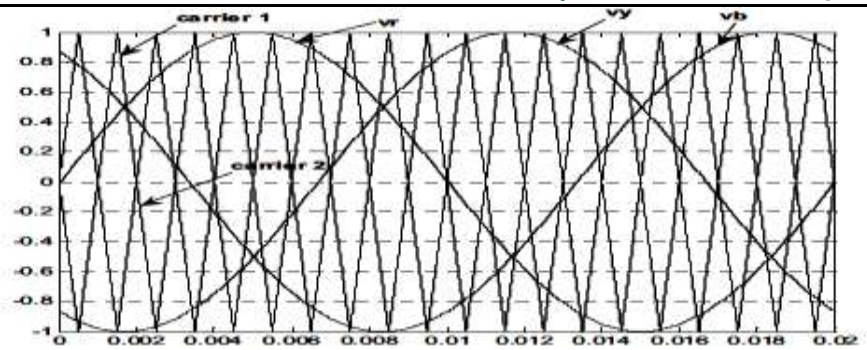

Fig. 3. Modulation and carrier waveforms with POD SPWM technique.

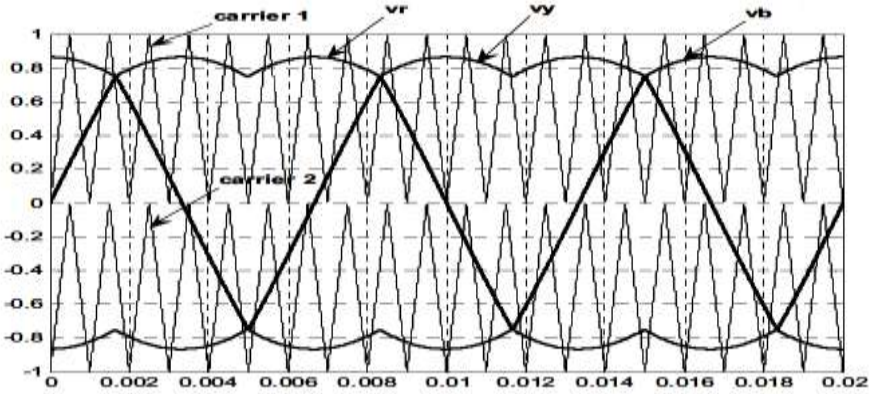

Fig. 4. Modulation and carrier waveforms with addition of common mode off-set voltage in PD SPWM technique.

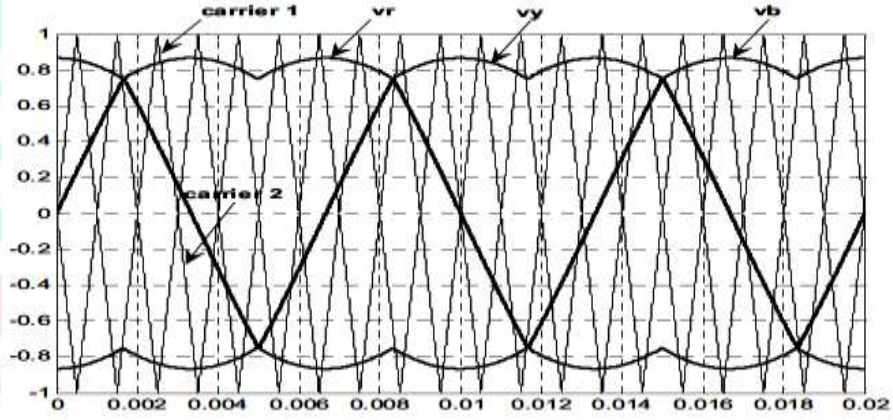

Fig. 5. Modulation and carrier waveforms with addition of common mode off-set voltage in POD SPWM technique.

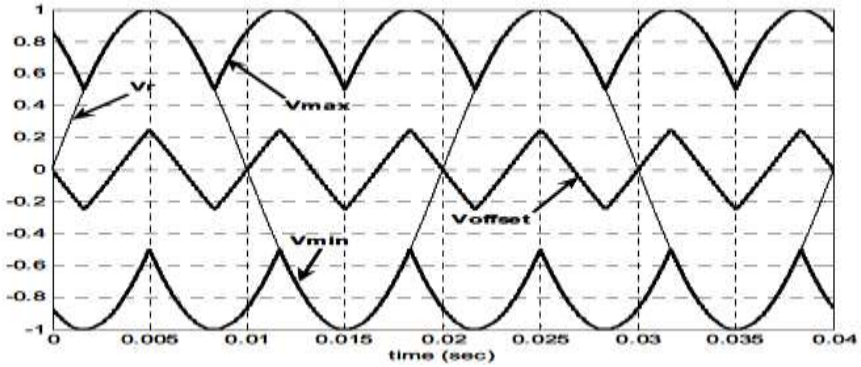

Fig. 6. Signals ‘Vmax’, ‘Vmin’, ‘v_r’ and off-set voltage ‘Voffset’ in PD SPWM technique with addition of offset voltage to the reference signals.

III. DESIGN OF NEUTRAL POINT POTENTIAL REGULATOR

Fig. 7 shows the closed loop scheme of proportional-integral (PI) neutral point potential (NPP) regulator.

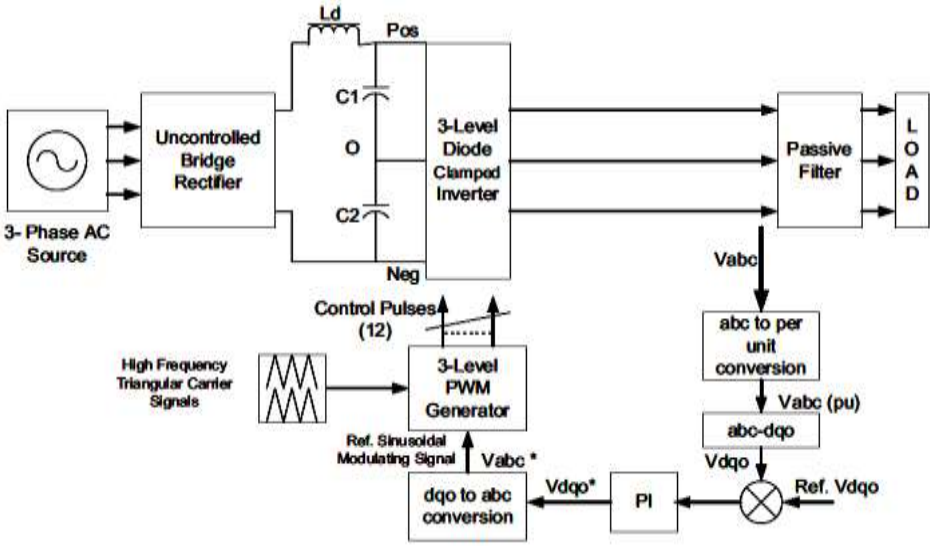

Fig. 7. Block diagram of closed loop voltage regulator.

The proposed PI voltage regulator aims to stabilize the dc link voltage to control neutral point potential variation by controlling the charging and discharging of upper and lower dc bus capacitors without dc capacitor voltage sensing. Three phase inverter output voltages are sensed and converted into per unit system. These per unit voltages are converted into dqo axis using following 3-phase to two-phase conversion,

$V_d = 2/3\ [V_a \sin(\omega t) + V_b \sin(\omega t - 120^0) + V_c \sin(\omega t - 240^0)]$,

$V_q = 2/3\ [V_a \cos(\omega t) + V_b \cos(\omega t - 120^0) + V_c \cos(\omega t - 240^0)]$,

$V_o = (V_a + V_b + V_c)/3$ (5)

These dqo voltages, V_{dqo}, are compared with set values of dqo voltages $V_{dqo}{}^*$. It results in voltage error which is processed through a proportional-integral (PI) controller to generate two axis command signals V_{dq}. Then three phase reference voltage signal for PWM generator is synthesized using following two-to-three phase conversion,

$V_a = [V_d \sin(\omega t) + V_q \cos(\omega t) + V_o]$,

$V_b = [V_d \sin(\omega t - 120^0) + V_q \cos(\omega t - 120^0) + V_o]$,

$V_c = [V_d \sin(\omega t - 240^0) + V_q \cos(\omega t - 240^0) + V_o]$, (6)

$m = \text{sqrt}(V_{d2} + V_{q2})$ (7)

and the gain of PI controller is,

$G = K_p + [K_i * T_s/(Z-1)]$ (8)

Values of K_p, K_i and limits of integration are tuned to achieve fast response of modulation index and to reduce NPP variation below 2%. Output of 3-level PWM generator block is the 3- phase sinusoidal reference signals to be applied to the PD SPWM scheme as discussed in previous section.

IV. SIMULATION RESULTS

A simulation model has been developed in Matlab environment. Fig. 8 and Fig. 9, show the waveforms and harmonic spectrum of line voltage with PD SPWM without and with filter. It is observed that fundamental voltage is increased from 173.2 volts to 181.2 volts with reduction in % THD from 29.34% to 2.00%. Switching frequency used is 1 kHz. Table II gives the % THD and fundamental value of line voltage (V_{1ab}) and current (i_{1a}) without and with filter. From this table, it is clear that the fundamental voltage increases with filter and maintaining the low THD.

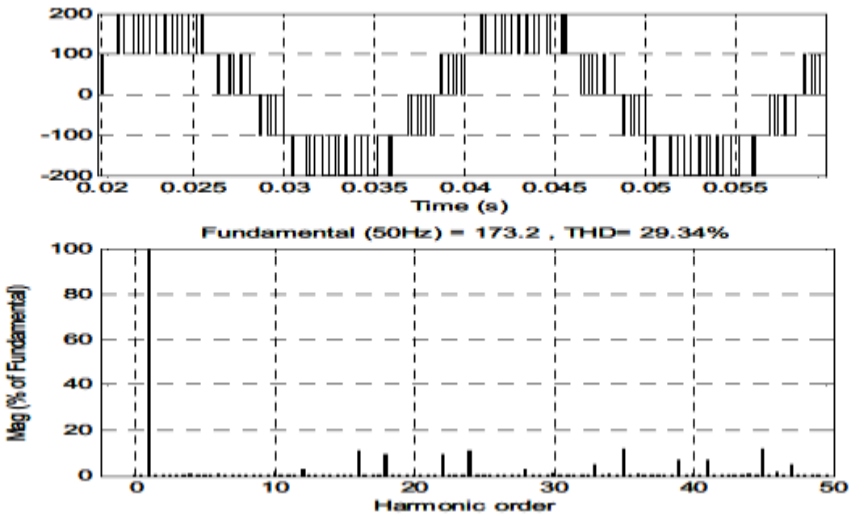

Fig. 8. Line voltage and its harmonic spectrum with PD SPWM.

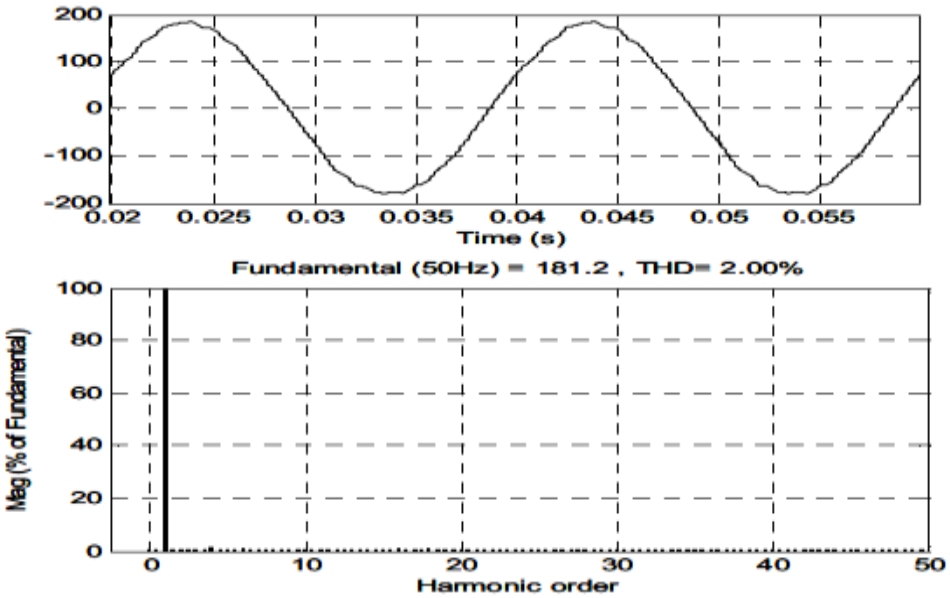

Fig. 9. Line voltage and its harmonic spectrum in PD SPWM with filter.

Fig. 10 gives the common mode voltages with normal and modified PD and POD SPWM techniques. It is clear from the Fig.10 that peak of the common mode voltage (V_{cm}) is less sharp in the case of Fig. 10(c) and amplitude is reduced from around 60 volts in PD SPWM to around 34 volts in POD SPWM. Also frequency of V_{cm} is reduced in Fig. 10(d) as compared to its counterpart in Fig. 10(b). Therefore, PODSPWM technique will be advantageous in view of the common mode voltage amplitude and frequency stress on motor windings.

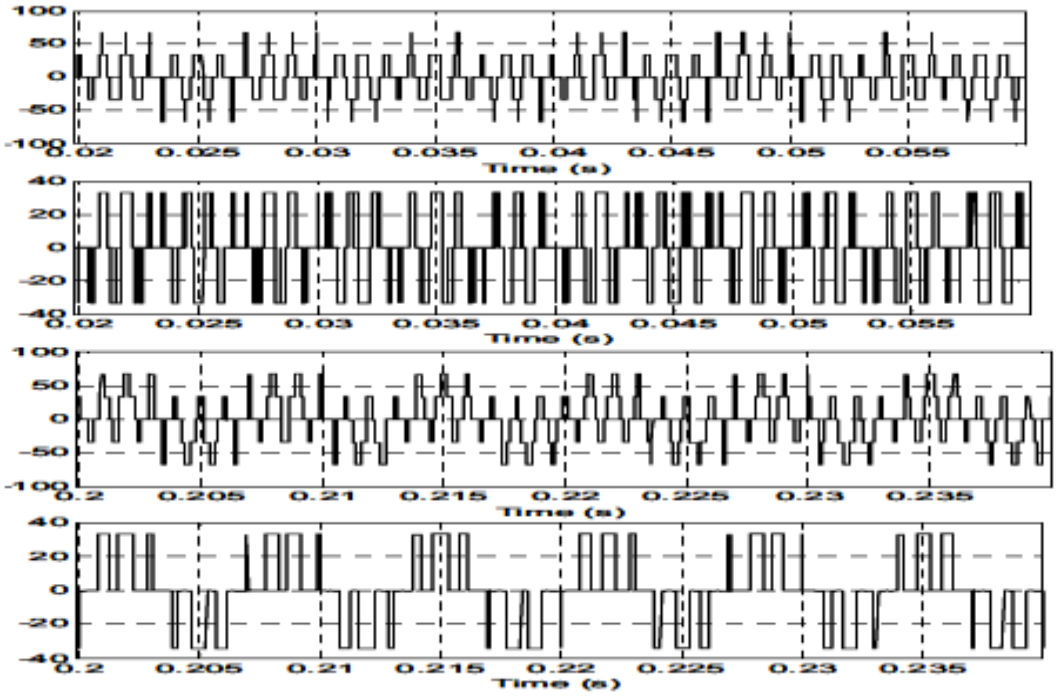

Fig. 10. Common mode voltages with (a) PD, (b) POD, and (c) common mode voltage PD and (d) common mode voltage POD SPWM techniques.

Fig. 11-15 shows, the results of closed loop control of inverter voltages and neutral point potential control with PI regulator. Upper and lower dc link voltage and neutral point potential is shown in Fig. 11 Average dc bus voltage across capacitors is 268 volts with % THD of 0.76.

The variation in NPP was observed at 1.4 % of dc bus voltage across one capacitor.

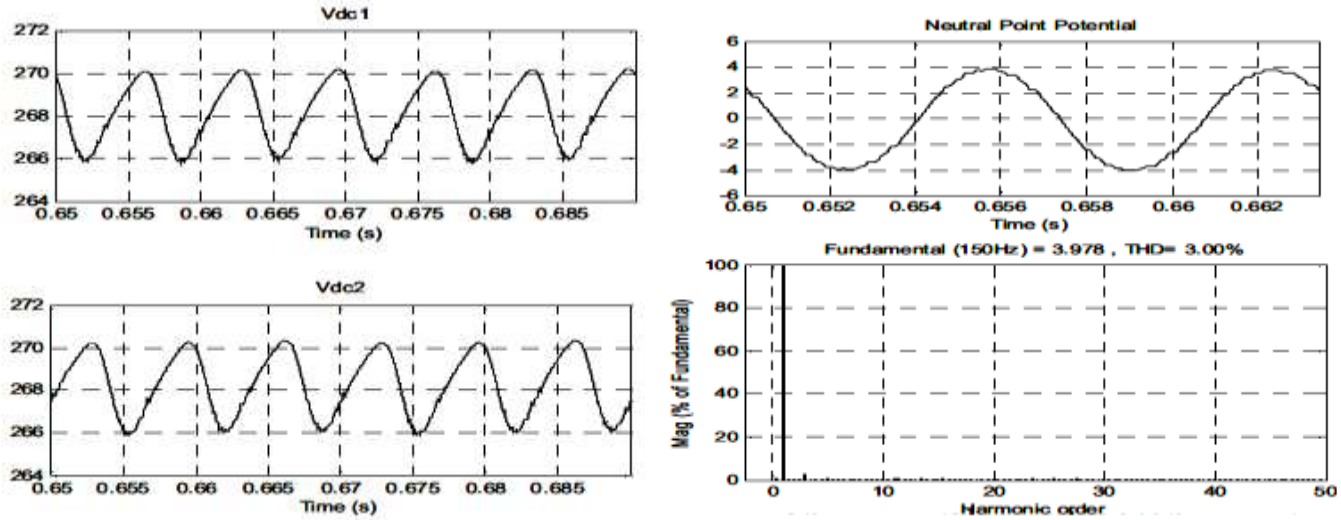

Fig. 11. Voltages across capacitors, V H dc1, Vdc2 and neutral point potential with its frequency spectrum.

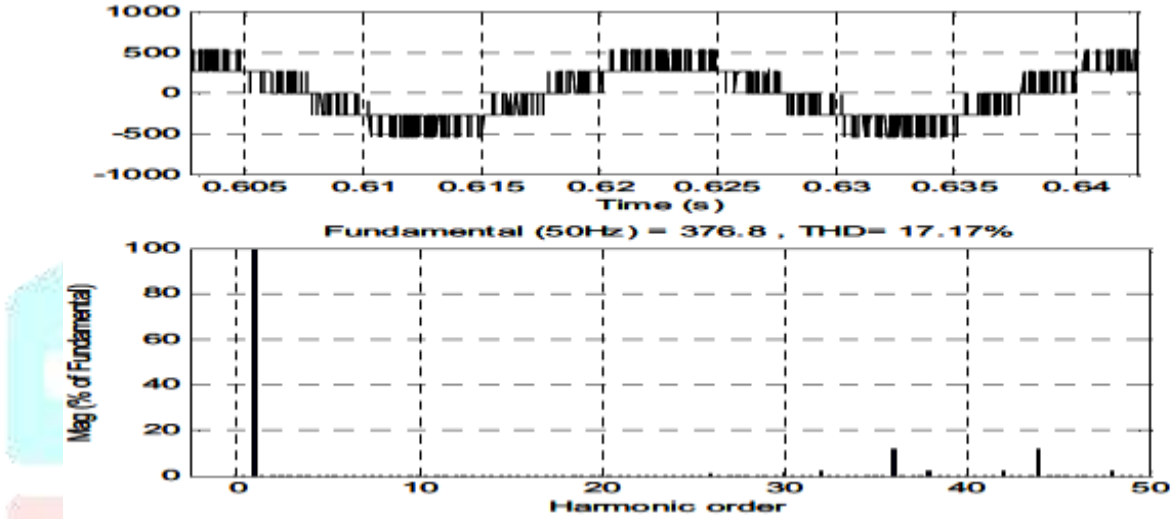

Fig. 12. Inverter output voltage, V_{ab}, and its harmonic spectrum at 2 kHz switching frequency.

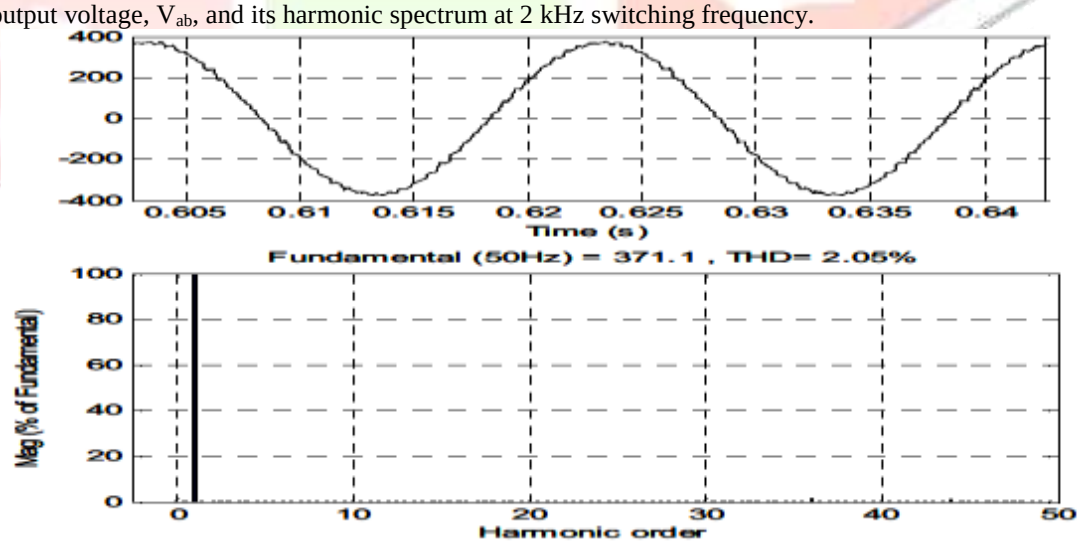

Fig. 13. Load voltage and its harmonic spectrum at 2 kHz switching frequency.

Inverter output voltage its harmonic spectrum for two cycles is shown in Fig. 12. Voltage across load is shown in Fig. 13. It is observed that % THD in voltage is reduced from 17.17 to 2.05 when using LC passive filter with 2mH inductance and 2kVar capacitive reactive power. Inverter line currents without and with filter are shown in Fig. 14 and Fig.15 Current THD also reduces from 12.20 % to 1.27 % using suitable passive filter.

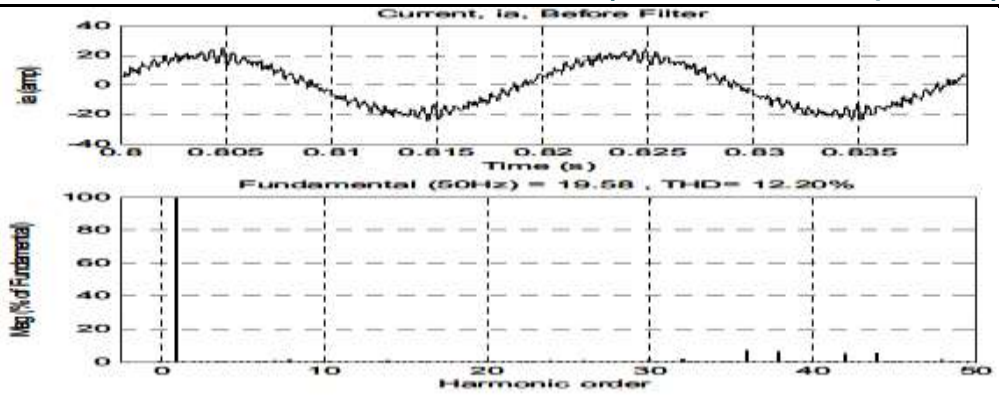

Fig. 14. Inverter output current and its harmonic spectrum at 2 kHz switching frequency.

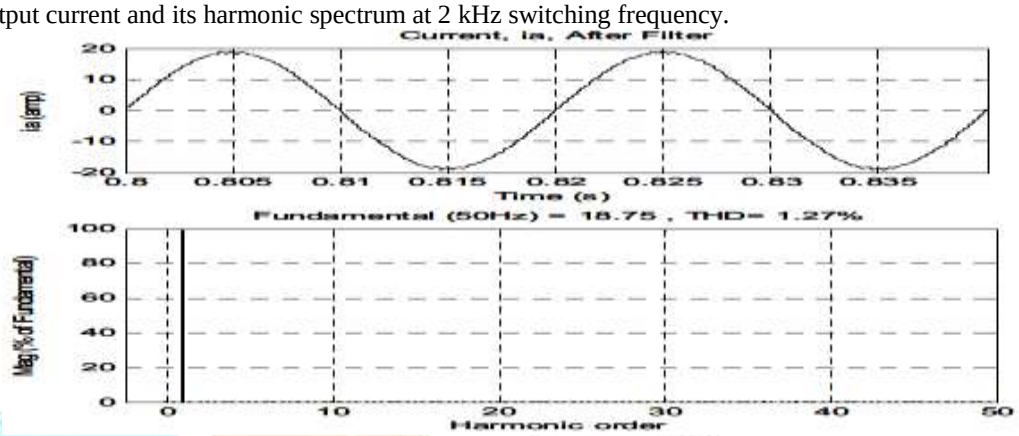

Fig. 15. Filtered inverter output current and its harmonic spectrum at 2 kHz switching frequency.

V. CONCLUSION

Common mode voltage generated in PWM inverter output may damage the motor windings, shaft, and bearings. Although, some methods have been developed for completely eliminating common mode voltages (with space vector PWM techniques) which is very complex to implement, it may be possible control it via simple SPWM techniques and their modified forms such as addition of common mode voltage off- set to the actual reference voltage wave as presented in this paper. Simulation results show that modified SPWM technique not only controls the THD in output voltage of inverter but also reduces the amplitude, switching transients and frequency of common mode voltages. Simple closed loop PI voltage regulator has been proposed to control neutral point potential without sensing dc capacitor voltages.

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