SINGLE-PHASE FIVE-LEVEL SYMMETRICAL CASCADED H-BRIDGE MULTILEVEL INVERTER WITH REDUCES NUMBER OF SWITCHES.

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Abstract-**Multilevel inverter with a reduced number of switches. A multi-level inverter is one kind of effective and practical solution to the increasing power demand and reducing harmonics of ac waveforms. This multilevel inverter requires eight switches to achieve the multilevel output. By reducing switches and increasing levels will reduce filter costs, harmonic content, reducing switching losses and costs.**
Keywords – Cascaded multilevel inverter; SPWM; APOD; PD; POD; THD.

I.Introduction

Basically, inverter is electrical devices that convert direct current (dc) input voltage to a symmetrical alternating current (ac) output voltage of desired magnitude and frequency. The output voltage could be fixed or variable at a fixed or variable frequency.

The waveform of a practical inverter is non-sinusoidal and contains few harmonic. Limitations for this inverter is Low efficiency, high cost and high switching losses. To overcome these Defects are called multilevel inverters introduce.

A multilevel inverter is a power electronic device capable of delivering the desired alternating voltage level at the output using several lower level DC voltages as input. This multilevel inverter works just like the inverter, but on high power applications. This multilevel inverter is an electrical device capable of producing Different voltage levels. The term multilevel inverter starts with three Level converter. In past years multilevel inverters are used in high power and high voltage applications. Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform.

A variable output voltage can be obtained by isolating the input DC Maintaining inverter and AC output ratio Voltage to DC input voltage) constant. Conversely, if the dc input voltage is fixed and not controllable, The gain of a variable output voltage can be obtained by

varying Inverter which is usually with pulse width modulator Within the inverter. Commutation of the switch allows the capacitor voltage to be connected, which Reach higher voltages at the output, while power semiconductors must withstand Only the reduced voltage. However, if the number of levels is Increases, the greater the number of components required, this results in Reduction in overall reliability and efficiency of the power converter. On the other hand, solution with a low number of levels either need a rather large and expensive LC filter to limit the motor winding insulation stress or can only be used with motors that do withstand such stress.

There are several topologies of multilevel inverters available. The difference lies in the mechanism of switching and the source of input voltage to the multilevel inverters. Three most commonly used multilevel inverter topologies are Cascaded H-bridge multilevel inverters Diode Clamped multilevel inverters Flying Capacitor multilevel inverters Among These three, Cascade H-bridges multilevel have a modular structure and Requires fewer components than diode clamped And flying capacitor multilevel inverter, and consequently, it is Widely used for many applications

All researches work that has gone on inverter circuit configuration mainly in reducing the switches at higher voltage levels, by reducing switches and increasing voltage levels will reduce filter cost and harmonic content. Five-levels CHB MLI topology required Ten switches and two separate dc sources, but to reduce switching loss and cost, Eight switches required in which the same MLI output voltage is obtained. These CHB MLI with eight switches and two sources will improve output waveform and reduce total harmonic distortion.

The circuit diagram of Cascaded H-bridge Multilevel inverter with eight switches and two separate dc sources and its switching states is shown below Table 1. The core aim of this topology is to reduce number of switches. This 5-level inverter carries eight switches in two legs, and four switches in each leg.

The switches are named as S1, S2, S3, S4, S5, S6, S7 and S8. S1, S2, S3, S4 are placed in first leg and S5, S6, S7, S8 are placed in second leg.

Switching Schemes with Operations

• For +200, switch S1, S4, S5 and S8 are switched ON for getting maximum voltage.

• For +100, switch S1, S2 , S5, and S8 are switched ON for next priority level of voltage.

• For zero output voltage, switches no switches are in ON state.

• For negative (-100) voltage switch S1, S2 ,S6 and S7 are switched ON.

• For negative (-200) voltage, switch S2, S3, S6 and S7 are switched ON.

Simulation Results

In this paper MATLAB,is used. In MATLAB the five level inverter circuit is simulated and results of output voltage and THD. The GUI plots are used for the Fast Fourier Transforms (FFT) analysis to determine the Total Harmonic content (THD). The simulation of 5-level is carried out in MATLAB SIMILINK.MOSFET are used in this design which has high voltage and current carrying

capability. A gate driver circuit is to be used for boosting the pulses from a microcontroller PIC16F877A and is used for generating required pulses.

Note: 1 indicates that switch is ON state, 0 indicates that switch is OFF state.

Five Level Cascaded H-Bridge Inverter Switching Table

Level	S1	S2	S3	S4	S5	S6	S7	S8
200	1	0	0	1	1	0	0	1
100	1	1	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
-100	1	1	0	0	0	1	1	0
-200	0	1	1	0	0	1	1	0
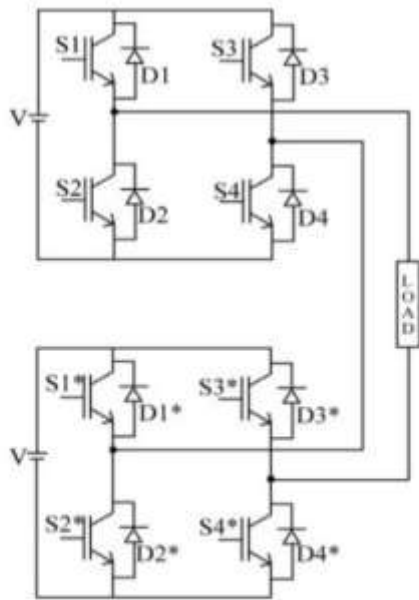
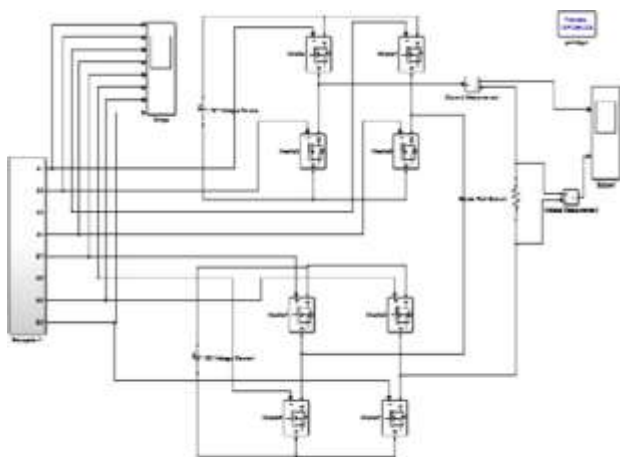Figure 1. 5-level Cascaded multilevel inverter circuit

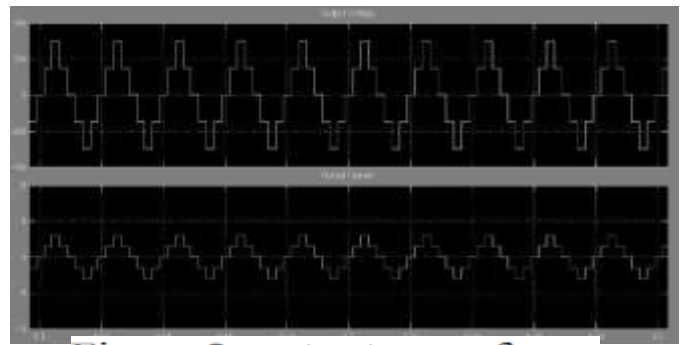

Figure 2. Simulink construction cascaded 5-level inverter

Figure 3. output waveform

Fundamental (50Hz) = 30.89 , THD= 23.20%

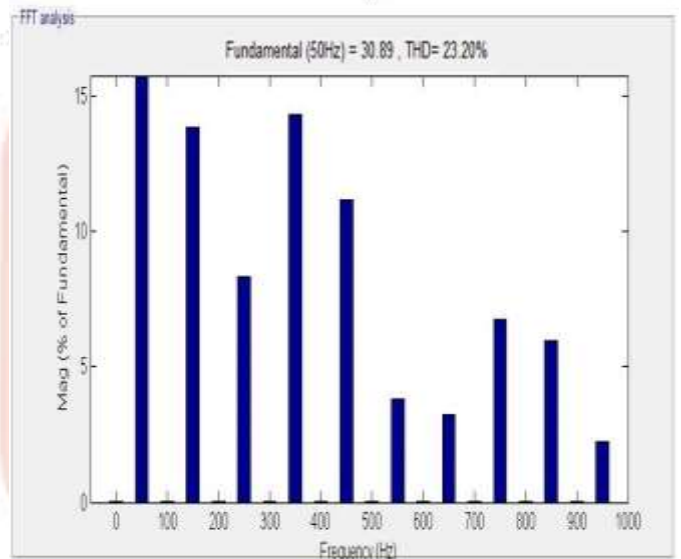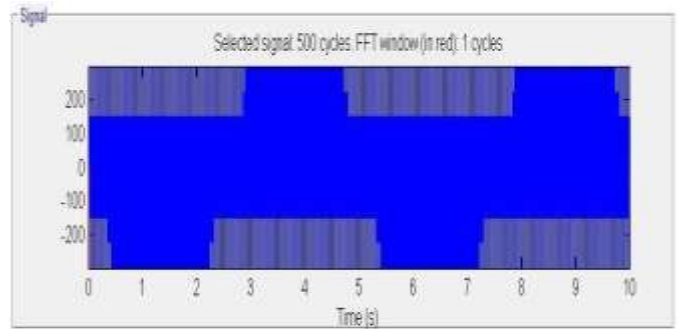## Conclusion:

This paper showed that this modified multilevel inverter topology with reduced number of switches can be implemented for industrial drive applications. This multilevel inverter structure and its basic operations have been analyzed. A detailed procedure for calculating required voltage level on each stage has been analyzed. As conventional five-level inverter involves eight switches, it increases switching losses; cost and circuit complexity. This 5-level inverter engages only eight switches which reduces switching losses, cost and circuit complexity. Moreover it effectively reduces lower order harmonics. Therefore effective reduction of total

harmonics distortion is achieved.

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