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Modeling of Capacitive Coupled Interconnects for Crosstalk Analysis in VLSI Circuits

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***Abstract*—In this paper, we have estimated the crosstalk noise for CMOS driver with coupled capacitive interconnect model in digital High-speed VLSI circuits. Crosstalk noise is one of the important factor for designing accurate interconnect models. Crosstalk by which a net/wire creates undesired effect on the neighbouring circuit due to the capacitive coupling which as a result increases the clock frequency , density of the circuit and reduces the performance The design of L - Model Interconnect with capacitively coupled at high frequencies, estimating the crosstalk noise on both ends of victim lines with respect to aggressor line for global interconnects at 180nm Technology Node. It is also analyzed analytically and simulated results using SPICE tool.**

I. INTRODUCTION

VLSI microcircuit design have entered a new technology termed as Very Deep Sub-Micron design technology. For design, below the feature size of micro-meter. It plays role of signal integrity (Eric Bogatin, 2010), which is the ability to get the signal correct response of a circuit. Major signal integrity issues are Crosstalk Noise, IR voltage drop in power lines, ringing and ground bounce,
Electro-migration, Crosstalk delay, etc,.

Crosstalk delay and crosstalk noise are the first effects which is occurs because of coupling capacitance and narrow feature sizes the coupling capacitance tends to be more important. Capacitance coupling is the main reason for crosstalk noise which occurred between two aggressor lines**.** In submicron designs technology increase of integration density has helped to the greater closeness of adjacent wires with higher aspect ratio, thus it results in an increase in effect such as crosstalk noise and delay Crosstalk is interconnection between the signals on two different interconnects[1-3].

One interconnect which is creating a crosstalk is called an “aggressor”, and the one who receives this effect is called a “victim”. Generally a wire can be active (aggressor) as well as a quit (victim) line. The RC delay of interconnect should be reduced so as to increase operating speed of an PCB’ components used to form crosstalk noise are coupling capacitance and mutual inductance[4-6].

Now a days, crosstalk noise or crosstalk delay has become a design challenging issues due to growing integration density with every technology node[2].Since, crosstalk in interconnect had a great impact on reliability and performance of PCB design, that’s why there is need to minimize this effect to maintain signal integrity in interconnect[7].

At low frequencies power is considered to be delivered to the load through the wire but in high frequency power is considered to be in electric field and magnetic fields in the form of voltage and currents are guided from source to load by required physical structure[8]. Any physical construction that will guide an electromagnetic wave is called a Transmission Line. Different Transmission lines are Microstrip line, a two-wire line, coaxial cable, a planar line, and a wire above the conducting plane.

In interconnect model Very Large Scale. Transmission line can be either a stripline or microstrip line in Integrated circuits[9].

Transmission line as a Micro-strip line is important in Printed Circuits Boards (PCB) where metallic strips line connecting to electronic elements are deposited on dielectric substrates. The primary key factors in determining the performance of an interconnect models are the impedance, delays and losses[10].

Transmission line is uniformly, the total line resistance, inductance and capacitance can characterized by line impedance. In order to model accurately to transmission line is driver, line impedance, and load capacitance. The exact values of separate three parameters are driver, line impedance, and load capacitance does not provide directly guideline to determine the best model for accuracy. Relative impedance is plays important role to determine the best model [11] of RLC interconnect line.

In the recent technology, Crosstalk noise analysis and noise minimization are becoming more important rather than the power and timing analysis. Crosstalk noise shows an undesirable impact on the reliability of Printed circuit boards Design Crosstalk noise creates many undesirable effects such as glitches, undershooting, overshooting, increasing and minimizing a signal delay. Telegraph equations are used to solve and an analytical formula for crosstalk peak noise in

case of Coupled capacitively lines is obtained.

The work is previously derives bounds for crosstalk noise for lumped RLC model assumes a step input for aggressor line but most of these models fail to represent in the distributed RLC nature of network[3].

At the semiconductor device level, although reducing the size of MOSFET has enabled incredible improvements in the switching speed, density, functionality, and cost of an integrated circuit, silicon devices are reaching the limits of dimension and material scaling. The semiconductor industry is anticipating that within a decade silicon devices will be unable to meet the demands at the nanoscale. At present, advanced MOSFET technology now faces many challenges. Scaling of the supply voltage is reduce the dynamic power however the degradation of dynamic performance with decreasing supply voltage is today particularly challenging.

In high-speed Printed Circuit Boards (PCBs). The physical construction of Printed Wiring Boards determines conductor's resistance, its self-capacitance and inductance, and the coupling to neighbouring conductors. At high frequencies of interest in electrical primitives appear on a Printed wiring boards as distributed RLC interconnect rather than lumped RLC elements to a behavior of transmission line (Stephen H. Hall, 2010). It is thus necessary for the high-speed circuit printed circuit board designer to have an understanding of how Printed wiring boards are constructed and manufacturing high-density Printed wiring boards.In this paper CMOS gate driver used instead of resistance line driver[4].

This paper is organized as follows In the Section II, deals with design of an accurate L-type interconnect model and closed-form expressions for the RLC Interconnect line. In Section III, CMOS gate of transistor using Alpha power-law model is used for capacitively coupled interconnect. In Section IV results validation between proposed interconnect model to the SPICE tool. Finally, concluded in Section V.

II. Analytical Interconnect Model

Moving to copper interconnect trenches are created in the underlying silicon oxide insulation layer where the metal is desired. A thick coating of copper deposited overfills the trenches of Chemical-mechanical Polishing is used to remove the copper to the level of the top of the insulation layer barrier metal needed to prevent spreading Metal Migration Can result in long-term failure of interconnects Reliability problem in integrated circuits Copper is better than Aluminium.

As speeds of circuit increase, the effects of on-chip crosstalk noise become more critical issues. Fig. 1 shows two neighbouring wires are called aggressor line and victim line. At high frequency signal of Very Large Scale Integration circuits causes the on-chip wires to exploit transmission line effects, These effects are electric (capacitive coupling) and magnetic (inductive coupling) couplings and thus we have electrical coupling and magnetic couplings between aggressor and victim pair of lines to reshape the signal waveforms through the transmission lines.

At the interconnect level, the major challenge in current high density integrated circuit is the electromagnetic (due to inductance) and electrostatic (due to capacitance) impacts in the signal carrying lines. Addressing these problems require better analysis of interconnect Resistance (R), Inductance (L), and Capacitance (C).

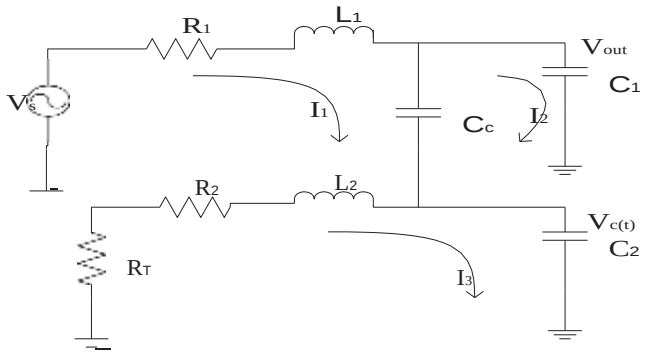

Fig. 1. Equivalent RLC interconnect model with coupling capacitances.

A. *Analysis of Crosstalk Noise voltage:*

For analysis of crosstalk noise voltage by applying loop analysis for Fig. 1.

Applying KVL in first mesh:

$$V_{in} = R_1 I_1(t) + L_1 \frac{d}{dt} I_1(t) + \frac{1}{C_c} \int \big(I_1(t) - I_2(2)\big)\, dt \quad (1)$$

Applying KVL in second mesh:

$$\frac{1}{C} \int \big(I_2(t) - I_1(t)\big)\, dt + \frac{1}{C} \int I_2(t)\, dt = 0 \quad (2)$$

Applying KVL in third mesh:

$$R_T I_3(t) + R_2 I_3(t) + L_2 \frac{d}{dt} I_3(t) + \frac{1}{C} \int I_3(t)\, dt = 0 \quad (3)$$

Applying Laplace transform in equation (1), (2) and (3)

$$V_{in}(s) = R_1 I_1(s) + sL_1 I_1(s) + \frac{1}{sC_c}\big(I_1(s) - I_2(s)\big) = 0 \quad (4)$$

$$I_2(s) = I_1(s) \frac{C_1}{C_1 + C_c} \quad (5)$$

$$R_T I_3(s) + R_2 I_3(s) + sL_1 I_3(s) + \frac{1}{sC_2} I_3(s) = 0 \quad (6)$$

From equation (4) and (5)

$$I_1(s) = \frac{V_{in}(s)}{R_1 + sL_1 + \frac{1}{sC_c}\left[1 - \frac{C_1}{C_1 + C_c}\right]} \quad (7)$$

Current through Victim's line capacitor:

$$I_v = I_3 \left[\frac{R_T + R_2 + sL_2}{R_T + R_2 + sL_2 + \frac{1}{sC_2}}\right] \quad (8)$$

$$then\ I_3 = I_1 \left[\frac{C_c}{C_c + C_2}\right] \quad (9)$$

Voltage across victim's capacitor:

$$V_c(s) = I_v \left[\frac{1}{sC_2}\right] \quad (10)$$

With help of equations (7), (8) and (9) in (10)

$$V_c(s) = \left[\frac{V_{in}(s)}{R_1 + sL_1 + \frac{1}{sC_c\left[1 - \frac{C_1}{C_1 + C_c}\right]}}\right] \cdot \left[\frac{R_T + R_2 + sL_2}{R_T + R_2 + sL_2 + \frac{1}{sC_2}} \cdot \left(\frac{1}{sC_2}\right)\right] \left(\frac{C_c}{C_c + C_2}\right) \quad (11)$$

Taking the Inverse Laplace Transform of equation (11) , $V_c(t)$ can be obtained

There fore $V_c(t) = L^{-1}[V_c(s)]$

B. *Closed form expressions for RLC Interconnect*

The semi-empirical closed-form expressions [6][7][8] for the Interconnect line resistance, Inductance and capacitance of the interconnect line has been presented used to calculate the per unit length *RLC* values of a Copper wire in this work.

The interconnect line resistance equation is given by

$$R = \frac{\rho L}{WT}\Omega \quad (12)$$

Where T is Thickness, W is Width, ρ is Resistivity, L is Length of the Interconnect line [6]

The line to substrate Capacitance equation is

$$\frac{C_s}{\varepsilon_{ox}} = \frac{w}{h} + 2.2217\left(\frac{s}{s+0.7h}\right)^{3.193} + 1.171\left(\frac{s}{s+1.5h}\right)^{0.7642} \times \left(\frac{T}{T+4.532h}\right)^{0.1204} \quad (13)$$

Coupling Capacitance equation is given by

$$\frac{C_c}{\varepsilon_{ox}} = 1.144\frac{T}{s}\left(\frac{h}{h+2.059s}\right)^{0.0944} + 0.7428\left(\frac{W}{W+1.592s}\right)^{1.144} + 1.158\left(\frac{W}{W+1.874s}\right)^{0.1612} \times \left(\frac{h}{h+0.9801s}\right)^{1.179} \quad (14)$$

Where ε_{ox} is Oxide permittivity, h is distance between interconnect to the substrate, s is spacing between adjacent interconnects and W is width of interconnect. [7]
Self-inductance of a line equation is given by

$$L_s = \frac{\mu_o L}{2\pi}\left[ln\left(\frac{2L}{W+T}\right) + \frac{1}{2} + 0.22\frac{W+T}{L}\right] \quad (15)$$

Mutual inductance of a line equation given by

$$L_m = \frac{\mu_o L}{2\pi}\left[ln\left(\frac{2L}{d}\right) - 1 + \frac{d}{L}\right] \quad (16)$$

Where μ_0 is the permeability of free space, d is the center to center distance between two adjacent interconnects.[8]

III. Proposed Interconnects Model

The aggressor (active) line and victim (quit) line CMOS gate of transistor can be represented using Alpha power-law model [9] is used for capacitively coupled interconnect which is given by

$$I_{DS} = \begin{cases} 0 & V_{GS} \le V_{TO} \quad : Cut-off\ regions \\ K_l(V_{GS} - V_{TO})^{\alpha/2}V_{DS} & V_{DS} < V_{DSAT} : linear\ region \\ K_s(V_{GS} - V_{TO})^{\alpha} & V_{DS} \ge V_{DSAT} : saturation\ region \end{cases}$$

where K_l is trans conductance parameters in linear region, Ks is trans conductance parameter in saturation region, V_{TO} is zero bias threshold voltage, V_{DSAT} is drain saturation voltage, and. α is velocity saturation index, The proposed CMOS gate Inverter driver coupled transmission line model[10] represented as below,

$$V_1 = (A_1 e^{-\gamma_e z} + A_2 e^{\gamma_e z}) + (A_3 e^{-\gamma_o z} + A_4 e^{\gamma_o z})$$
$$I_1 = \left(\frac{1}{Z_{0e}}\right)(A_1 e^{-\gamma_e z} - A_2 e^{\gamma_e z}) + \left(\frac{1}{Z_{0o}}\right)(A_3 e^{-\gamma_o z} - A_4 e^{\gamma_o z})$$
$$V_2 = (A_1 e^{-\gamma_e z} + A_2 e^{\gamma_e z}) - (A_3 e^{-\gamma_o z} + A_4 e^{\gamma_o z})$$
$$I_2 = \left(\frac{1}{Z_{0e}}\right)(A_1 e^{-\gamma_e z} - A_2 e^{\gamma_e z}) - \left(\frac{1}{Z_{0o}}\right)(A_3 e^{-\gamma_o z} - A_4 e^{\gamma_o z})$$

where $V_1(z, t)$ and $V_2(z, t)$ voltages wave form on aggressor line and victim line respectively, $I_1(z,t)$and $I_2(z,t)$ are voltage and current waveforms on active and quit line respectively. The A 's are constants values of boundary conditions. The constants Z_{OO}, γ_o and Z_{oe}, γ_e are characteristic impedance and propagation constant for odd modes and even modes. The coupled interconnects is receivers at the far-end of the lines are model as the lumped capacitive loads which is shown in Fig. 2.

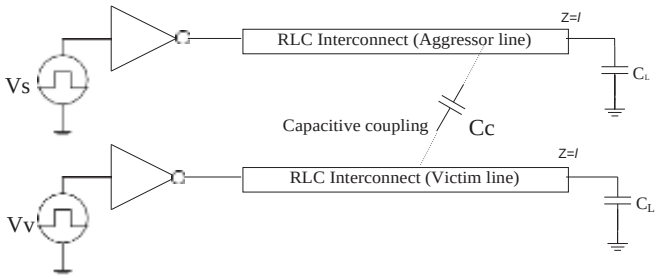

Fig. 2. RLC distributed interconnects driven by CMOS gate inverter drivers.

The interconnect model of an extracted value parameters RLC using in 180nm technology. So values of the parameter RLC using in 180nm technologies are extracted by using predictive technology model(PTM)[5] given in Table I and also these values are compared with closed form expressions equations(12)-(16) for interconnect line Resistance, capacitance and inductance.

TABLE I
THE EXTRACTED VALUES OF RLC PARAMETERS AT 180NM TECHNOLOGY

Parameters	Value/mm
Resistance(R1 and R2)	22Ω
Inductance(L1 and L2)	2.26nH
Capacitance(C1 and C2))	106.06fF
Coupling Capacitance(Cc)	107.16fF

The schematic RLC interconnect circuit for simulation is shown in Fig. 3. The high-speed interconnect model system specifications for two coupled interconnect lines and ground, the length of the line is l=2inches. The dimensions cross sections of a minimum sized wire in an 180nm process technology for CMOS inverter with a power supply voltage v=1.8v, length l=180nm, width=5um for PMOS and length l=180nm, w=2um for NMOS transistor. For interconnect consist of Materials dielectric constant Ɛr = 4.6 (FR-4), Overall height of the dielectric material H = 0.65um, Length of the trace L=2 Inch, trace width W = 0.80um, trace thickness T = 1.25um, and Spacing between coupled line S=0.80um.

IV. Results And Discussion

In this section summarizes the simulation results of our work. For a design of two parallel distributed RLC interconnect lines such as one line is called aggressor line and another is victim (quit) line as shown in Fig. 3. The aggressor line is excited by a step input signal with applied voltage is 1.8V, period of 10nsec, rise time and fall time of 100psec and also operating frequency of 100MHz to observe the input and output wave form on aggressor line is shown in Fig. 4. Near-

end crosstalk noise waveform for interconnect on victim line is shown in Fig. 5, Far-end crosstalk noise waveform for interconnect on victim line is shown in Fig. 6.

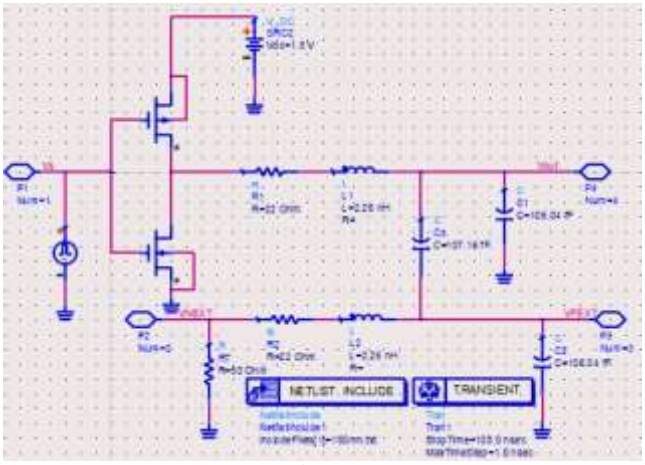

Fig. 3. RLC Interconnect circuit for Advanced design system (ADS) simulation

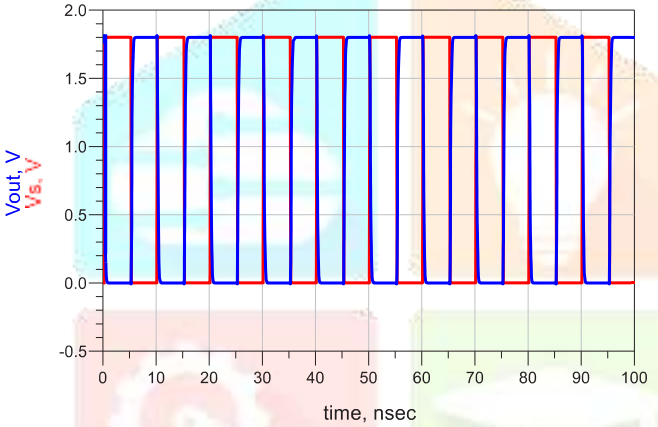

Fig. 4. Input and output waveform for interconnect on aggressor line using ADS Simulation.

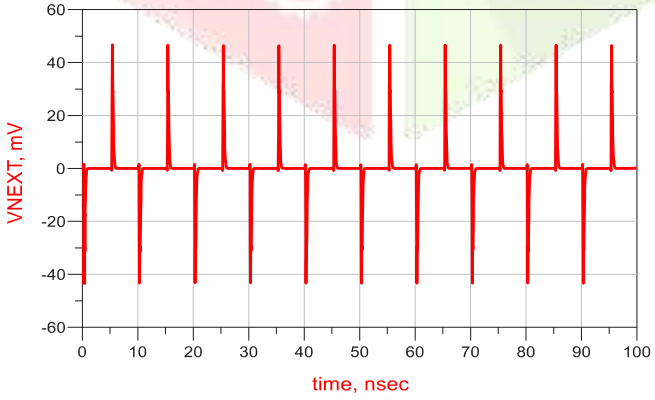

Fig. 5. Near-end crosstalk noise waveform for interconnect on victim line using ADS Simulation

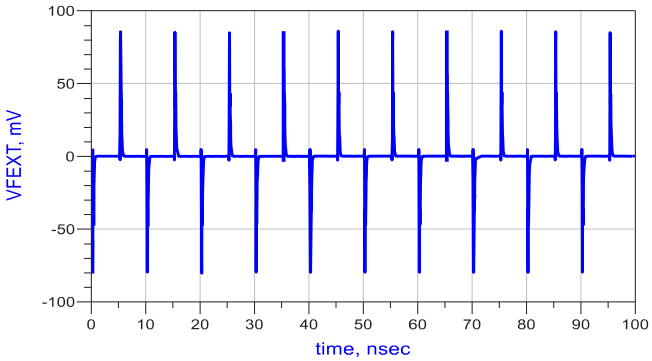

Fig. 6. Far-end crosstalk noise waveform for interconnect on victim line using ADS Simulation

The schematic distributed RLC interconnect circuit for SPICE tool is shown in Fig. 7. In this circuit similar parameters of proposed model are applied. Observe the input and output wave form on aggressor line is shown in Fig. 8, Near-end crosstalk noise (NEXT) waveform for interconnect on victim line is shown in Fig. 9 and Far-end crosstalk noise (FEXT) waveform for interconnect on victim line is shown in Fig. 10.

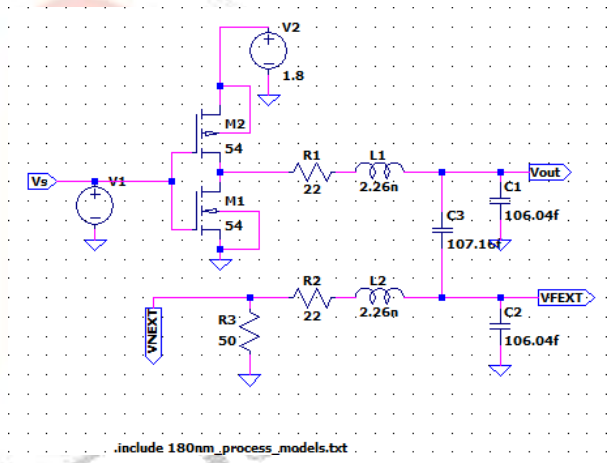

Fig. 7. Equivalent RLC Interconnect circuit for SPICE tool.

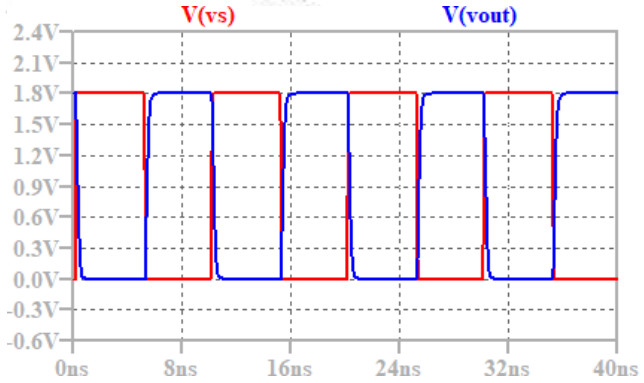

Fig. 8. Input and output waveform for Interconnect on aggressor line using SPICE tool

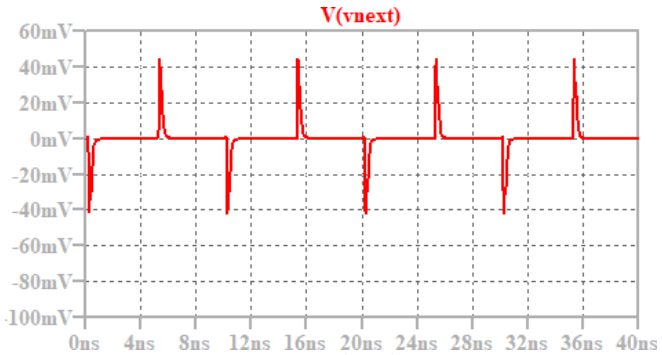

Fig. 9. Near-end crosstalk noise waveform for interconnect on victim line using SPICE tool.

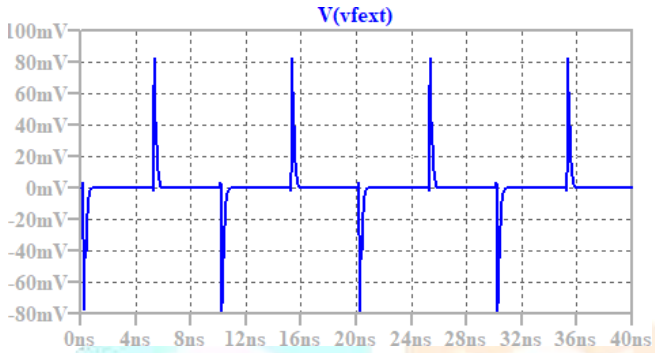

Fig. 10. Far-end crosstalk noise waveform for interconnect on victim line using SPICE tool

TABLE II
COMPARATIVE RESULTS ON VICTIM AND AGGRESSOR LINE CROSSTALK NOISE IS OBTAINED FROM SPICE TOOL AND PROPOSED MODEL

	Aggressor line		Victim line (crosstalk noise)	
	Vin (V)	Vout (V)	Vnext (mV)	Vfext (mV)
Proposed model Values	1.8	1.8	47	87
SPICE tool values	1.8	1.8	45	85

Table II discuss the comparison between proposed model of near end crosstalk noise and far end crosstalk noise with SPICE simulation of crosstalk noise for aggressor line and victim line. It is analyzed that error presented by proposed model is less than 1% compared to validated SPICE tool for near end crosstalk peak and far end crosstalk peak voltages.

V. CONCLUSION

In this paper proposed a problem of near end Crosstalk noise and far end crosstalk noise in high-speed transmission line based distributed RLC interconnect is presented using 180nm process technology analytical model for the estimation of the near end and far end Crosstalk noise peak voltage under capacitively coupled effect was introduced. Many researchers modeled the CMOS gate drivers rather than linear resistances driven circuit, which lead to inconsistency between the analytical model and simulation results. Simulation results show that the proposed L-type interconnect model for crosstalk noise based on CMOS gate inverter driven and capacitively coupled-transmission-line is most accurate noise estimation, efficient and compared with SPICE tool shows that the model captures crosstalk noise peaks voltage, timing, and waveform shape is good. The proposed model results in an error of near-end crosstalk noise peak voltage and far end crosstalk noise peak voltages are less than 1% compared from the SPICE tool. This work can be used in many applications such as high speed interconnect noise minimization.

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