DESIGN AN HIGH SPEED FAULT TOLERANT HAN CARLSON ADDER

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ABSTRACT: In digital VLSI systems, binary addition is the most significance arithmetic function. Adders are utilized as DSP lattice filter where by the parallel prefix adder the ripple carry adders are substituted for reducing the delay. The adder requirement is fast, low power consumption and area efficient. In this paper, the parallel prefix adder is initiated as speculative Han-Carlson adder for variant binary addition of the most significant arithmetic function. In this method the proposed system has wider word length and the parallel prefix adder is replaced as speculative Han-Carlson adder is introduced as different stages of Kogge-Stone and Brent-Kung adders in which the complexity of design of the adder is reduced. The design of Verilog code is implemented in Xilinx and simulated by utilizing ISim.

Index Terms: **adders, variable latency, parallel-prefix adders, speculative adders**

I. INTRODUCTION

The decimal numbers are easy to analyze and implement for performing arithmetic. In digital systems, like DSP (Digital Signal Processor), a microprocessor or ASIC (Application-Specific Integrated Circuit), binary numbers are practical for a provided computation. This occurs due to the binary values which are optimally efficient at presenting various values. Binary adders are one of the most essential logic elements within a digital system.

Binary adders are one of the basic and extensively utilized the operations of arithmetic in integrated circuits. They play a critical role in determining the performance of the design.
Arithmetic operations are the regular common operations in digital integrated circuits. The simplest circuits such as subtracts, adds, and divides or multiplies. The computation should be very speed and the area is consumed by the arithmetic units must be small. These are the two basic needs for any adder.

High speed adders are depends on the previous carry for generating the present sum. In integer addition any reduces in delay will directly related to a maximize in throughput. In nanometer range, it is most significant to improve addition algorithm which produces high performance while reducing the power. Parallel prefix adders are more satisfactory for VLSI implementation due to they rely on the utilization of simple cells and sustain regular connection among them. We can define each prefix.

In ripple carry adder, the operation of each bit full adder contains sum and carry. The carry will be provided to the next bit full adder operation, the process is continuous until the Nth bit operation. In the N-1th bit full adder operation the carry will be provided to the Nth bit full adder operation which is present in the ripple carry adder.

For 16-bit ripple carry adder, the initial bit carry is provided to second bit full adder, second bit carry is given to the next bit full adder, similarly the operation is similar until fifteenth bit carry is provided to sixteenth bit full adder. The addition operation is executed from least significant bit to most significant bit in ripple carry adder.

II. EXISTED SYSTEM

The existed structure is depends on the schemes of both incrementation and the concatenation with the structure of Conv-CSKA and therefore, it is represented by CI-CSKA. It produces us with the ability for utilizing the simpler carry skip logics. The logic is 2:1 multiplexers instead of AOI/OAI compound gates.

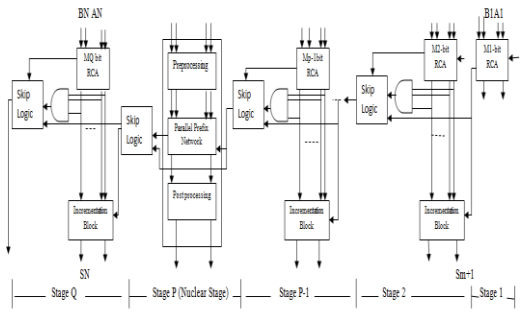

Fig. 1 Structure of the existed hybrid variable latency CSKA

The gates, which contains less transistors, has lower area, delay and less power consumption when differentiate with those of the 2:1 multiplexer. In this structure, as the carry propagates through the skip logics, it becomes most complemented. Hence, the carry complement is produced at the skip logic output of even stages. The structure has a significant lower propagation delay with a slightly lower area differentiated with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the existed CI-CSKA is a little more than that of the conventional one. This is because of maximize in the number of the gates, which imposes a higher wiring capacitance.

III. PROPOSED SYSTEM

The Han-Carlson prefix tree is as same to the Kogge-Stone's structure because it has a maximum fan-out of 2 or f = 0. The variant is that the proposed adder utilizes few cells and wire tracks than the Kogge-Stone. Single extra logic level is the cost. Han-Carlson prefix tree can be observed as a scarce version of Kogge-Stone prefix tree.

At all logic levels the fan-out is similar. For building a Han-Carlson prefix tree, we must easily modify the pseudo-code in Kogge-Stone's structure. The major variant of proposed system is that in every other bit, Han-Carlson prefix tree keep cells and the last logic level accounts for the missing carries in each logic level.

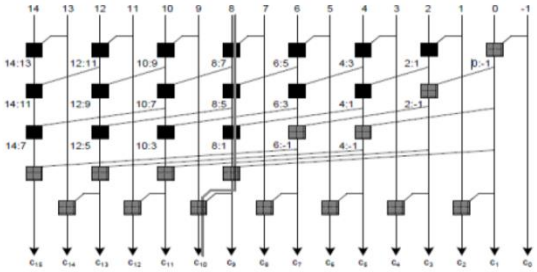

Fig 2. 16-bit Han-Carlson prefix Tree

A Han-Carlson prefix tree which is 16 bit is shown in above figure 2, ignoring the buffers. The thick solid line is represented as critical path. Han-Carlson adder provides a good trade-off among fan-out, number of logic levels and black cells. In Han-Carlson topology, the outer rows are represented as Brent-Kung graphs, while the inner rows are denoted as Kogge-Stone graphs.

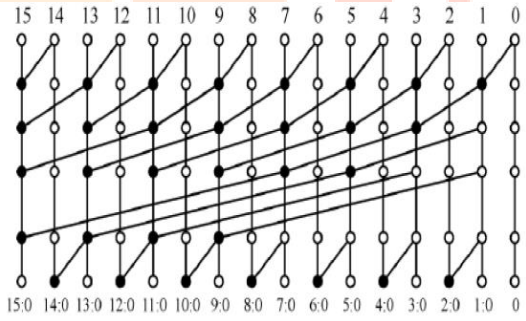

Fig 3. 16-bit Han- Carlson topology

Fig 3 shows the Han-Carlson adder which utilizes a single Brent-Kung level at the beginning and at the end of the graph, the number of levels is 1+ $log2(n)$. Here black dots represent the prefix operator, while white dots are represented as simple placeholders.

Han-Carlson adder consists of a good trade-off among fanout, number of black cells and number of logic levels. Han-Carlson adder can perform speed performance which is equal with Kogge-Stone adder, at less area and lower power consumption. Due to these reasons, a Han-Carlson speculative prefix-processing stage is generated by reducing the last rows of the Kogge-Stone part of the adder.

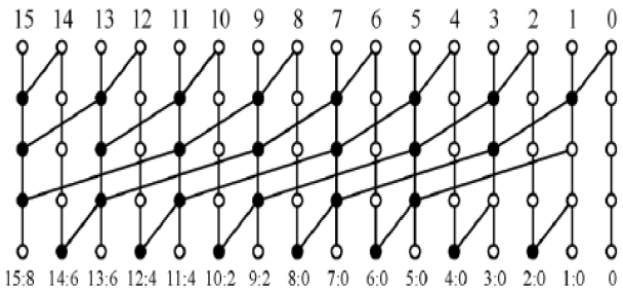

Fig 4 Han-Carlson speculative prefix-processing stage

IV. HAN-CARLSON ADDER WITH ERROR DETECTION AND ERROR CORRECTION

The conditions in which at least one of the approximate carries is wrong (mis-prediction) are signaled by the error detection stage. In case of mis-prediction, an error signal is declared by detection of error stage and discarded the post-processing stage output. The error correction stage will provide the correct sum in the next clock period. It calculates the exact carry signals, which is to be utilized in mis-prediction. The error correction stage is collected by the prefix- processing stage levels reduced for attaining the speculative adder.

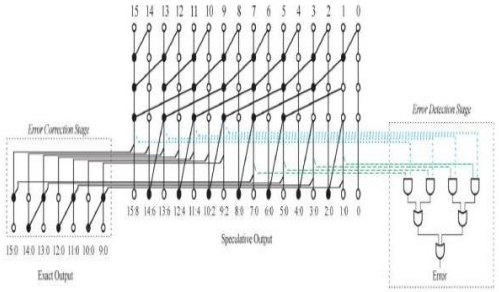

Fig 5. Error correction and detection stages for the proposed speculative Han-Carlson adder

V. RESULTS

Fig 6. RTL Schematic

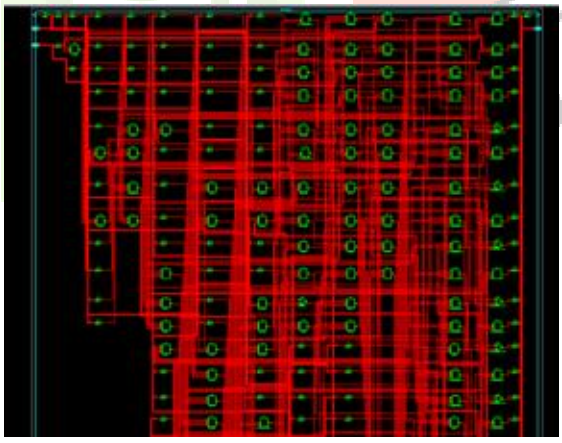

Fig 7. Technology Schematic

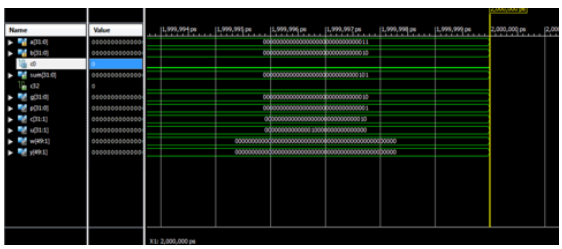

Fig 8. Output Waveform

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	70	960	7%
Number of 4 input LUTs	125	1920	6%
Number of bonded IOBs	98	66	148%

Fig 9. Report

VI. CONCLUSION

In this paper a novel variable inertness Han-Carlson parallel prefix speculative adder for fast application is proposed. A new, more accurate, error detection network is introduced, which allows reducing the error probability compared to the previous approaches. Compared with traditional, non-speculative, adders, our analysis exhibits that variable inertness Han-Carlson adders show sensible upgrades when the most elevated velocity is required; generally the weight forced by error detection and error correction stages over powers any advantage. Additional work is required to extend the speculative approach to other parallel-prefix architectures, such as Brent-Kung, Lander-Fisher, and Knowles.

VII. REFERENCES

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