Low Power Circuit analysis with SiGe MOSFET at 22nm

[1]R P Mahajan,[2]S R Patil,[3]D K Gautam

[1] Research Scholar,[2] Research Scholar,[3] Professor
Electronics Department,
North Maharashtra University, Jalgaon, Maharashtra, India

Abstract : The paper presents the circuit implementation of pseudomorphic structure wherein the power analysis is carried with the help of CMOS circuits. The proposed device structure has incorporated silicon germanium (SiGe) layer as a channel. The device geometry is optimized for 22nm technology node. The high-k dielectric metal gate structure is used to provide the low leakage current. Silvaco Athena and Atlas simulators are used for simulation as well as for finding the electrical characteristics of the structures. Result comparison shows the presented device structure provides low power, high speed solution to the recent technology trends.

IndexTerms **- High-k,Pseudomorphic-Structures, SiGe MOSFET, SILVACO TCAD, Threshold Voltage**

I. INTRODUCTION

Scaling of the bulk complementary metal oxide semiconductor (CMOS) is struggling for further reduction due to the technology limitations. However, the scaling gives the greatest interest to accomplish the high integration, speed and performance. Moreover the scaling enables high device integration, the Power consumption is becoming one of the most critical design challenges in the VLSI circuits. Optimization techniques for low power are being employed at all design levels of abstraction. Paper proposes the optimized device structure and reports the power analysis at 22nm with basic building gates of CMOS circuits for the first time. Simultaneously the device is optimized for low leakage current and high speed operation.

As CMOS devices reaches to deep submicrometer and below consequently the gate dielectric thickness simultaneously gate leakage current becomes significant for power consumption. Analysis of the effect of leakage current on circuit operation shows increased leakage current more than 100 A/cm2 may causes the computer chips to generate heat with power densities of 100 w/cm2. This makes chip cooling challenging and costly. Conversely it becomes very challenging to control the leakage current and accordingly impact on the performance of the device as well as circuit [1]. Detailing of gate leakage current with different doping concentration of polysilicon gate for conventional silicon MOSFET can be found in [2]–[4]. Manju et al has reported the n-MOSFET structure with graded polysilicon. Device is implemented at 0.13 m with 18 Ao effective oxide thickness. Structure is analyzed for constant doping as well as consistently increasing doping at polysilicon gate. Results shows reduction in leakage current by 25 % for consistently increasing graded doped polysilicon [5].

In accordance with the International Technological Roadmap for Semiconductors (ITRS), sub-100-nm generation MOS devices requires the use of high-k dielectric materials with EOT less than 2 nm to reduce gate leakage current [6]. Review of high-k dielectric devices with metal gate can be found in [1]. Chau et al reported about the performance enhancement and reduction in gate leakage current via use of high-k dielectrics and metal gate electrodes [7]. Analysis of threshold voltage for high-k/metal gate structure is depicted by Ma Fei et al [8]. Author has implemented two dimensional structure with ISE-TCAD. The influence of metal gate and high-k stacks on the flat-band voltage is investigated in the paper. Intel has reported the successful implementation of silicon MOSFET on 45 m with high-k metal gate.

All the previously reported work has carried with conventional silicon technology. However the further improvement in mobility cab be achieved by the incorporation of silicon germanium layer into the structure. Due to the band gap difference in silicon and germanium material carrier can easily fall form higher band gap to lower. Generated strain will work as a mobility booster in nanometer regime [9]–[14].

Figure 1 represents the proposed implemented structure. SiGe channel layer is sandwiched between Si-cap layer and Si buffer layer. The purpose of Cap layer is to provide good interface quality with native oxide. LDD source and drain (S/D) structure is implemented with shallow junction depth. The use of metal gate with high-k dielectric further reduces the problem of leakage current citerashmi2014. The optimized structure of silicon germanium MOSFET at 22 nm and corresponding analytical model is presented in [15], [16].

Section 2 of this paper gives details about the circuit implementation of the proposed device structure and corresponding power analysis. Moreover the device is already optimized for high switching speed as well as lower leakage current. Furthermore the detailed results are discussed in section 3. Concluding remarks are presented in section 4.

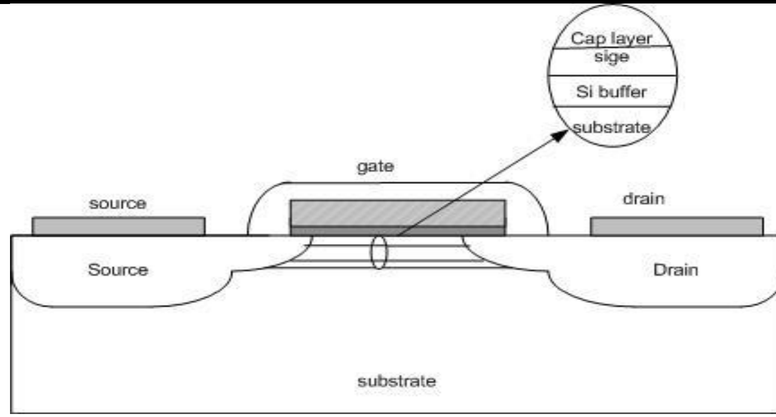

Fig. 1: Cross section of SiGe p-MOS structure

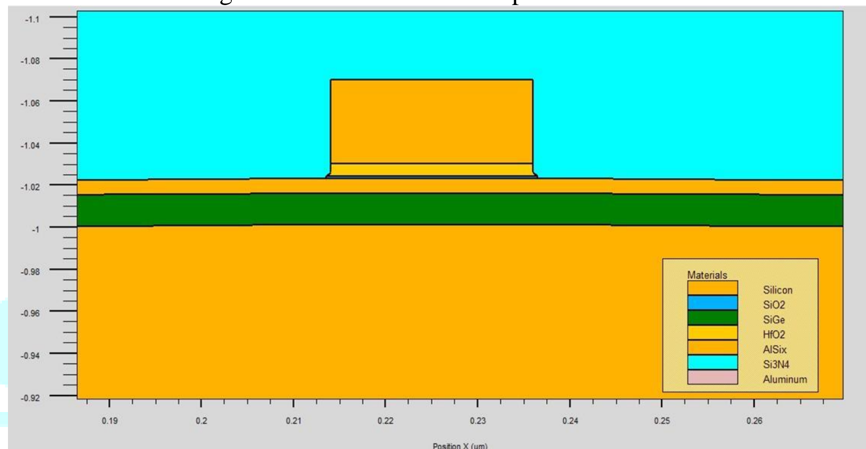

Fig. 2: HfO2/SiO2 stack as a dielectric with metal gate

II. MODELLING AND DESIGN OF THE DEVICE

Device is implemented at 22nm which is maintained as a device physical gate length with SILVACO Athena process simulator. Process is initiated with mesh formation followed by substrate declaration with the concentration $2x10^{18}$. Epitaxial growth with phosphorous concentration $4x10^{16}$ is developed on the substrate. Spacer formation is done with Silicon Nitrite. Si buffer layer is developed with thickness 10 nm followed by SiGe layer with the same thickness and cap layer used is 7 nm thick. These three layers are doped with phosphorous. Phosphorous doping and Ge concentration in SiGe layer is varied to optimize the performance of the device. The fabricated structure is shown in figure 2.

As the device is at very small dimensions it is necessary to maintain shallow Source/Drain implantations. For the structures containing many non-planar layers more sophisticated simulation models are required. The most flexible and universal approach to simulate ion implantation in non-standard conditions is the Monte Carlo technique. Monte Carlo implantation method is used here for maintaining shallow junction depth. It is one type of deposition model mentioned in TCAD device simulator which can be used to model low-pressure chemical vapor deposition(LPCVD). Mentioned model is used with the statement implant along with tilt, energy and rotation. The model uses an analytical approach to calculate a surface diffusion through a normalized Gaussian distribution [17], [18]. Measured S/D junction depth(xj) is 3.54 nm with the concentration $2x10^{20}$.

In conventional silicon CMOS technology doped polysilicon has used as the gate electrode. When voltage gets applied to doped polysilicon, depletion region will get formed. It reduces inversion charge resulting increase in threshold and degradation in drive current. These transistors exhibit severely degraded channel mobility due to the coupling of phonon modes in high-K to the inversion channel charge carriers. Mobility degradation could be reduced by using metal gate electrodes along with strained channel layer. Used electrodes will help to reduce phonon scattering. Metal gate is implemented on the same geometrical stack of oxides mentioned in B and represented in figure 3. Gate workfunction is important parameter which should be highlighted in device modeling. Workfunction for the implemented device is 3.95 [17] reflecting Al gate on HfO2 dielectric. Pseudomorphic n-MOSFET structure is optimized followed by the successful implementation of p-MOSFET.

There are two main components that constitute the power used by a CMOS integrated circuit: static power and the dynamic power. Static power essentially consists of the power used when the transistor is not in the process of switching and is essentially determined by the equation 1.

$$Pstatic = Istatic \ x \ VDD_i \qquad (1)$$

Where, VDD is the supply voltage and Istatic is the total current flowing through the device. Typically, CMOS technology has been praised for its low static power. Dynamic power is the sum of transient power consumption and the capacitive load power consumption. Ptransient represents the amount of power consumed when the device changes logic states, i.e. ”0” bit to ”1” bit or vice versa. Capacitive load power consumption as its name suggests, represents the power used to charge the load capacitance. Together it is represented by equation 2

$$Pdynamic = Pcap + Ptrasient = (C_L + C).V_{DD}^2.f.N \qquad (2)$$

where CL is the load capacitance, C is the internal capacitance of the circuit, f is the frequency of operation, and N is the number of bits that are switching. Conventionally as performance increases, meaning the speed and frequency of the IC increases, the amount of dynamic power also increases.

After more than two decades of relentless scaling to ever smaller dimensions for higher packing density, faster circuit speed, and lower power dissipation, CMOS technology has become the prevailing technology for very large scale integration (VLSI) applications today. Hence in the presented research work the device analysis is carried out with different CMOS circuits presented in figure 3 with 22 nm technology node device.

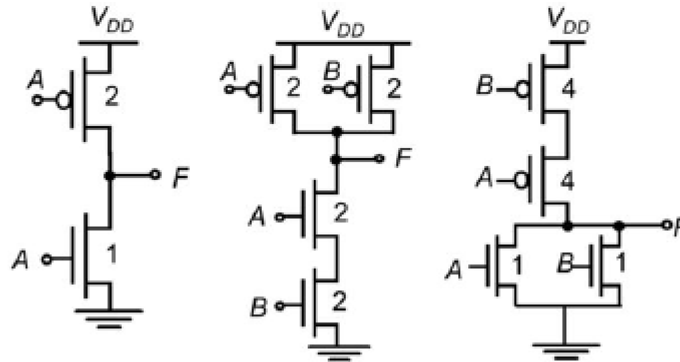

Fig. 3: Schematic diagram of implemented circuits

III. RESULTS AND ANALYSIS

In case of CMOS technology, the static power consumption is almost negligible hence the work is concentrated to calculate the dynamic power. For the power calculations equation 2 is used, wherein CL is the load capacitor which is considered as 3fF for the implemented CMOS inverter. The internal capacitor C is extracted from the device. The used p-MOSFET and n-MOSFET devices are virtually fabricated with the Silvaco Athena simulator at 22nm technology node. The electrical characterization of the device has been performed with Silvaco Atlas simulator and corresponding capacitors are calculated. Figure 3 represents the implemented CMOS inverter circuit along with the used capacitive load. In Table 1 implemented results are compared with the previously reported results [5]. Comparison is based on circuit power dissipation as well as device gate leakage current. From the analysis it has been found that the fabricated device structure provides the contributory solution for low power, high speed circuits with less leakage current.

Table 1 shows the calculated power for the inverter, NAND gate and NOR gate with VDD equals to 1.8 Volt, at 1 GHz frequency. Results shows that power dissipation is reduced with considerable amount as compared to previously reported results. Circuit performance is analyzed and detailed in figure label power. Power analysis is carried out for different frequencies with different drain power supplies. From the analysis it has been observed that the proposed device structure in the research gives optimum power consumption at CMOS circuit level.

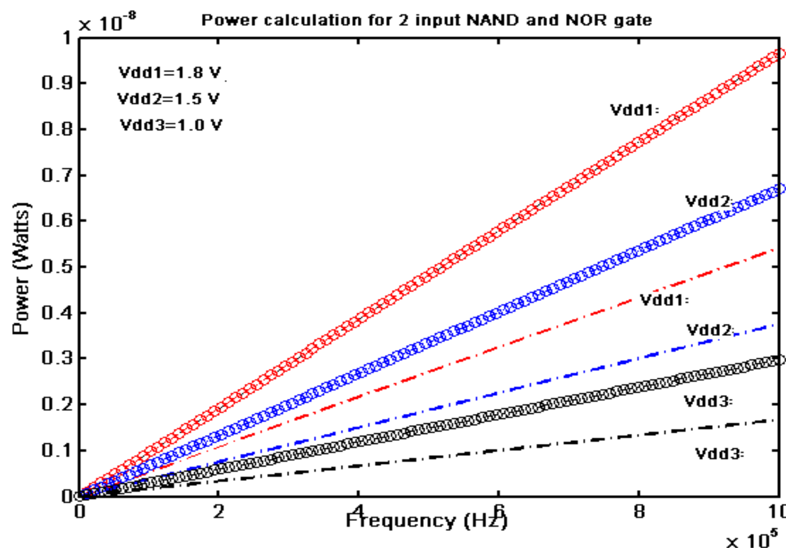

Fig. 4: Power analysis of CMOS NAND and NOR

Table 1: Descriptive Statics

Type of the circuit	Implemented Circuit(Vdd=1.8 volt, freq=1GHz, 22nm gate length)	Reported Results (Vdd=0.9 volt, channel length =20nm)
Inverter	9.84×10^{-10}W	235×10^{-9} W
NAND Gate (Considering inverter as a load)	3.01×10^{-9} W	--
NOR Gate (Considering inverter as a load)	5.3×10^{-9}W	--

IV. CONCLUSION

In this paper the circuit level implementation of SiGe MOSFET with 22nm geometry node is analyzed. Circuit analysis shows that the fabricated device structure provides the contributory solution for low power, high speed circuits. Power analysis is carried out for different frequencies with different drain power supplies. From the analysis it has been observed that the proposed device structure in the research gives optimum power consumption at CMOS circuit level.

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