PERFORMANCE COMPARISION OF SEVEN AND FIVE LEVEL CASCADED H-BRIDGE SINGLE PHASE INVERTER

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***Abstract*—** Multilevel inverter technology has emerged recently as a very important alternative in the area of high power ,medium voltage energy control .This paper present the most important topologies like H-bridge inverter, diode-clamped inverter (neutral-point clamped) and capacitor clamped (flying capacitor) and their working as single phase. Cascaded H-Bridge Multilevel inverters are basically used for high power applications as it helps in getting improved output waveform, nearly sinusoidal. As the levels obtained by Multilevel inverters increased the efficiency, harmonic content reduced but with this merits there are certain problems offered by it .This paper study this tradeoffs. The theoretical study made in this paper considers the comparison of 7-level and 5-level inverters.

***Index term*-5-level, 7-level multilevel inverter, H-bridge Inverter, Diode clamped Inverter, Cascaded multilevel inverter, Flying Capacitor**

1.INTRODUCTION

Inverters are needed to convert the direct current electricity produced into alternating current electricity required for loads. Multilevel inverter promises a lot of advantages over conventional inverter especially for high power applications. Some of the advantages are that the output waveform were improved since multilevel inverter produced nearly sinusoidal output voltage waveforms, hence the total harmonic distortion also low, reduced switching losses and the filter needed to smooth the output voltage is small hence, the system is compact, lighter and much cheaper.

There are different types of multilevel circuits involved. The first topology introduced was the series H-bridge design followed by the diode clamped converter, which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through interphase reactors. In this design, the semiconductors block the entire dc voltage, but share the load current. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require clamping diode and flying capacitor

II.COMPARISION OF SEVEN LEVEL AND FIVE LEVEL INVERTER

A .SEVEN LEVEL MULTILEVEL INVERTER

The Figure 1 . Shows the Simulation result obtained 7-level inverter topology and it is very much similar to 5-Level inverter which comprised of an additional auxiliary circuit. In general it comprised of two bidirectional switches (the auxiliary circuit), full bridge inverter, and three capacitors. The two Auxiliary circuit present comprised of two switching element and eight diodes and is responsible for the generation of one third and two third levels of dc supply voltage. The three capacitors are used as voltage divider. The ON-OFF
conditions of four switches used in H-bridge and the two used in auxiliary circuit decides the operation of the new topology and the output voltage levels i.e. +Vdc, +2Vdc/3, +Vdc/3, 0, -Vdc, -Vdc/3 & -2Vdc/3. Considering the direction of the load current the switch in auxiliary circuit must be switched ON and OFF. The operations of the new topology using the particular combination of switches is explained in table no 1.below.

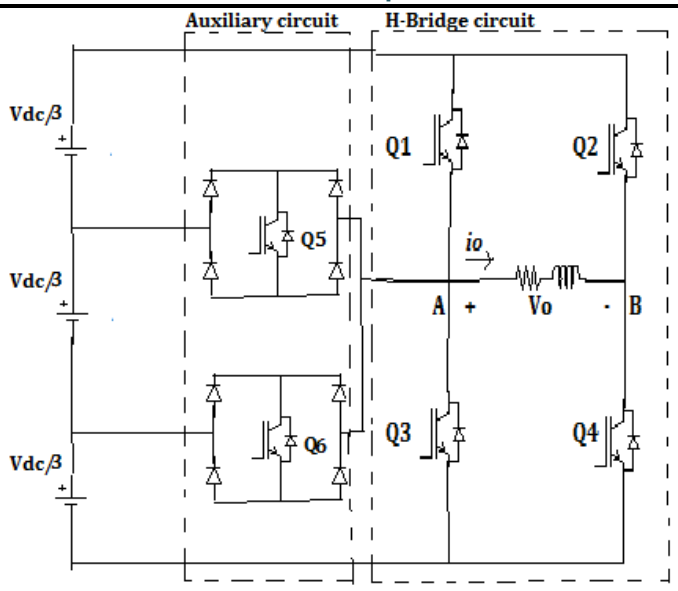

Figure 1. Seven Level Inverter Topology

Table 1 : Various output obtained by ON/OFF Switching Conditions of Switches in Seven Level inverter

Output voltage$_{ss}$ Voltage	Q 1	Q2	Q3	Q4	Q5	Q6
+Vdc	1	0	0	1	0	0
+2/3Vdc	0	0	0	1	1	0
+1/3Vdc	0	0	0	1	0	1
0	0	0	1	1	0	0
0*	1	1	0	0	0	0
-1/3Vdc/	0	1	0	0	1	0
-2/3Vdc	0	1	0	0	0	1
-Vdc	0	1	1	0	0	0

B. FIVE LEVEL MULTILEVEL INVERTER

The Figure 2. Shows the 5-level inverter topology which comprised of auxiliary circuit, full bridge inverter and two capacitors. Auxiliary circuit comprised of one switching element and four diodes and is responsible for the generation of half level dc supply voltage. The two capacitors are used as voltage divider. The on-off conditions of four switches used in H-bridge and the one used in auxiliary circuit decithe operation of the new topology and the output voltage levels i.e. +Vdc, +Vdc/2, 0, -Vdc & -Vdc/2. Considering the direction of the the new
topology using the particular combination of switches is explained in table below

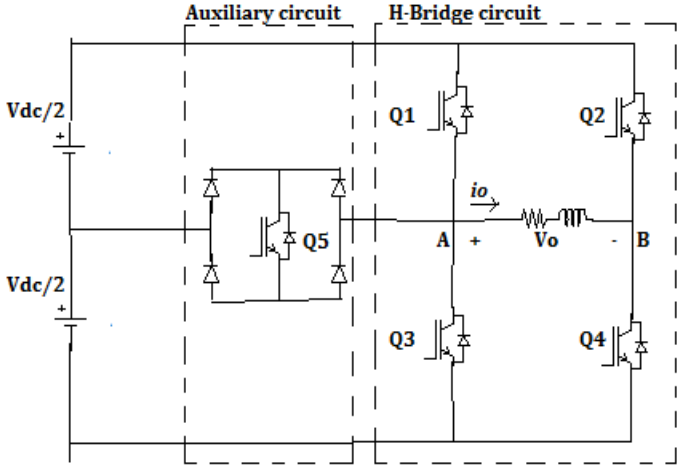

Figure 2. Five Level Inverter

Table 2: Various output obtained by ON/OFF Switching Conditions of Switches in Five Level inverter

Output Voltage	Q1	Q2	Q3	Q4	Q5
+Vdc	1	0	0	0	1
+Vdc/2	0	0	0	1	1
0	0	0	1	1	0
-Vdc	0	1	0	0	1
-Vdc/2	1	0	0	1	0

III. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The Multilevel Inverters can be classified into following three types

A.DIODE- CLAMPED MULTILEVEL INVERTERD (DCMLI)

If a diode is required to use as a power devices voltage stress limiter. The voltage across each capacitor and switch is Vdc. The main reason behind using diodes to limit the power The m-Level DCMLI typically comprised of (m-1) Capacitors on the DC bus,2(m-1) switching devices and (m-1)(m-2) clamping diodes and produces m levels on the phase voltage. This Inverter produces half of the DC source output as the maximum output voltage which is the main drawback of it which is solved by using twice the voltage source or cascading two diode clamped multilevel inverters. The figure 3 below shows the One phase of a diode clamped inverter

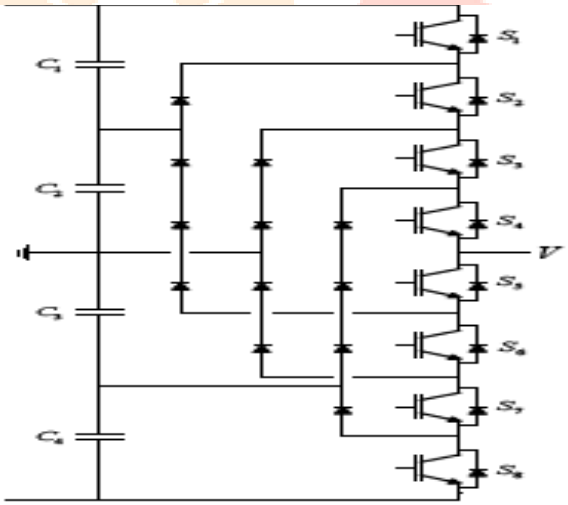

Figure 3 . One phase of a Diode Clamped Inverter

B.FLYING CAPACITOR MULTILEVEL INVERTER(FCMLI):

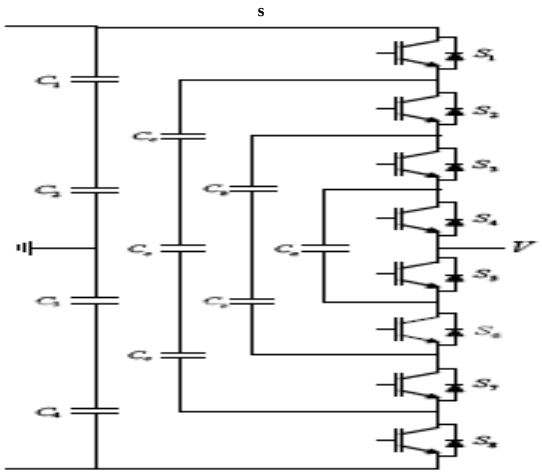

Figure 4. One phase of a 5-level Flying capacitor multilevel inverter

IV.MODULATION TECHNIQUE

The modulation technique used here is SPWM i.e. Sinusoidal Pulse Width modulation in which a triangular carrier wave signal is compared with two sinusoidal reference signal in case of 5 Level and three sinusoidal reference signal in case of 7 Level having same frequency and in phase but having different offset voltage. The Phase depends on Modulation Index which is AM//2Ac in case of 5Level and AM//3Ac in case of 7 Level where AM is the peak value of reference voltage and Ac is the peak value of carrier wave. The recommended range for modulation Index(M) is 0.66 and 1.

V. SIMULATION AND RESULT

The figure 5 and 6 shown below shows the implementation of SPWM Technique on 5-Level and7-Level Multilevel Inverters

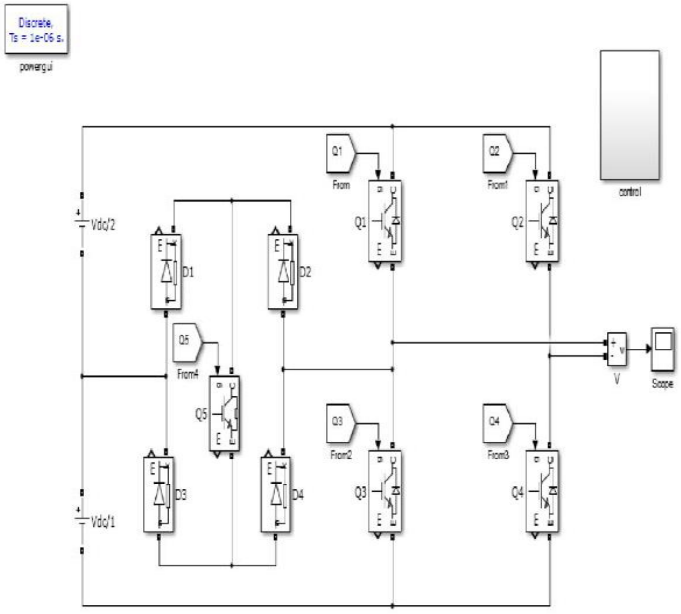

Figure 5 : MATLAB Model of 5-Level Multilevel Inverter

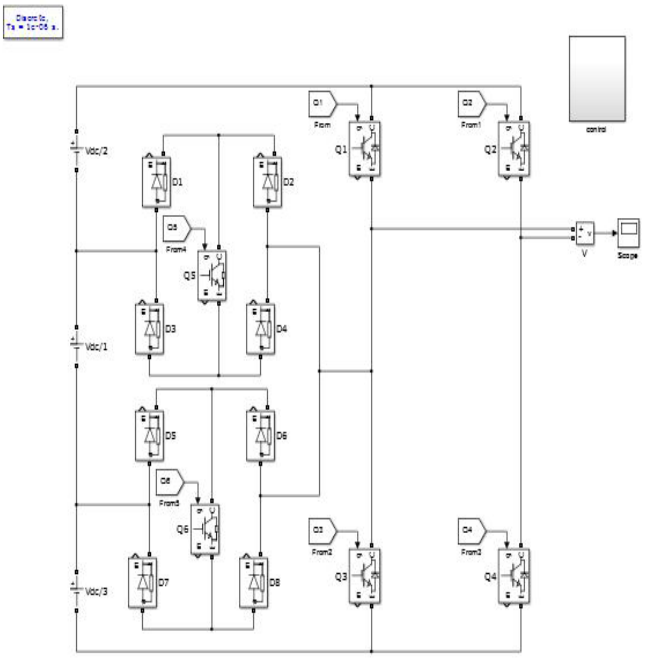

Figure 6. MATLAB Model of 7- level Multilevel Inverter

The Comparisons between 5level and 7level is given in table 3.

Table 3 . Results after comparison for same input given to 5 and 7 Level

	5 level	7 level
Total Harmonic Distortion	High	low
Efficiency	Low	High
Complexity	Low	High
Cost	Low	High

VI. CONCLUSION

The Total Harmonic Distortion (THD)and the simulation result obtained .The level gets reduce as the level of multilevel increases the efficiency is increased but the complexity of the circuit is also increased therefore the cost esclates but this problem can be solved by using new topology for same output and levels.

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