AN ENVELOPE TYPE MODULE: ASYMMETRIC MULTILEVEL INVERTER WITH REDUCED COMPONENTS.

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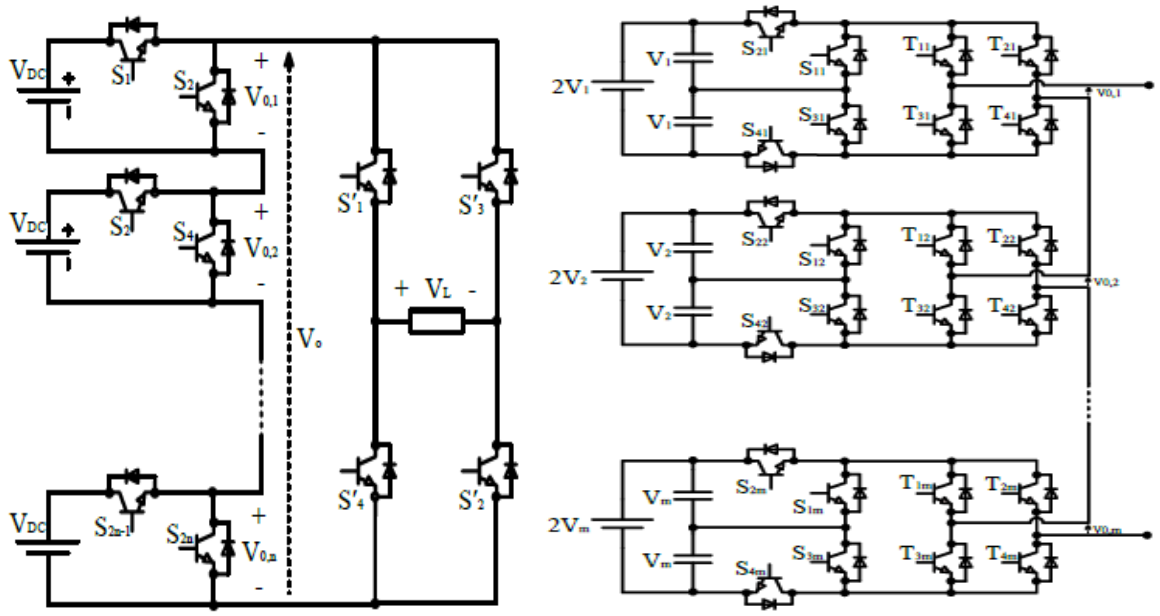
Abstract :This paper presents a new E-Type module for asymmetrical multilevel inverters with reduced components. Each module produces 13 levels with four unequal DC sources and 10 switches. The design of the proposed module makes some preferable features with a better quality than similar modules such as the low number of semiconductors and DC sources and low switching frequency. Also, this module is able to create a negative level without any additional circuit such as an H-bridge which causes reduction of voltage stress on switches. Cascade connection of the proposed structure leads to a modular topology with more levels and higher voltages.MATLAB simulations are presented to validate the proposed module good performance.
IndexTerms **- Asymmetric, components,Matlab, E-Type, multilevel inverter, power electronics.**__

1. Introduction

Multilevel inverters (MLIs) have been innovated as necessary cost benefit devices with a wide range of applications. They have been in the focus for decades because of interesting features such as high quality output voltage, operation in high voltage/power, low stress on switches, etc. Multilevel converters have a wide range of applications which has rapidly developed the area of power electronics with good potential for further technology [1].They can be used in photovoltaic systems, wind farms, and HVDC systems. Multilevel converters are different arrangements of semiconductor switches with DC links to create n-level output waveform which are divided into three main categories [2]: Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascade H-Bridge (CHB). In 1981, NPC was introduced as the first multilevel converter which can be used in medium voltage applications. Early 1990s, FC was presented and in 1996, CHB was reintroduced. Design of multilevel inverters depends on the number of voltage levels, number of semiconductors, output quality, number of DC supplies andDC link capacitors, THD amplitude, maximum voltage level, creating positive and negative level, modularity, switch stress and total standing voltage (TSV).

Researchers presented different types of modular multilevel inverters. As shown in Fig.1.a, each level is created by two switches and one source in [3]. These levels are connected in series together to achieve positive voltage levels and an auxiliary H-bridge circuit is used to create alternative voltage. Note that, H-bridge switches tolerate more voltages than other switches. As shown in Fig.1.b, the stress of H-bridge switches are divided between each sub-module [4]. Two capacitors are added for each DC source to reach more voltage levels with the penalty of using more components. Researchers tried to reach more levels with lower components. Asymmetric multilevel inverters which have unequal DC links become interesting in order to increase the quality of output waveform by minimizing the number of components. Modules are designed based on optimal using of DC links by reduced switches.

One of the important factors of MLI design for high voltage applications is high voltage stress on the switches of the output H-bridge. Therefore, a redesign is vital to reduce the stress of the switches by dividing H-bridge voltage into all sub-modules in order to have a uniform stress on all switches which in turn leads to the increasing number of semiconductors and total standing voltage (TSV) of the module. This paper aims to achieve maximum capacity from DC link by a suitable arrangement of switches which improves economic implementation cost, switching frequency, TSV, number of levels, and THD. It presents a new asymmetric multilevel module based on cascade category which does not need any additional circuit to create negative voltage levels. Also, it makes 13 levels by reduced switches. The proposed system illustrates multilevel inverters including module description, switching patterns, cascade connection and comparison table with similar modules. Selective harmonic elimination (SHE) is also introduced for for eliminating harmonics.



(a) **(b)**

Fig.1 Some Modular multilevel inverter topologies

2. Comparison with other topology:

A comparative study between the proposed topology and other famous ones is carried out regarding the number of semiconductors, DC links, capability to generate negative voltage level and the number ofswitches. Among these topologies are: NPC, FC, CHB. According to Table I, the number of semiconductors (switches and diodes), number of DC links are reduced down to $5(NL-1)/6$ and $(NL-1)/3$ respectively which are lower than other topologies. Note that this topology can generate a negative voltage level which does not need any additional circuit. This ability along with lower components and stress on the devices confirms that the proposed inverter can perform well in comparison with other existing ones.

TABLE I
Comparison Of Some Modular Multilevel Inverter Topology

	NPC	**FC**	**CHB**	**PROPOSED (E -Type)**
No. of switches	$2(N_L-1)$	$2(N_L-1)$	$2(N_L-1)$	$5(N_L-1)/6$
No. of Diodes	N_L+1	$2(N_L-1)$	$2(N_L-1)$	$5(N_L-1)/6$
No. of DC links	$(N_L-1)/2$	(N_L-1)	$(N_L-1)/2$	$(N_L-1)/3$
Negative level	With at least two arms	With at least two arms	With H bridge	Inherent

3. Methodology of proposed topology:

A general schematic diagram of a typicalasymmetrical multilevel inverter with two DC linksfordescription of multilevel operation is shown in Fig 2. Unequal DC links can bearranged with different connections (through switching components) in order to achieve high number of voltagelevels.

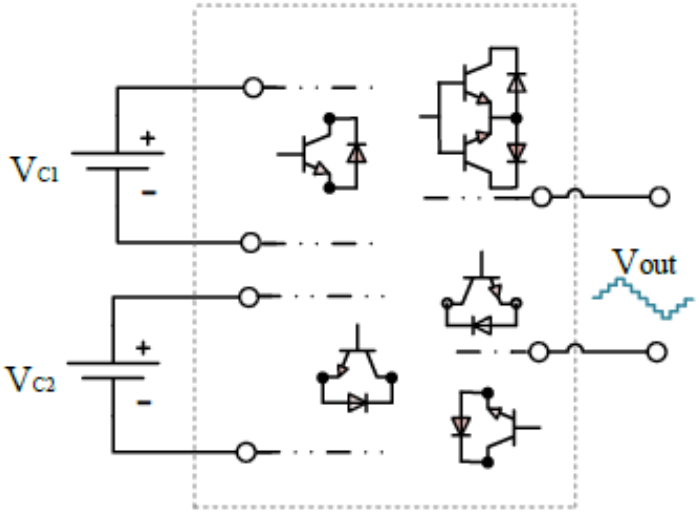
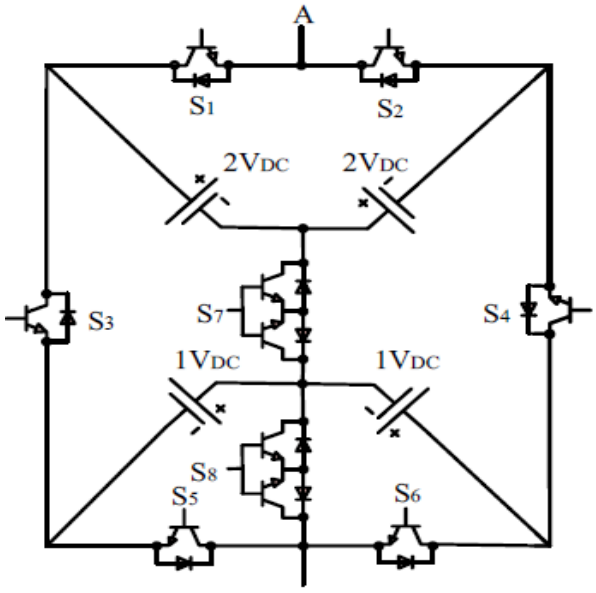


Fig.2 The general structure of asymmetric multilevel inverters

For example, assuming VC1=VDC and VC2=2VDC voltage levels of $\pm VDC$ ،$\pm 2VDC$ and $\pm 3VDC$ can be achieved by choosing suitable paths from switches and DC links depends on the module topology. Using this idea for multilevel inverters, a different ratio of DC link voltages may be utilized to generate a different number of output voltage levels. An elimination in harmonic content peak with a same switchingfrequency and the same structure is approximately expected by increasing the number of output voltage levels in the asymmetrical inverter.

Module Configuration

This proposed system introduces a new topology of asymmetric multilevel modular with a new component arrangement including 10 switches, 10 diodes and 4 unequal DC sources (two $2VDC$, two $1VDC$) named as Envelope type (E-Type). This arrangement synthesizes voltage sources produces 13 levels (6 positive level, 6 negative level and zero level) without any additional circuit. The main concept of this circuit is to create different paths from different sides of a DC source to be connected to other sources. Fig.4 shows the configuration of E-Type asymmetrical module in where DC sources are located in the middle of the circuit and are connected together to form different voltage levels via surrounding switch (S1-S6). A bidirectional switch (S7) is required to avoid short circuit of DC sources on left or right sides of the module. Another bidirectional switch (S8) is also needed to achieve voltage levels of ±5 . Different switching conditions of this structure are shown in Fig.3 and Table I.



(a)

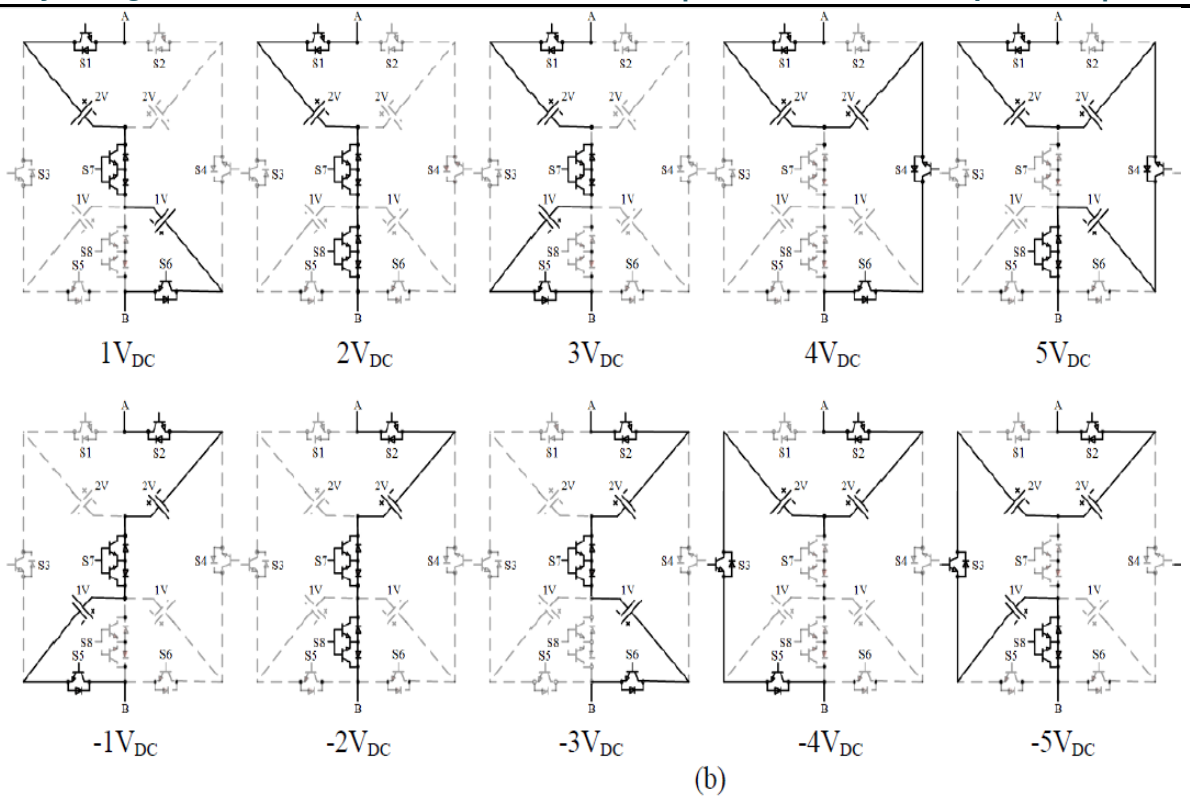


Fig. 3 Proposed E-Type module of multilevel inverter (a) Circuit topology (b) different switching states

TABLE II
SWITCHING TABLE

		S1	S2	S3	S4	S5	S6	S7	S8
positive level	$1V_{DC}$	1	0	0	0	0	1	1	0
	$2V_{DC}$	1	0	0	0	0	0	1	1
	$3V_{DC}$	1	0	0	0	1	0	1	0
	$4V_{DC}$	1	0	0	1	0	1	0	0
	$5V_{DC}$	1	0	0	1	0	0	0	1
	$6V_{DC}$	1	0	0	1	1	0	0	0
Negative level	$-1V_{DC}$	0	1	0	0	1	0	1	0
	$-2V_{DC}$	0	1	0	0	0	0	1	1
	$-3V_{DC}$	0	1	0	0	0	1	1	0
	$-4V_{DC}$	0	1	1	0	1	0	0	0
	$-5V_{DC}$	0	1	1	0	0	0	0	1
	$-6V_{DC}$	0	1	1	0	0	1	0	0

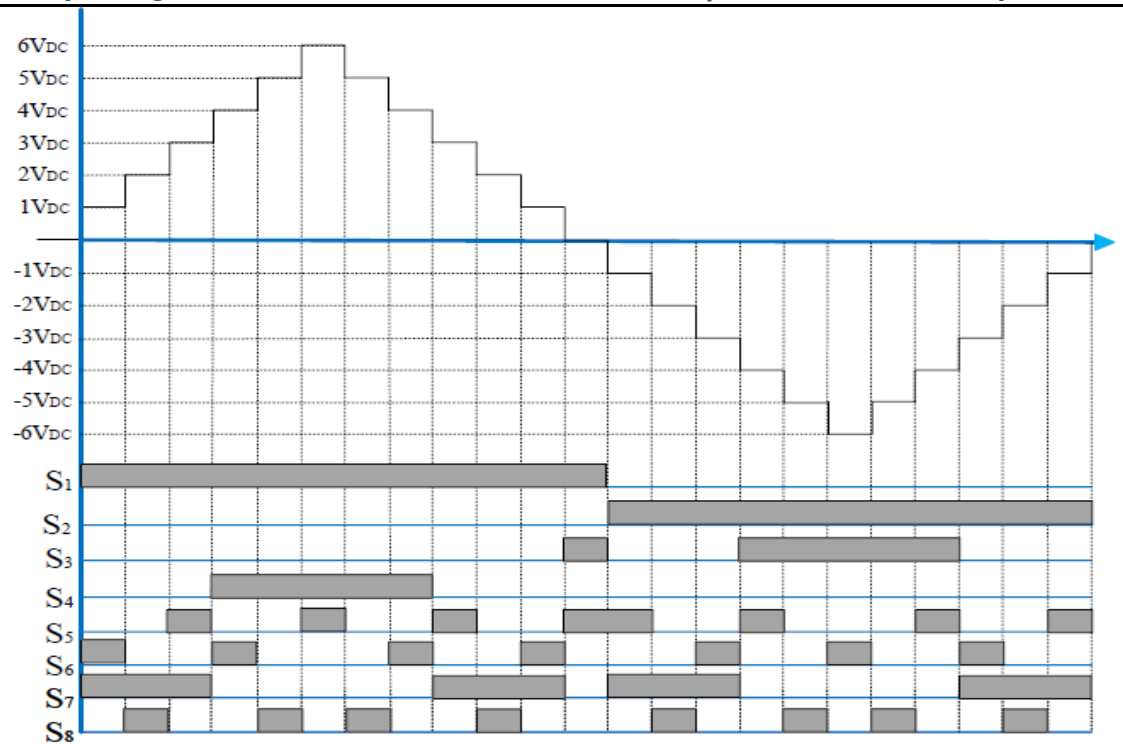


Fig.4 Switching Pattern Of Proposed Converter In One Cycle

As shown in Table II, switch pairs (S1, S4) and (S2, S3) belong to positive and negative levels, respectively. In addition, (S1, S2) and (S3, S4) cannot be on at the same time. Fig.4 shows output voltage of the proposed inverter with the associated pulse pattern in one cycle of fundamental voltage. As shown in Fig.4, switches S1, S2, S3, S4 and S7 are turned on and off in low frequency which reduces switching losses to a great extent. Other switches also operate in a reasonable switching frequency. Table II shows number of voltage levels, semiconductor components, DC sources and drivers based on number of module units (n) and number of desired levels (NL).

TABLE III
EQUATIONS OF E-TYPE MODULE

	Based on number of module units	**Based on number of desired levels**
Levels	12n+1	N_L
Number of switches	10n	$5(N_L-1)/6$
Number of Diodes	10n	$5(N_L-1)/6$
Driver	8n	$8(N_L-1)/6$
Number of DC Links	4n	$(N_L-1)/3$
TSV	20n	$10(N_L-1)/6$

Number of levels are in the form of 12n+1 (n=1, 2, 3, ….)

Fig.3(b) shows all switching states of E-type module. The designing of the proposed module and their switching paths are smartly selected in such a way that there are no positive pole of DC links on the anode side of diode to conduct. Thus, diodes prevent short circuiting of the switches. Also Fig.3(b) illustrates the switching paths does not form any close loop for DC links. It guarantees that short circuiting will be not occurred in E-type module.

Selective harmonic elimination modulation :Selective harmonic elimination modulation (SHE-PWM) method is utilized in this paper to create pulse pattern for the proposed inverter. In this method, as shown in Fig.6, different angles ($\alpha 1,...,6$) are calculated to form a staircase multilevel waveform with the lowest possible THD. The method is implemented based on optimization techniques where each desired harmonic order can be eliminated. Selection of switching angles for a multilevel converter is presented in using a phase-shift harmonic suppression approach. Generally, SHE-PWM is based on the Fourier series

decomposition of the periodic PWM voltage waveform and calculation of the switching angles (αi) in order to eliminate selected low harmonic orders. Fourier series of a periodic function can be written as:

$(t)=a02+\Sigma(ancos(2\pi ntT)+bnsin(2\pi ntT))\ nn=1$ (1)

As (t) is odd, the equation can be rewritten as:

$(t)=\Sigma(bnsin(2\pi ntT)\ )nn=1$ (2)

Where bn as follows, v is step level voltage:

$bn=4Vn\pi\Sigma sin(n\alpha i)ii=1$ (3)

For proposed topology, as shown in Fig.5, there are 6 voltage levels in a quarter-wave symmetry and therefore 6 switching angles (αi) have to be calculated. Third harmonic multiples are eliminated in three phase systems. Thus 9th and 15th harmonics are not considered in the equations. It helps to consider more harmonic components in equations for elimination (such as 17th and 19th instead of 9th and 15th). 3rd is just considered for its higher amount in equations in single phase systems to reduce THD%. To eliminate 3th, 5th, 7th, 11th, 13th, 17th and 19th harmonic orders, (4) have to be solved in order to achieve α1 to α6 with the condition of $0<\alpha1<\alpha2<\alpha3<\alpha4<\alpha5<\alpha6<\pi2$. Fig.8 illustrates switching angles for different modulation indexes (ma). Table V shows the results for the degree of each step level with ma= 0.98.

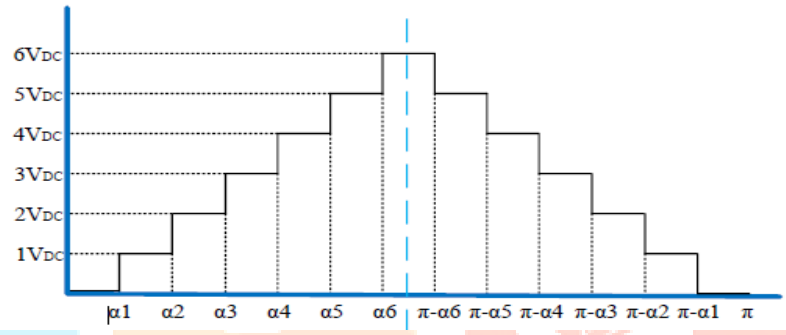


Fig.5Shows the waveform of Selective harmonic elimination modulation to find αi (Quarter wave symmetry)

4. SIMULATIONS RESULTS

The proposed multilevel module is simulated by MATLAB to examine the performance of proposed module. Fig.6shows the output voltage of 13-levels (Each level is 50 volts) for the proposed multilevel with SHE modulation switching method with THD% of 3.46%. It satisfied IEEE 519 (i.e. max. of THD%: 8%, max. of THD for each order: 5%).

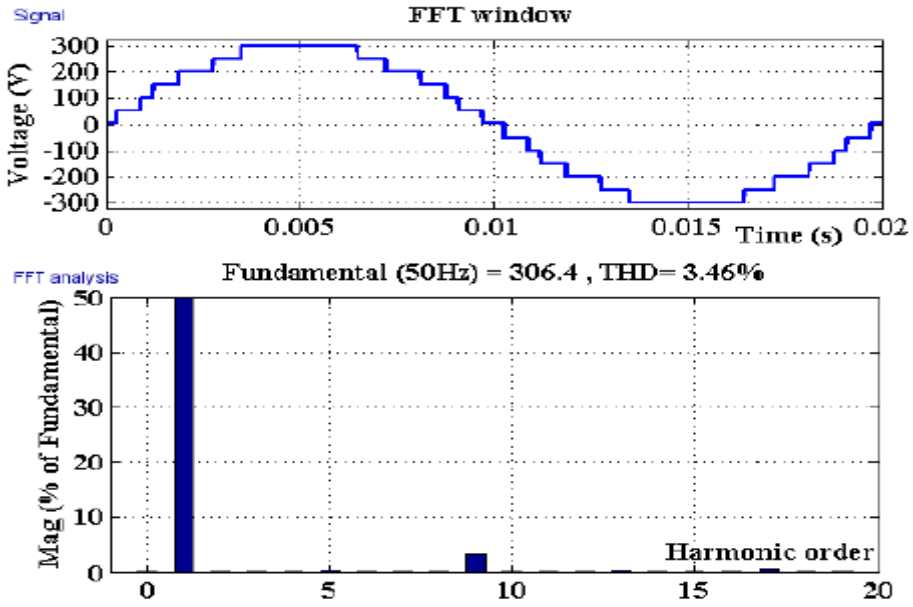


Fig.6 Output voltage and FFT analysis of proposed multilevel

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