DESIGN AND SIMULATION OF VEDIC MULTIPLIER USING VHDL CODE

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Abstract: This Paper is devoted for the design and analysis of high speed Vedic multiplier. In this paper the multiplier circuit is designed using Vedic mathematics. Vedic mathematics is a part of Indian ancient literature known as Vedas. There are four Vedas in which Atharva Veda consist sixteen magical sutras which are used in mathematical calculation. VHDL programs of this multipliers is synthesized using Xilinx 9.2i software and simulated using Xilinx ISE simulator.

The comparative study of Vedic multipliers is done with conventional multiplier for finding the efficient multiplier design to perform high speed operation of multiplication and it has been found that the Vedic multiplier is more efficient than conventional multiplier because it gives minimum delay for multiplication. The designed Vedic multiplier is based on "Urdhva-tiryakbhyam" algorithm or sutra of ancient Indian Vedic mathematics. It is one of the sixteen sutras of Vedic mathematics. Vedic mathematics sutra "Urdhva-tiryakbhyam" increases the speed of multiplier by reducing the number of partial products. Hence the speed of overall system or processor can be increased by designing high speed Vedic multiplier.

Keywords **- VHDL, Vedic multiplier, Urdhva-tiryakbhyam sutra, SOP, POS, ISE.**

I. INTRODUCTION

In arithmetic operation Multiplication is an important fundamental function. The operations which are based on Multiplication takes more time than addition and subtraction, hence if we increase the speed of multiplication operation then we can also increase the speed of calculations of operations which are based on Multiplication. There are so many operations which are based on multiplication like Multiply and Accumulate (MAC) and computation intensive arithmetic function (CIAF) , convolution, FFT, filtering and in microprocessor & microcontroller's arithmetic and logical unit. There is always a need of high speed multiplier because it dominates the execution time of most DSP algorithm. The application area of computer is expanding day by day, so the need of high speed multiplier to increase the speed of the whole system is basic requirement of the system [1].

In Vedic times when there are no calculators and computers were present to calculate the data values, the ancient Guru's were used some techniques or methods for their calculations, now that techniques are known as Vedic calculations. Vedic techniques are very fast and logical. The Vedic mathematics approach is totally different and considered very close to the way a human mind thinks and works.

It is also proved by many publications that the Vedic algorithms are very useful in designing digital multiplier to reduce calculation time or to increase the speed of multiplier.. Vedic multiplier makes the calculation of data very fast as compared to simple multiplier for complex multiplication. The conventional multiplication method generates partial products to produce output, in the technique of Vedic multiplier the number of partial products generated is less, hence the speed is high [2].

For any multiplier circuit or system, the basic requirements are it should consume less power and contain smaller area. So optimizing the area and speed of multiplier is a major task. The multiplier is a slowest component in any system; hence if we decrease the calculation time of multiplier then we can increase the performance of overall system. As we know the number of partial products is less in Vedic multiplier than the power requirement of the system is also less as compare to conventional multiplier. There are different types of multipliers are available depending upon the arrangement of components used during the design of the multiplier. According to power, area and speed we can choose the best architecture for our application.

The term Vedic Mathematics comes from VEDAS. According to Hindu Methodology the Vedas are a collection of hymes and other ancient religious texts written in India. The Vedas includes poems, prayers, formulas, liturgical material and mythological accounts. There are four Vedas are present, and they are as follows:

- Rig-Vedic: "Knowledge of the songs of praise of god", for Recitation
- Sama-Veda: "Knowledge of the Music", for Chanting
- Yajur-Veda: "Knowledge of the prose Mantras", for worship
- Atharva-Veda: "Knowledge of the Magic formulas" for Mathematical Calculation.

The origin of Vedic Mathematics is Athrva Veda and this collection of magic formulas is rediscovered by Shri Bharthi Krishna Tirthaji Maharaj in between 1911 to 1918. The name given to this set of formulas (Vedic Mathematics) is based on their origin i.e. Vedas. According to Tirthaji Maharaj, the Vedic mathematics consists of sixteen formulas, which are intended to describe the way the mind naturally works. Complex arithmetic problems and difficult calculations can often be solved immediately by the use of these sixteen formulas. Many Research work is being carried out on Vedic mathematics sutra's applications in mathematical calculations and it has proved that this formulas are very helpful to increase the speed of processor, which is responsible for mathematical calculations [3].

The applications of Vedic mathematics formulas and sutras almost cover all the branches of mathematics. The mathematical calculations like Addition, Subtraction, Multiplication, Division, Squaring, Cubing etc. of complex numbers can be made very easy and interesting with the help of Vedic mathematics formulas because this formula uses mental ability and pattern to perform calculation. So it is the power of Vedic mathematics that it can converts a tedious subject into a playful and blissful one.

All the sixteen sutras rediscovered by Tirthaji Maharaj from Vedas are listed below along with their meanings:

- Nikhilam Navtascaramam Dastah : All from nine and last from ten
- Ekadhikina Purvena : By one more than the previous one
- Urdhva Tiryagbhyam : Vertically and crosswise
- Paravartya Yojayet : Transpose and adjust
- Sunyam Samyasamuccye : When the sum is the same, that sum is zero
- Sunyanmanyat or Anurupye : If one is in ratio, the other one is zero
- Sankalana Vyavakalanabhyam : By subtraction and addition
- Puranapuranabhyam : By non-completion or completion
- Calana kalanabhyam : Similarities and non similatities
- Yavadunam : Whatever the extent of its deficiency
- Vyastisamastih : Use the averages
- Sesanyankena Caramena : The remainders by the penultimate
- Sopantyadvayamantyam : The ultimate and twice the penultimate
- Ekanyunena Purvena : By one less than the previous
- Gunitasamuccayah : The POS is equal to the SOP
- Gunakasamuccayah : The factors of the sum is equal to the sum of factors

The above mentioned sixteen sutras are covers almost every branch of mathematics. Applications of these sutras in mathematical calculation save a lot of time and effort. There are so many sub-sutras are also discovered but are not discussed here. From above mentioned sixteen sutras I am going to use only Urdhva-tiryakbhyam sutra to design Vedic multiplier. According to the pattern used in multiplication by Urdhva-tiryagbhyam sutra, it is also known as vertically and crosswise. Out of sixteen sutras presented above five sutras can be used to perform multiplication operation namely Nilhilam sutra, Anurupyena sutra, Urdhva-tiryakbhyam sutra, Ekanyunena Purvena sutra and Antyayoreva sub-sutra. All the sutras have their own application areas where they can be used to perform calculation in less time [4].

II. METHODOLOGY

Urdhva-tiryakbhyam sutra is General method of multiplication in Vedic mathematics which takes less time to perform multiplication operation to multiply any types of numbers. Nikhilam sutra of Vedic mathematics is applicable in some special cases of multiplication, but Urdhva tiryagbhyam sutra in applicable to do all cases of multiplication. The pattern used in Urdhva tiryagbhyam sutra is Vertically and Cross-wise.

The application of Urdhva-tiryagbhyam sutra for multiplying two numbers consisting 2 digit, 4 digit and 8 digits are described as follows:

MULTIPLICATION OF TWO-DIGIT NUMBER:

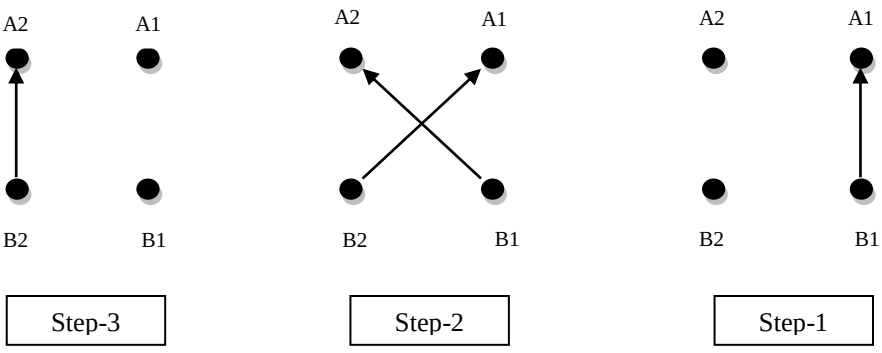
Formula Used: (x=10)
First Number => A_2A_1
Second Number => B_2B_1

$$(A_2x + A_1)(B_2x + B_1) = A_2B_2x^2 + (A_2B_1 + A_1B_2)x + A_1B_1$$

Process (Right to Left):

- Vertical Multiplication of last digits of both the numbers.
- Crosswise Multiplication of digits of both numbers and adding them.
- Vertical Multiplication of First digits of both numbers

2×2 Vedic Multiplier

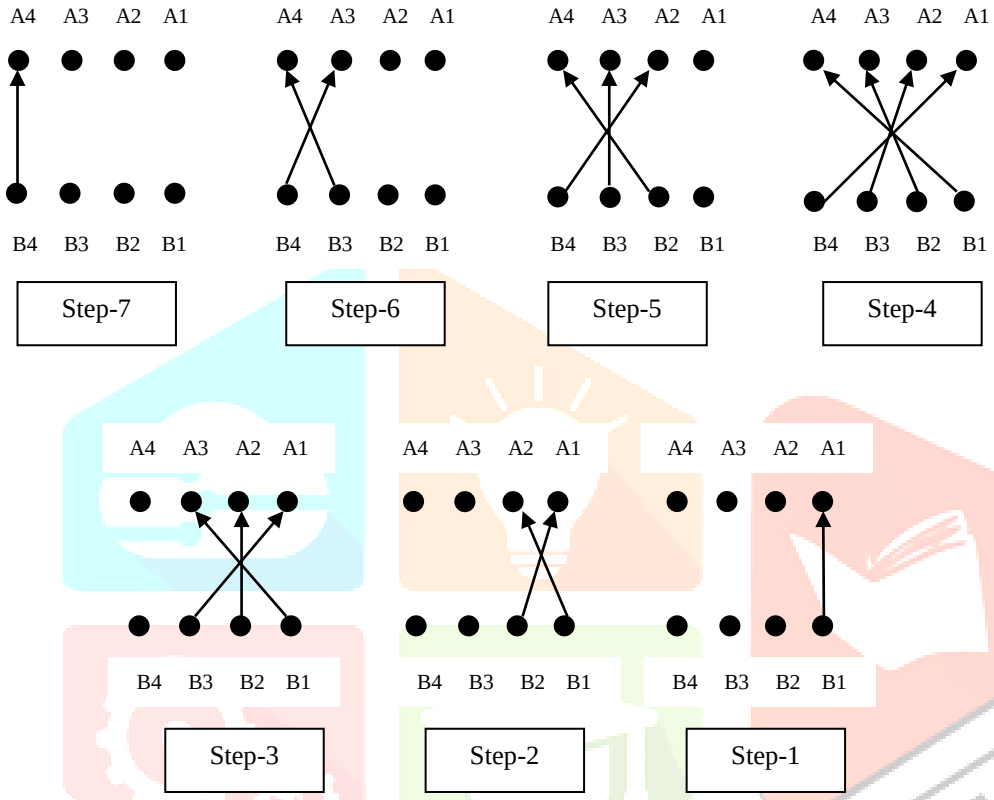


MULTIPLICATION OF FOUR-DIGIT NUMBER:

Formula Used: (x=10)
First number => $A_4A_3A_2A_1$
Second number => $B_4B_3B_2B_1$

$$(A_4x^3 + A_3x^2 + A_2x + A_1)(B_4x^3 + B_3x^2 + B_2x + B_1)$$
$$= A_4B_4x^6 + (A_4B_3 + A_3B_4)x^5 + (A_4B_2 + A_3B_3 + A_2B_4)x^4 + (A_4B_1 + A_3B_2 + A_2B_3 + A_1B_4)x^3$$
$$+ (A_3B_1 + A_2B_2 + A_1B_3)x^2 + (A_2B_1 + A_1B_2)x + A_1B_1$$

4×4 Vedic Multiplier



III. IMPLEMENTATION AND SYNTHESIS

The proposed 8-bit Vedic multipliers is designed using VHDL coding using Urdhva-tiryagbhyam sutra.. The simulation results and input & output waveforms are for Vedic multipliers is as follows:

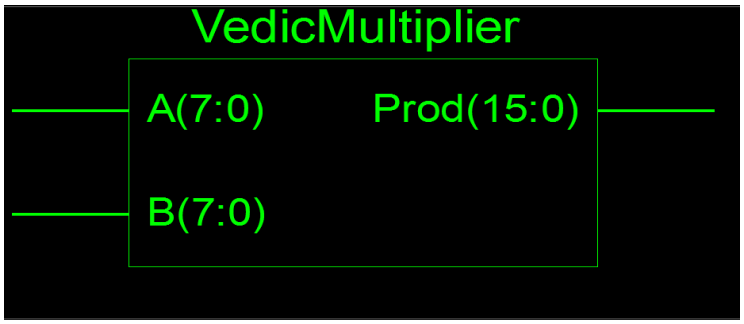


Figure 1: Block Diagram of Vedic Multiplier

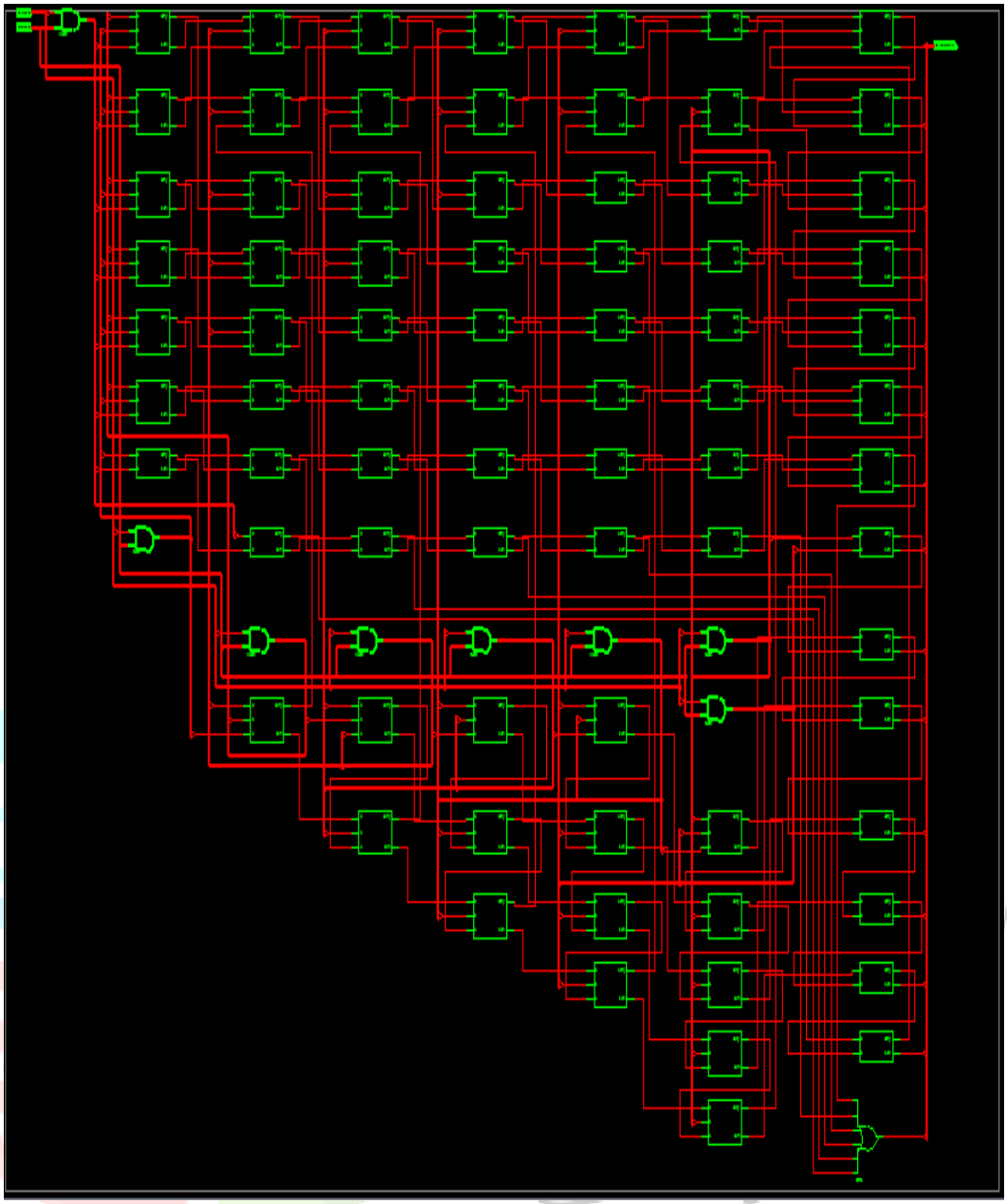
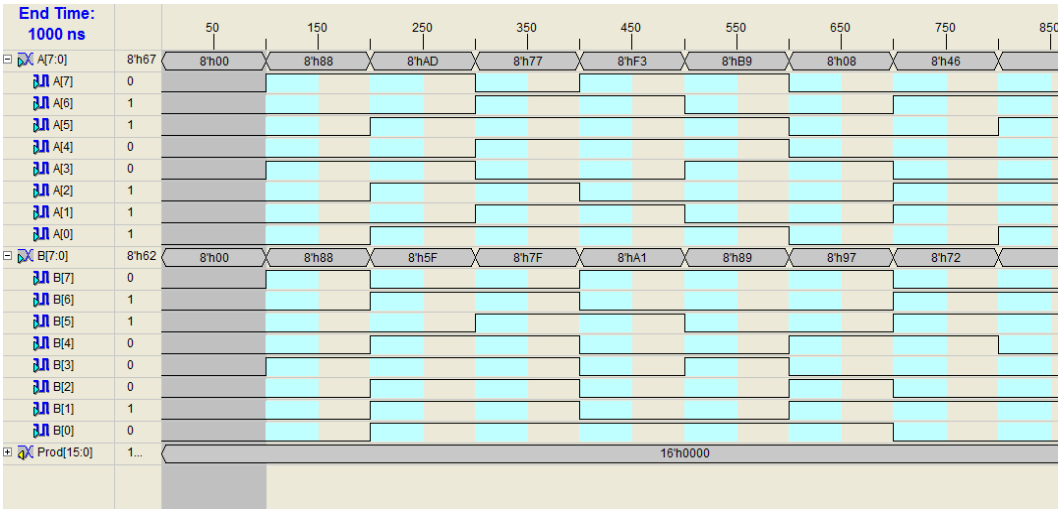
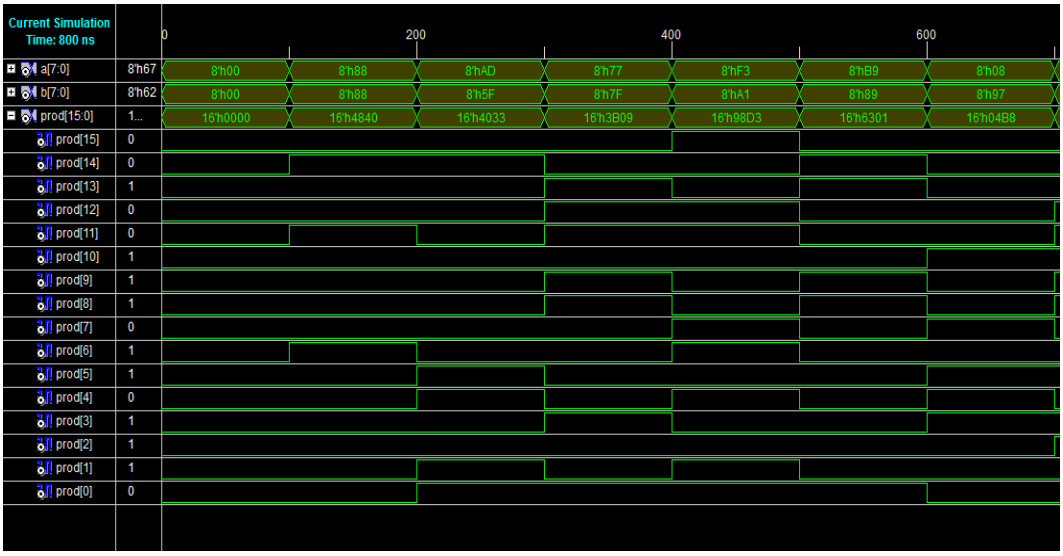


Figure 2: RTL view of Vedic Multiplier



Waveform 1 : TBW input of Vedic Multiplier



Waveform 2 : TBW output of Vedic Multiplier

IV. SIMULATION RESULTS

VEDICMULTIPLIER Project Status			
Project File:	VedicMultiplier.ise	Current State:	Synthesized
Module Name:	VedicMultiplier	• Errors:	No Errors
Target Device:	xc3s200-5ft256	• Warnings:	No Warnings
Product Version:	ISE 9.2i	• Updated:	Tue Apr 10 14:54:54 2018

VEDICMULTIPLIER Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	91	1920	4%
Number of 4 input LUTs	159	3840	4%
Number of bonded IOBs	32	173	18%

Figure 3: Design Summary of Vedic Multiplier

Number of Slices	91 out of 1920
Number of 4 input LUTs	159 out of 3840
Number of IOs	32
Number of bounded IOBs	32 out of 173
Maximum combinational path delay	28.351 ns
Total Memory usage	177872 Kilobytes
Number of Errors	0
Number of Warnings	0

Table 1: Vedic Multiplier Summary

V. CONCLUSION

. The designs of 8*8 multipliers have been successfully simulated using Xilinx 9.2i software for Vedic multiplier. The Vedic multiplier is based on Urdhva-tiryakbhyam sutra of Vedic Mathematics. It is shown that the maximum combinational path delay for 8*8 bit Vedic multipliers is 28.351 ns. The proposed multiplier is designed using the array of half adders and full adders, which are used to generate addition of partial factors.

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