

# PFC Zeta Converter Fed BLDC Motor Drive for Fan Applications

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**Abstract :** A Zeta converter fed BLDC motor drive using a single voltage sensor is proposed for fan applications. A single phase supply followed by diode bridge rectifier and a Zeta converter is used to control the voltage fed to the VSI. Output of Zeta converter is controlled to achieve the speed control of BLDC motor. A sensorless control of BLDC motor is used to eliminate the requirement of position sensors. A MATLAB Simulation is used to simulate the developed model to achieve a wide range of speed control with high Power Factor and improved Power Quality at the supply.

**IndexTerms -** BLDC motor, Sensorless, Voltage Control, VSI, Zeta,PFC.

## I. INTRODUCTION

SOLID-STATE ac-dc conversion of electric power is widely used in adjustable-speed drives (ASDs), switch-mode power supplies (SMPSs), uninterrupted power supplies (UPSs), and utility interface with nonconventional energy sources such as solar PV, etc., battery energy storage systems (BESSs), in process technology such as electroplating, welding units, etc., battery charging for electric vehicles, and power supplies for telecommunication systems, measurement and test equipments. Conventionally, ac-dc converters, which are also called rectifiers, are developed using diodes and thyristors to provide controlled and uncontrolled dc power with unidirectional and bidirectional power flow. They have the demerits of poor power quality in terms of injected current harmonics, caused voltage distortion and poor power factor at input ac mains and slow varying rippled dc output at load end, low efficiency and large size of ac and dc filters.

The requirement of improved power quality at the AC mains is becoming essential for any appliance as imposed by the International PQ (Power Quality) standards like IEC 61000-3-2 [1]. The requirement of power factor above 0.9 and THD (Total Harmonic Distortion) below 5% for Class-D (under 600 W, <16 A, single phase) applications recommends the use of improved power quality converters for BLDC (Brush Less DC) motor drive. There are many AC-DC converters topologies reported in the literature to meet the recommended PQ standards [2]. BLDC motor when fed by an uncontrolled bridge rectifier with DC link capacitor results in highly distorted supply current which results in low PF (Power Factor) and high THD (Total Harmonic Distortion); hence various improved power quality AC-DC converters are used in these drives. BLDC motor is an ideal motor for low-medium power applications because of its high efficiency, high torque/inertia ratio, low maintenance and wide range of speed control [3-6]. It consists of three phase windings on the stator and permanent magnets on the rotor. Being an electronically commutated motor, the commutation losses in the BLDC motor are negligible.

Two stage PFC converters are widely in practice in which first stage is used for the power factor correction which is preferably a boost converter and second stage for voltage regulation which can be any converter topology depending upon the requirement [7]. This two stage topology is complex and results in higher cost and more losses; hence a single stage Zeta converter is proposed in this paper which is used for DC link voltage control and power factor correction. The operation is studied for a Zeta converter working in DICM (Discontinuous Inductor Current Mode) hence a voltage follower approach is used.

## II. PROPOSED CONTROLLED SCHEME

The proposed scheme for the Sensorless BLDC motor drive fed by a Zeta based PFC converter operating in DICM mode is shown in Fig. 1. The front end Zeta DC-DC converter maintains the DC link voltage to a set reference value. Switch of the Zeta converter is to be operated at high switching frequency for effective control and small size of components like inductors. A sensorless approach is used to detect the rotor position for electronic commutation. A high frequency MOSFET of suitable rating is used in the front end converter for its high frequency operation whereas an IGBT's (Insulated Gate Bipolar Transistor) are used in the VSI for low frequency operation.

The proposed scheme maintains high power factor and low THD of the AC source current while controlling rotor speed equal to the set reference speed. A voltage follower approach is used for the control of Zeta DC-DC converter operating in DICM.

The DC link voltage is controlled by a single voltage sensor.  $V_{dc}$  (sensed DC link voltage) is compared with  $V_{dc}^*$  (reference voltage) to generate an error signal which is the difference of  $V_{dc}^*$  and  $V_{dc}$ . The error signal is given to a PI (Proportional Integral) controller to give a controlled output. Finally, the controlled output is compared with the high frequency saw tooth signal to generate PWM (Pulse Width Modulation) pulse for the MOSFET of the Zeta converter.

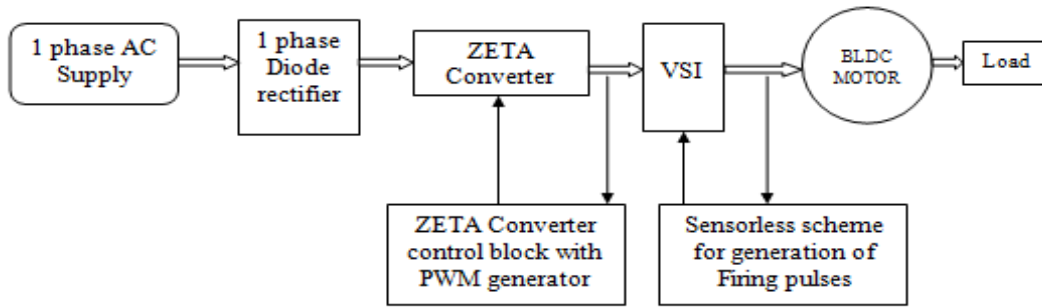


Fig. 1. Proposed Zeta converter fed Sensor-less BLDC MOTOR drive

**III. ZETA CONVERTER**

Similar to the SEPIC DC/DC converter topology, the ZETA converter topology provides a positive output voltage from an input voltage that varies above and below the output voltage. The ZETA converter also needs two inductors and a series capacitor, sometimes called a flying capacitor. Unlike the SEPIC converter, which is configured with a standard boost converter, the ZETA converter is configured from a buck controller that drives a high-side PMOS FET. The ZETA converter is another option for regulating an unregulated input-power supply, like a low-cost wall wart. To minimize board space, a coupled inductor can be used. This article explains how to design a ZETA converter running in continuous-conduction mode (CCM) with a coupled inductor. Like the SEPIC converter, the ZETA converter is another converter topology to provide a regulated output voltage from an input voltage that varies above and below the output voltage. The benefits of the ZETA converter over the SEPIC converter include lower output-voltage ripple and easier compensation. The drawbacks are the requirements for a higher input-voltage ripple, a much larger flying capacitor, and a buck controller (like the TPS40200) capable of driving a high side PMOS.

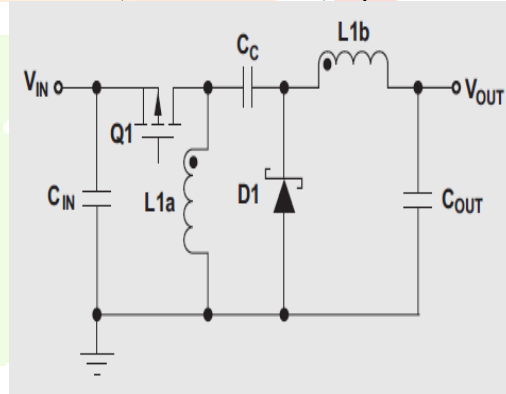


Fig. 2. Basic circuit for Zeta converter

**IV. DESIGN OF PFC ZETA CONVERTER**

The proposed drive system is designed for Zeta converter as PFC converter fed BLDC motor drive operating in DICM. The output inductor value is selected such that the current remains discontinuous in a single switching cycle as shown in Fig. 2. The average input voltage  $V_{in}$  after the rectifier is given as [7],

$$V_{in} = 2 * 1.414 * V_s / \pi \tag{1}$$

Where  $V_s$  is the rms value of the supply voltage.

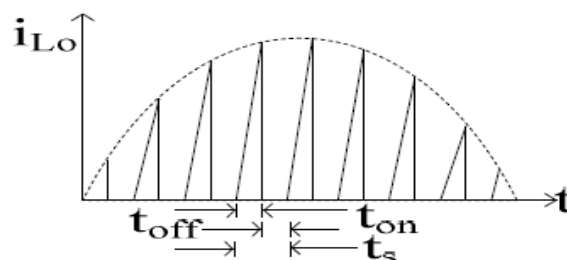


Fig. 3. Waveform of output inductor current in DICM control

The duty ratio D for the Zeta converter (buck-boost) is given as [7],

$$D = V_{dc} / (V_{in} + V_{dc}) \tag{2}$$

where  $V_{dc}$  represents the DC link voltage of Zeta converter. If the permitted ripple of current in input inductor  $L_i$  and output inductor  $L_o$  is given as  $\Delta i_{L_i}$  and  $\Delta i_{L_o}$  respectively, then the inductor value  $L_i$  and  $L_o$  are given as [8-11],

$$L_i = D.V_{in} / \{f_s.(\Delta i_{L_i})\} \tag{3}$$

$$L_o = (1-D) V_{dc} / \{f_s.(\Delta i_{L_o})\} \tag{4}$$

where  $f_s$  is the switching frequency. For the critical conduction mode,  $\Delta i_{L_o} = 2.I_{dc}$

$$\text{i.e. } L_o(\text{critical}) = (1-D) V_{dc} / \{f_s. (2.I_{dc})\} \tag{5}$$

The value of intermediate capacitor  $C_1$  is given as [8-11],

$$C_1 = D.I_{dc} / \{f_s. (\Delta V_{C_1})\} \tag{6}$$

where  $\Delta V_{C_1}$  is the permitted ripple in  $C_1$ . The value of DC link capacitor  $C_d$  is given as [8-11],

$$C_d = I_{dc} / (2. \omega. \Delta V_{dc}) \tag{7}$$

where  $\omega = 2\pi f_L$ ;  $f_L$  is the line frequency. Equations (1)-(7) represent the design criteria of the Zeta converter in discontinuous conduction mode.

A PFC converter of rating 500W is designed for operating at 50-200V at source voltage  $V_S = 220V$  for switching frequency of 45 kHz. The ripple in input inductor ( $\Delta i_{L_i}$ ) current is considered to be 10% and ripple in DC link voltage ( $\Delta V_{dc}$ ) as 4%. The design values thus obtained are  $L_i = 2.463 \text{ mH}$ ,  $L_o = 60 \mu\text{H}$ ,  $C_1 = 330 \text{ nF}$  and  $C_d = 2500 \mu\text{F}$ . The simulation diagram is shown in fig. 4.

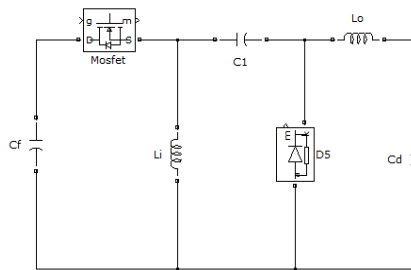


Fig. 3. Basic circuit for Zeta converter

### V. CONTROL OF PFC BASED ZETA FED SENSORLESS BLDC MOTOR DRIVE

The PFC converter and the sensorless BLDC motor drive are modeled for the proposed drive scheme. The control scheme of the PFC converter consists of following three blocks.

#### 5.1. Reference Voltage Generator

The speed of BLDC motor is proportional to the DC link voltage of the VSI, hence a reference voltage generator is required to produce an equivalent voltage corresponding to the particular reference speed of the BLDC motor. The reference voltage generator produces a voltage by multiplying the speed with a constant value known as the voltage constant ( $K_b$ ) of the BLDC motor.

#### 5.2. Speed Controller

An error of the  $V_{dc}^*$  and  $V_{dc}$  is given to a PI (Proportional Integral) speed controller which generates a controlled output corresponding to the error signal. The error voltage  $V_e$  at any instant of time  $k$  is as;

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k) \tag{8}$$

and the output  $V_c(k)$  of the PI controller is given by,

$$V_c(k) = V_c(k-1) + K_p.(V_e(k) - V_e(k-1)) + K_i.V_e(k) \tag{9}$$

where  $K_p$  is the proportional gain and  $K_i$  is the integral gain constant

### 5.3. PWM Generator

The output of the PI controller  $V_c$  is given to the PWM generator which produces a PWM signal of fixed frequency and varying duty ratio. A saw tooth waveform is compared with the output of PI controller as shown in Fig. 3 and PWM is generated as; If  $m_d(t) < V_c(t)$  then  $S=1$  else  $S=0$  (10) where  $S$  denotes the switching signals as 1 and 0 for MOSFET to switch on and off respectively.

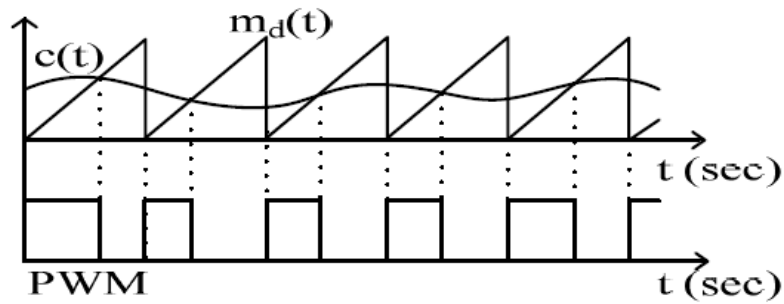


Fig. 4. Generation of PWM signal by comparing a saw tooth waveform with the controller output

The simulation diagram is as shown in fig. 5

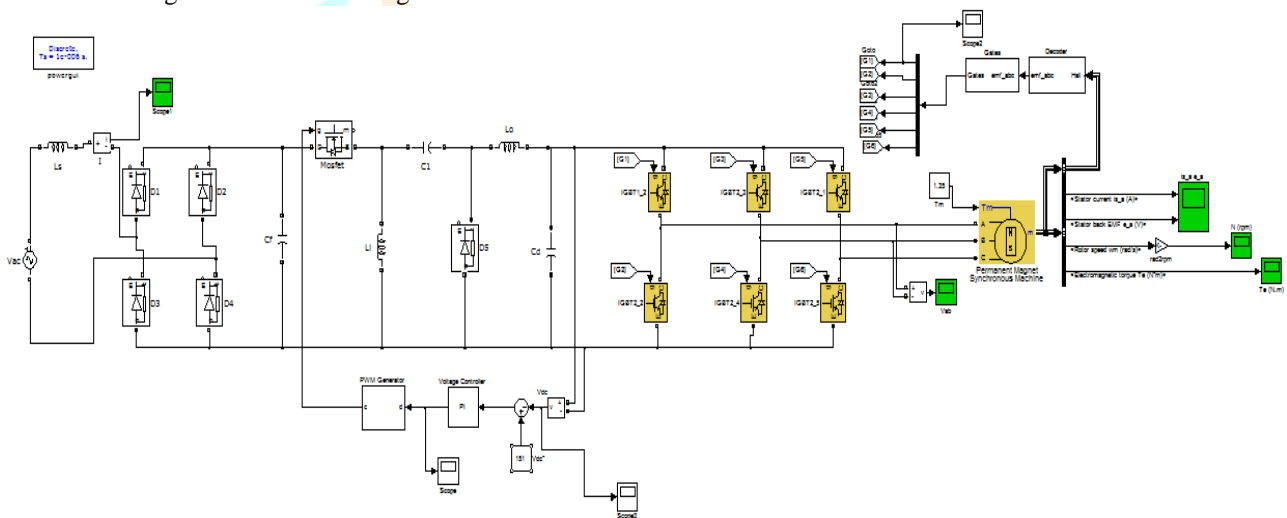


Fig. 5. Simulation Diagram for Zeta converter fed BLDC Motor Drive

## VI. RESULTS AND DISCUSSION

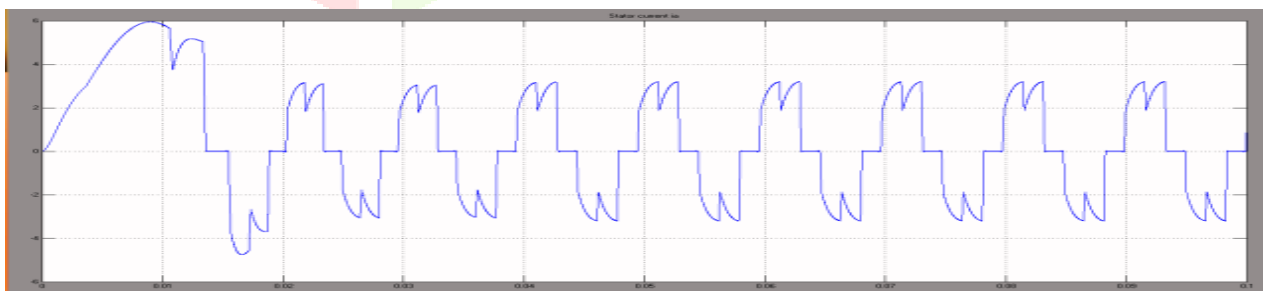


Fig. 6. Stator Current

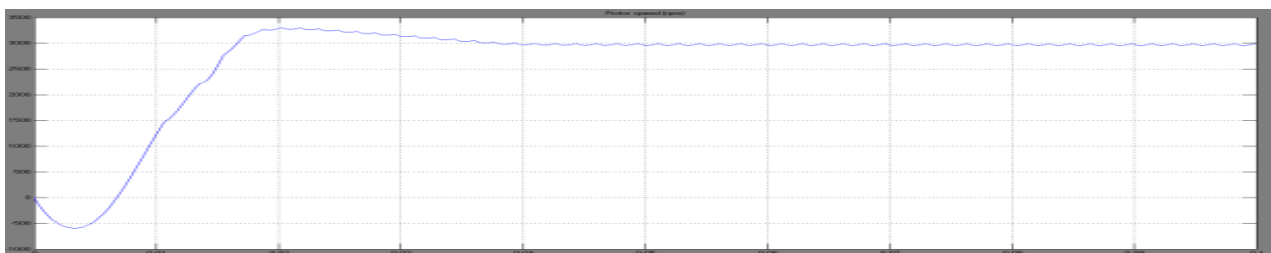


Fig. 7. Speed in RPM

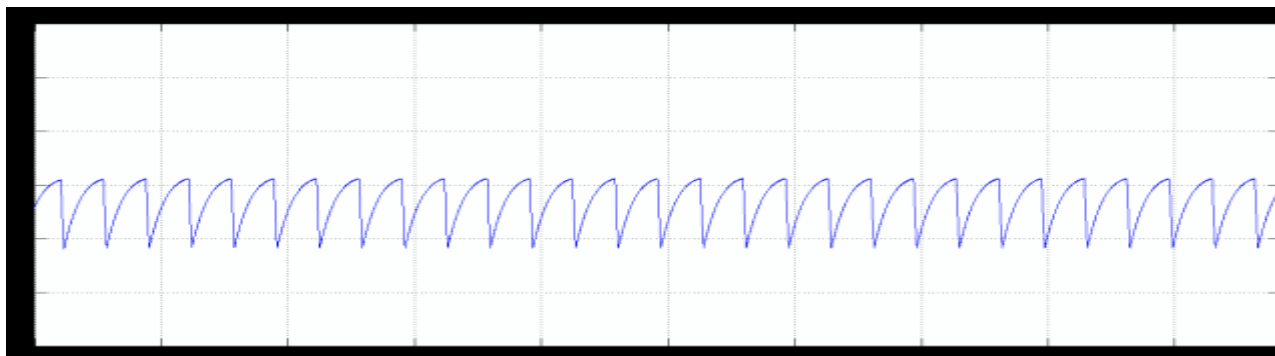


Fig. 8. Electromagnetic Torque

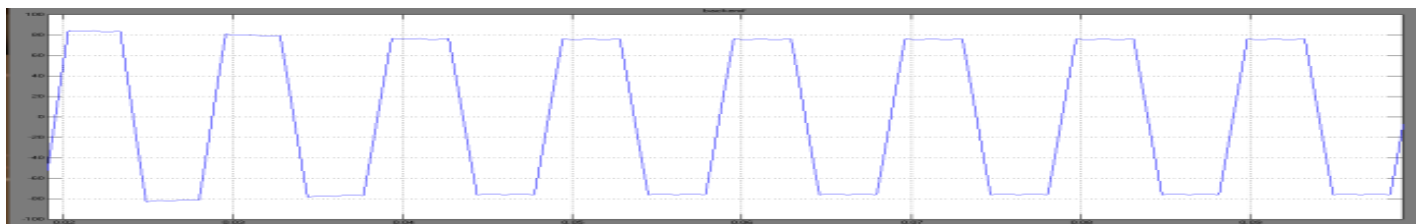


Fig. 9. Back EMF

A simple control using a voltage follower approach has been used for voltage control and power factor correction of a PFC Zeta converter fed BLDC motor drive. A novel scheme of speed control using a single voltage sensor has been proposed for a fan load. A sensorless operation for the further reduction of position sensor has been used. A single stage PFC converter system has been designed and validated for the speed control with improved power quality at the AC mains for a wide range of speed. The performance of the proposed drive system has also been evaluated for varying input AC voltages and found satisfactory. The power quality indices for the speed control and supply voltage variation have been obtained within the limits by International power quality standard IEC 61000-3-2. The proposed drive system has been found a suitable candidate among various adjustable speed drives for many low power applications

Table 1 BLDC MOTOR RATING

BLDC MOTOR RATING			
Parameters	Values	Parameters	Values
Pole	4	Prated (Rated Power)	424.11W
Trated (Rated Torque)	1.35 Nm	ωrated (Rated Speed)	3000 r.p.m
(Back EMF Constant)	51 V/krpm	Kt (Torque Constant)	0.49 Nm/A
Rph(Phase Resistance)	7.20Ω	L (Phase Inductance)	4.77 mH
J (Moment of Inertia)	0.37kg-cm2.		

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