DESIGN OF 4:2 COMPRESSORS FOR UTILIZING IN MULTIPLIER ARCHITECTURE FOR LOW POWER

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Abstract : Multiplication is one of the important operations in many signal processing and image processing applications. The performance of the multiplier has a direct effect on the final output of these applications. Due to this, there is always a need to design a multiplier with high speed and low power consumption. Accuracy is a term relative to the application. In our work, we have designed 6 different types of compressors, which were implemented in an 8 bit Dadda Multiplier evaluated in 45nm technology. The compressors are 4:2 Compressor, Exact Compressor and four approximate compressors, namely DQ4:2C1, DQ4:2C2, DQ4:2C3 and DQ4:2C4, with different levels of accuracy. The results have shown that the DQ4:2C3 compressor has the lowest power consumption among all.

Index Terms **- Compressors, Dadda Multiplier, Accuracy, Power.**

I. INTRODUCTION

Among different arithmetic blocks, the multiplier is one of the main blocks, which is widely used in different applications especially signal processing applications. There are two general architectures for the multipliers, which are sequential and parallel. While sequential architectures are low power. On the other hand, parallel architectures (such as Wallace tree and Dadda are fast while having high-power consumptions. The parallel multipliers are used in high-performance applications where their large power consumptions may create hot-spot locations on the die. Since the power consumption is a critical parameter in the design of digital circuits, the optimizations of these parameters for multipliers become critically important. Very often, the optimization of one parameter is performed considering a constraint for the other parameter. Specifically, achieving the limited power budget of portable systems is challenging task.

II. PROPOSED 4:2 COMPRESSORS

In this section, first, the details of an exact compressor are discussed. Next, the overall structures and the details of the suggested dual-quality approximate compressors are described.

A. Exact 4:2 Compressor

To reduce the delay of the partial product summation stage of parallel multipliers, 4:2 and 5:2 compressors are widely employed . Some compressor structures, which have been optimized for one or more design parameters (e.g., delay, area, or power consumption), have been proposed . The focus of this paper is on approximate 4:2 compressors. First, some background on the exact 4:2 compressor is presented. This type of compressor, shown schematically in Fig. 1, has four inputs (*x*1–*x*4*)* along with an input carry (*C*in*)*, and two outputs (*sum* and *carry*) along with an output *C*out. The internal structure of an exact 4:2 compressor is composed of two serially connected full adders, as shown in Fig. 2. In this structure, the weights of all the inputs and the s*um* output are the same whereas the weights of the *carry* and *C*out outputs are one binary bit position higher. The outputs *sum*, *carry*, and *C*out are obtained from

$$sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin \quad (1)$$

$$carry = (x1 \oplus x2 \oplus x3 \oplus x4)Cin + (x1 \oplus x2 \oplus x3 \oplus x4)x4 \quad (2)$$

$$Cout = (x1 \oplus x2)x3 + (x1 \oplus x2)x1. \quad (3)$$

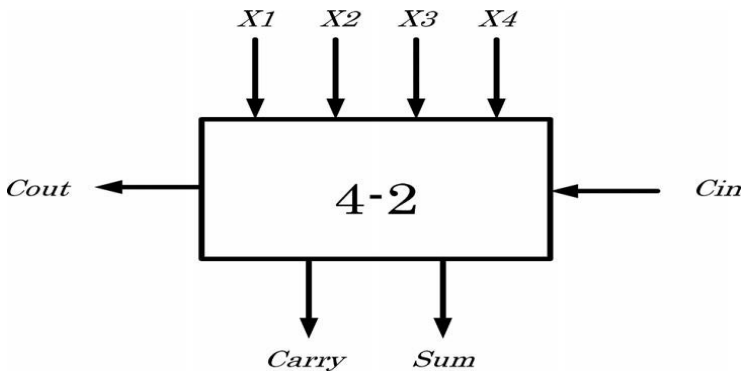

Fig.1 Block diagram of 4:2 compressor

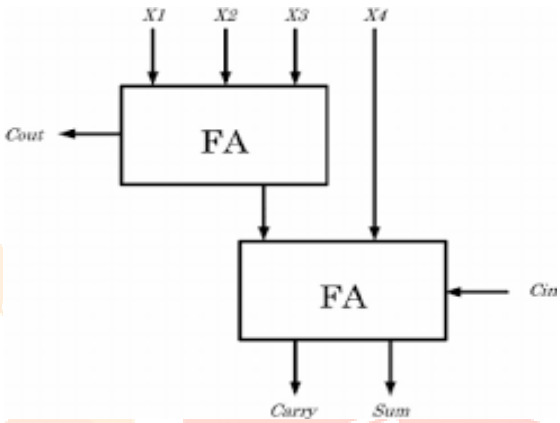

Fig.2 Structure of the conventional 4:2 compressor

B. Proposed Dual-Quality 4:2 Compressors:

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors is shown in Fig. 3. The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized. In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, as is evident from Fig. 3, in the exact operating mode, tristate buffers are utilized to disconnect the outputs of the approximate part from the primary outputs. In this design, the switching between the approximate and exact operating modes is fast. Thus, it provides us with the opportunity of designing parallel multipliers that are capable of switching between different accuracy levels during the runtime. Next, we discuss the details of our four DQ4:2Cs based on the diagram shown in Fig. 3. The structures have different accuracies, delays, power consumptions, and area usages. Note that the *i* th proposed structure is denoted by DQ4:2C*i* . The basic idea behind suggesting the approximate compressors was to minimize the difference (error) between the outputs of exact and approximate ones. Therefore, in order to choose the proper approximate designs for the compressors, an extensive search was performed.

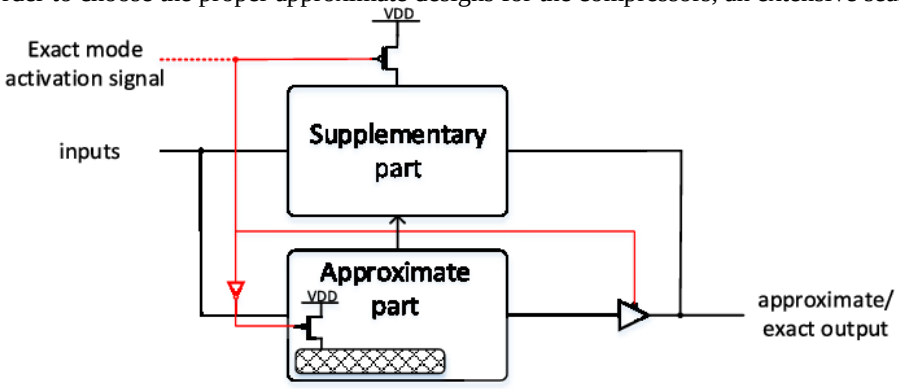

Fig. 3. Block diagram of the proposed approximate 4:2 compressors. The hachured box in the approximate part indicates the components, which are not shared between this and supplementary parts.

1) Structure 1 (DQ4:2C1): For the approximate part of the first proposed DQ4:2C structure, as shown in Fig. 4(a), the approximate output carry (i.e., *carry_*) is directly connected to the input *x*4 (*carry_* = *x*4*)*, and also, in a similar approach, the

approximate output sum (i.e., *sum_*) is directly connected to Fig. 5. (a) Approximate part and (b) overall structure of DQ4:2C2. input *x*1 (*sum_ = x*1*)*. In the approximate part of this structure, the output *C*out is ignored. While the approximate part of this structure is considerably having low power. The supplementary part of this structure is an exact 4:2 compressor. The overall structure of the proposed structure is shown in Fig. 4(b). In the exact operating mode, the delay of this structure is about the same as that of the exact 4:2 compressor.

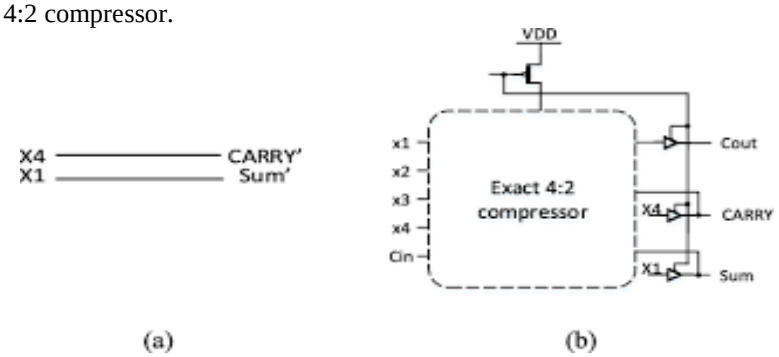

Fig. 4. (a) Approximate part and (b) overall structure of DQ4:2C1.

2) Structure 2 (DQ4:2C2): In the first structure, while ignoring *C*out simplified the internal structure of the reduction stage of the multiplication, its error was large. In the second structure, compared with the DQ4:2C1, the output *C*out is generated by connecting it directly to the input *x*3 in the approximate part. Fig. 5 shows the internal structure of the approximate part and the overall structure of DQ4:2C2. While the error rate of this structure is the same as that of DQ4:2C1.

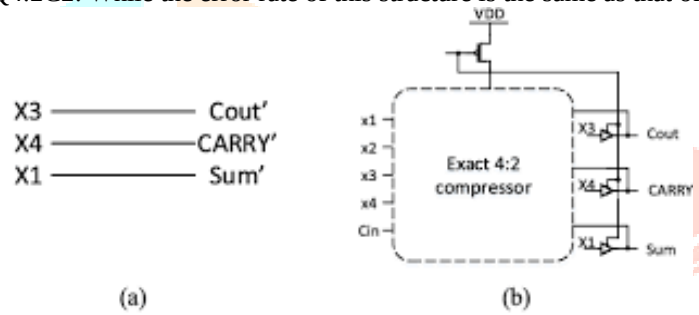

Fig. 5. (a) Approximate part and (b) overall structure of DQ4:2C2.

3) Structure 3 (DQ4:2C3): The previous structures, in the approximate operating mode, had maximum power compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed. In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown in Fig. 6(a). In this structure, the accuracy of output *sum_* is increased. Similar to DQ4:2C1, the approximate part of this structure does not support output *C*out. The error rate of this structure, however, is reduced to half. The overall structure of DQ4:2C3 is shown in Fig. 6(b) where the supplementary part is enclosed in a red dashed line rectangle. Note that in this structure, the utilized NAND gate of the approximate part (denoted by a blue dotted line rectangle) is not used during the exact operating mode. Hence, during this operating mode, we suggest disconnecting supply voltage of this gate by using the power gating.

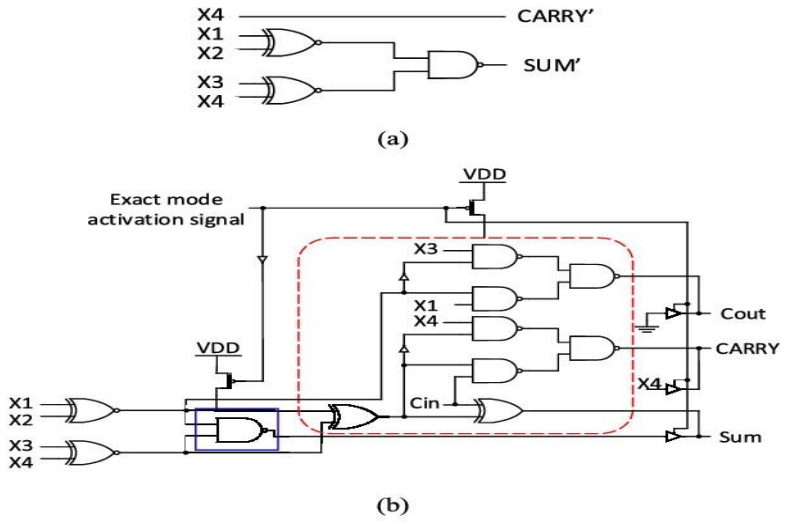

Fig. 6. (a) Approximate part of DQ4:2C3 and (b) overall structure of DQ4:2C3.

4) Structure 4 (DQ4:2C4): In this structure, we improve the accuracy of the output *carry_* compared with that of DQ4:2C3 at the cost of larger power consumption. The internal structure of the approximate part and the overall structure of DQ4:2C4 are shown in Fig. 7. The supplementary part is indicated by red dashed line rectangular while the gates of the approximate part, powered OFF during the exact operating mode, are indicated by the blue dotted line.

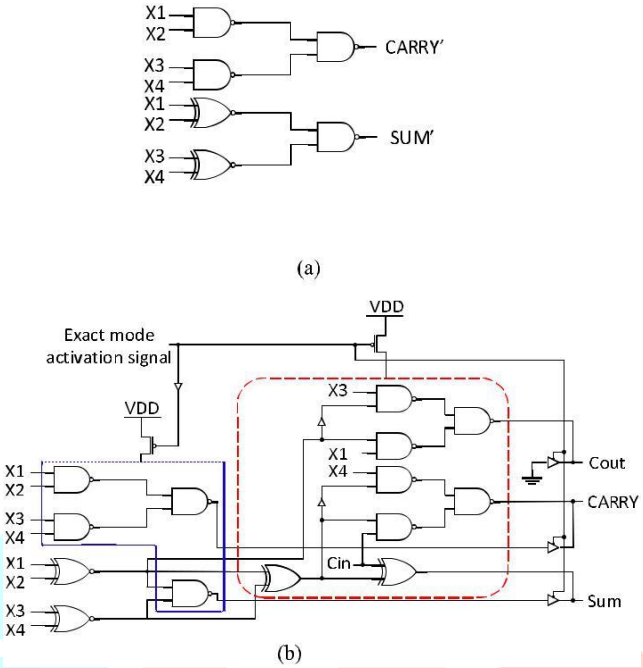

Fig. 7. (a) Approximate part of DQ4:2C$_4$ and (b) overall structure of DQ4:2C$_4$.

III. Study Of Multiplier Realized By The Proposed Compressors:

In this section, first the accuracy of 8-bit Dadda multipliers realized by the proposed compressors is studied. A proper combination of the proposed compressors may be utilized to achieve a better design parameters(area and power). These multipliers are compared by the approximate Dadda multipliers implemented by two prior proposed approximate 4:2 compressors discussed in as well as the configurable multiplier suggested. The architecture of 8-bit Dadda Multiplier is shown in the Fig. 8.

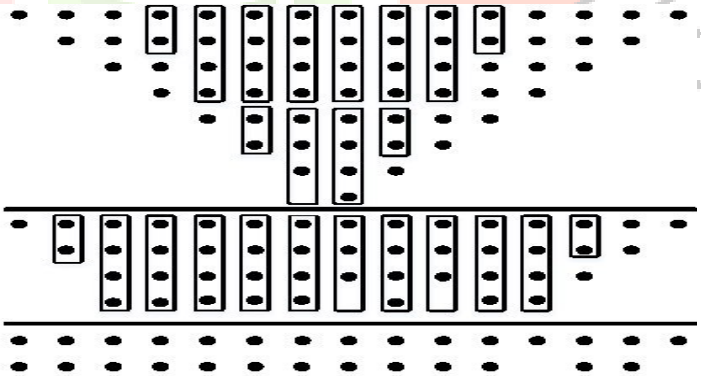

Fig. 8. Reduction circuitry of an 8-bit Dadda mutiplier.

IV. Results And Discussion:

In this section, the results of 8-bit Dadda Multiplier realized by the proposed compressors are compared. Table1 shows the comparison table for different compressor used in Dadda Multilipier. From the Table1 we can say that Exact compressor have less area and the number of gates is also less when compared to other compressors. But when coming to Power the Dual-Quality 4:2 compressor 3 i.e DQ4:2C3 consumes less power when compared to other compressor.

DADDA MULTIPLIER	Compressors Used	Area(um^2)	Power (nW)	Gate count
	4:2C	1045	2449398.581	234
	EXACT C	921	2507427.213	205
	DQ4:2C1	962	2496195.708	216
	DQ4:2C2	997	2463565.709	235
	DQ4:2C4	1213	2151167.386	273
	DQ4:2C3	943	1927253.845	222

Table1. Comparision Table

V. Conclusion:

Multiplication is one of the important operations in many signal processing and image processing applications. The performance of the multiplier has a direct effect on the final output of these applications. Due to this, there is always a need to design a multiplier with high speed and low power consumption. Accuracy is a term relative to the application. In our work, we have designed 6 different types of compressors, which were implemented in an 8 bit Dadda Multiplier evaluated in 45nm technology.

These compressors were employed in the structure of a 8-bit Dadda multiplier to provide a configurable multiplier whose accuracy (as well as its power) could be changed dynamically during the runtime. Our studies revealed that for the 8-bit multiplication, the proposed compressors yielded, on an average 192nW power consumption and in the approximate mode compared with those of the recently suggested compressors.

When compared to the other compressors the power consumption of the proposed compressor is very low. Finally, our study shows that the multipliers realized based on the suggested compressor have less power consumption when compared with the remaining compressors

VI. References:

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