Survey on Static Random Access Memory

[1]S.A.Sivakumar, [2]S.Geetha, [3]R.Senthil Ganesh, [4]Dr.R.Naveen
[1,3]Assistant professor, [2]PG Scholar (M.E., VLSI Design), [4]Associate Professor & Head
[1,2,3,4] Department of Electronics and Communication Engineering
[1,2,3,4] Info Institute of Engineering, Coimbatore, Tamilnadu, India

Abstract : This paper presents an extensive summary of the latest developments in low power circuit techniques and methods for static random access (SRAM) memories. SRAM has been a major component in many VLSI chips due to their large storage density and small access time. It has become the topic of substantial research due to the rapid development for low power and low voltage memory design. Low power consumption has been highlighted as one of the most important design features of a system on chip (SoC). SRAM performs both read stability and write ability. It is used for mobile applications as both on chip and off chip memories, because of their ease of use and low standby leakage.

***Index Terms* - Static Random Access Memory (SRAM), low power consumption, System on Chip (SoC), read stability, write ability.**

I. INTRODUCTION

With the recent proliferation of portable devices, low power consumption has been highlighted as one of the most important design features of a system on chip (SoC). Low power consumption in a static random access memory (SRAM) is particularly important, because a significant portion of the SoC is occupied by the SRAM. It is, therefore, necessary to minimize the supply voltage to achieve low power operation in the SRAM. However, scaling down the supply voltage increases the threshold voltage (Vth) variation due to the variation sources, such as the random dopant fluctuation (RDF) and line edge roughness (LER). An increase in the Vth variation exacerbates the mismatch between paired transistors in an SRAM cell, and this, in turn, degrades both the SRAM read stability and writes ability. To reduce the Vth variation, FinFET is widely used in 22-nm technology as an alternative device to conventional planar-bulk MOSFET.

A low-doped or undoped channel in FinFET suppresses the RDF, and the 3-D structure affords a better short-channel control Lability. Accordingly, the susceptibility to the Vth variation can be alleviated in a FinFET based SRAM. Despite the advantages of the FinFET, it cannot achieve sufficient operational yield at a low operating voltage using the conventional 6T SRAM cell. Moreover, the quantized strength ratio between transistors in a FinFET-based SRAM cell worsens the read–write tradeoff. There is thus the need for the development of a new variation-tolerant SRAM cell. In the light of the forgoing issues of the conventional 6T SRAM cell, various SRAM cells have been recently proposed. In 8T SRAM cell, the storage nodes are decoupled from the read bitline (BL) to enable the same level of read stability as hold stability.

9T SRAM cell in improves the write ability by turning OFF the transmission gate inserted into the feedback inverter loop, However, bit cell area is still large and unnecessary BL discharges the unselected columns increase the energy consumption during the read operation.

II. POWER GATED 9T SRAM

The PG9T SRAM cell consists of a cross-coupled pair of inverters (PU1, PU2, PD1, PD2, PGP, and PGN) and an access buffer (AC1, AC2, and MDR). One of the two cross-coupled inverters (PU1, PD1, PGP, and PGN) has stacked pMOSs (PU1 and PGP) and nMOSs (PD1 and PGN) in the pull-up and pull-down networks, respectively, where PGP and PGN are the power-gating pMOS and nMOS, respectively. A single-ended BL and the storage node Q are connected through the access buffer for read and write accesses. The row-based wordline (WL) is enabled for both the read and write operations while the column- based write WL (WWL) is enabled only for the write operation. The WL for PGP (WLPU) and the WL for PGN (WLPD) are the row-based control signals, which turn OFF the pass-gate transistors only during the write operation. Meanwhile, the column- based virtual VSS (VVSS) is activated only during the read operation is shown in Fig.2.1.

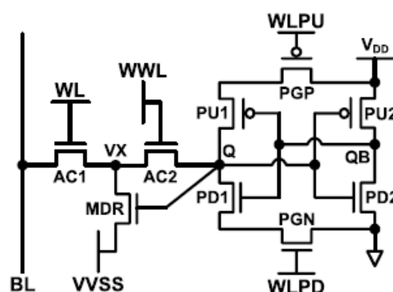

Fig. 2.1 PG 9T SRAM cell

2.1 Read Operation

A read operation begins when the WL is enabled and the VVSS is discharged to VSS while the AC2 is turned OFF. Depending on the data stored at node Q, the precharged BL is either discharged or remains high. When the data at node Q is “1,” MDR is turned ON, and this causes the discharge of the BL to VSS through AC1 and MDR. Conversely, when the storage at Q is low, the BL level remains high, because MDR is turned OFF. The read operation ends when a sense amplifier detects the transition of the BL. Because the data storage nodes are decoupled from the BL, the read current does not flow through the storage nodes, and this eliminates read disturbance. The read stability is thus the same as the hold stability.

2.2 Write Operation

A write operation begins when the WLPU is charged to VDD and the WLPD is discharged to VSS. Writing “1” at the storage node is much more difficult than writing “0,” because the access transistors (AC1 and AC2) are composed of NMOSs, which have a weak ability to

pass "1." Vth drop occurs in the nMOS transistors during a write "1" operation. write- assist technique can be used. When the WL boosting technique is applied to the PG9T SRAM cell, the higher voltage can be transferred to storage node Q to reduce the write delay.

2.3 Bit Interleaving Scheme

A bit interleaving scheme is necessary for nanoscale SRAM arrays to minimize the occurrence of multiple bit errors, because the soft error rate caused by α-particles increases with technology scaling. Error correction code is a common in memories and microprocessor caches for significantly reducing the external single bit errors. The conventional ECC has very limited correction capability. In the bit interleaving scheme, on the other hand, neighboring bits are arranged using different words, and then, column-based BL signals are interleaved through multiplexers and detected by a single sense amplifier.

III. ANALYSIS BASED ON 22NM TECHNOLOGY

In this section, the proposed PG9T SRAM cell is compared with the previously proposed SRAM cells in 22-nm FinFET technology is shown in Fig.3.1.The SRAM cells were verified by Monte Carlo simulations for statistical analysis. In the simulation, the Vth variation was modeled to follow Gaussian distribution whose standard deviation (σV th) is expressed as

$$\sigma_{V\text{th}} = \frac{A_{Vt}}{\sqrt{\text{Length} \times \text{Width}}}$$

where the Pelgrom coefficient AVt is assumed to be 1.8 mV .To consider all variation sources including RDF, LER, work,function variation, and fin width and gate length variations.

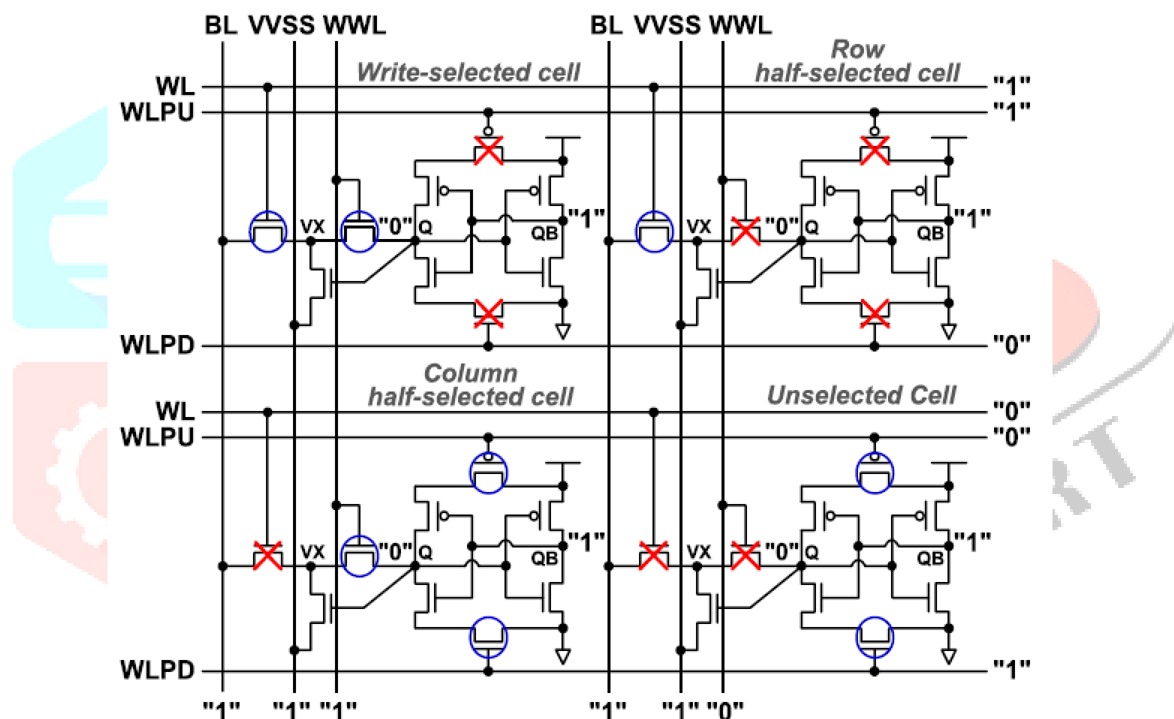

Fig.3.1 PG9T SRAM cell array and write "1" operation

3.1 Bit Cell Area

The layout of the previous 9T SRAM cell is different from that for area minimization with considering the layout rule restriction in 22nm FinFET technology, such as width quantization effect, single gate orientation, and regular gate pitch. The metal layout of the PG9T SRAM cell. It is assumed that the single fin is used for all devices in the SRAM cells. The number of metal layers is minimized by using local interconnects.Four metal layers are used to route the control signals along the rows and columns. VDD and VSS are routed by metal 1 in the column direction; BL and WWL are internally routed by metal 2 in the row direction; BL and WWL are routed again by metal 3 in the column direction; VVSS is also routed by metal 3 in the column direction; and WL, WLPU, and WLPD are routed by metal 4 in the row direction.

A detailed model of CAM is shown in Figure 2.1. The figure shows the CAM cell for 3 words and each word having 3 bits. That corresponds to 3 CAM cells. There is a match line is connected to each words and cell is connected with search line pairs. These are connected to match line sense amplifiers. Each CAM cell is stored with some data and the search operation starts with loading the register with search data. And also these are recharged to high value. The high value is in the match line. Next the search data from the register is given to these arch lines. The CAM cell compares the stored data against the search data bits on the search lines. If the comparison result is a mismatched condition then the match lines are discharged otherwise these remain in the precharged high state. The match line sense amplifier finds the matched or mismatched condition. And the encoder encodes the matching location to its encoded address

3.2 Read Stability and Delay

The read static noise margin (RSNM) was used as the read stability metric. The read stability yield is measured in μ/σ and obtained from the Gaussian distribution of the RSNMs for 10 000 Monte Carlo samples. All of the read- decoupled SRAM cells (8T, CP10T, PPN10T, previous 9T, and PG9T) have the same RSNMs, which are nearly equivalent to the hold static noise margins, because the read disturbances are eliminated by decoupling the storage nodes from the BLs. They all achieve the target read stability yield of 6σ, even in the low voltage region without the use of a read assist circuit is shown in Fig3.2(a).

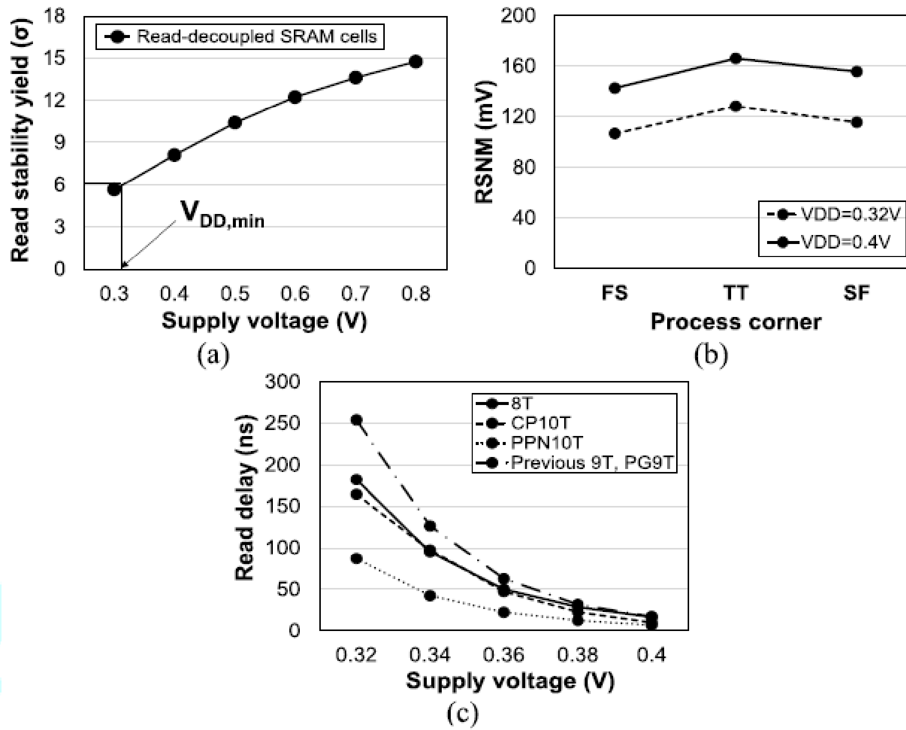

Fig.3.2 (a) Read stability yields, (b) RSNMs at different process corners, (c) read delays of read-decoupled SRAM cells.

Fig.3.2(b) shows the RSNM of the PG9T SRAM cell at different process corners (FS, TT, and SF). At TT corner, the inverters in the latch are low-skewed because of greater electron mobility than hole mobility. FS corner makes the inverters further low skewed while the SF corner cancels out the originally low- skewed effect by making them high skewed from the TT corner. Therefore, the RSNM is the smallest at FS corner. Fig.3(c) compares the 6σ worst read delay of the proposed PG9T SRAM cell with those of the previously proposed SRAM cells for different supply voltages. The PPN10T SRAM cell has the shortest read delay, because it has small BL capacitance and its differential BL pair requires only small voltage development for correct sensing.

3.3 Write Ability and Minimum Required Boosted WL Voltage

The write abilities of the read decoupled SRAM cells are compared based on the WL write trip voltage (WWTV) . The write ability yield is measured in μ/σ and obtained from the Gaussian distribution of the WWTVs for 10000 Mont Carlo samples.

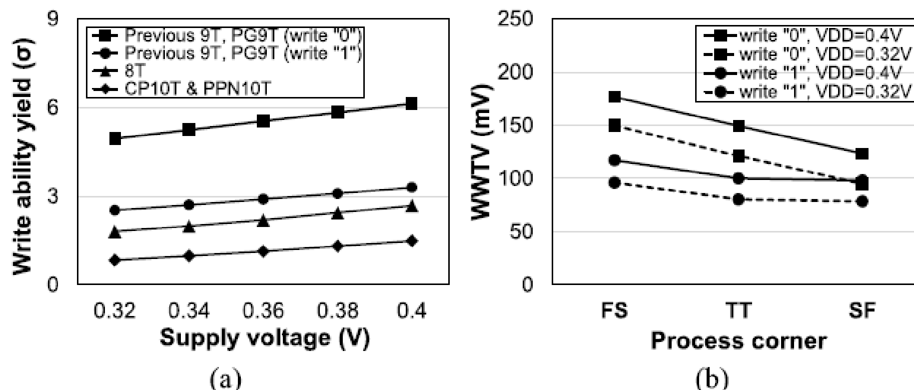

Fig.3.3 (a)Write ability yields of read-decoupled SRAM cells. (b) WWTVs of proposed PG9T SRAM cell at different process corners

Fig.3.3 (a) compares the write ability yields for low operating voltages. The write ability yields in the CP10T and PPN10T SRAM cells are significantly poorer than that in the 8T SRAM cell owing to the stacked access transistors in the former. The write ability yields of the previous 9T and PG9T SRAM cells are higher, because their disconnected latches facilitate the write operation despite the stacked access transistors. Fig.3.3(b) shows the WWTVs of the PG9T SRAM cell at different process corners (FS, TT, and SF). The WWTVs is the largest

in FS corner and the smallest in SF corner due to the stacked nMOS write path. In the low voltage region, none of the read-decoupled SRAM cells is able to achieve the 6σ target write ability yield without an assist circuit. The WL (WL and WWL) boosting-assist technique is an appropriate means of achieving the target write ability yield and speeding up the write operation.

3.4 Energy Consumption and Standby Leakage Power

The average energy consumptions per read or write operation of the SRAMs were measured and compared for different supply voltages using the worst case data pattern. A 4:1 bit interleaving scheme and 256 rows × 128 columns of the cell arrays were assumed. As the supply voltage reduces, the read energy consumption also reduces. The write energy consumptions of the different SRAMs when using the WL boosting scheme for ensuring 6σ write ability yield. The write energy consumption is dominated by the column-based signals, because the number of the selected columns is much larger than that of the selected row in the 256-row × 128-Column cell array with the 4:1 bit interleaving scheme. The comparison of the leakage power, the CP10T, PPN10T, previous 9T, and PG9T SRAMs consume similar leakage power, because they use the similar stacked write access transistors. The 8T SRAM consumes the highest leakage power, which derives from the single access transistor.

3.5 Column-Based VVSS Scheme and Sensing Yield

In a single-ended SRAM with the column-based VVSS scheme, a data- dependent leakage current undesirably discharges the precharged BL. The BL noise particularly deteriorates when all the column half-selected cells store "1"s. Column-based VVSS can also be applied to the previous SRAM cell. In this case, the sensing yield of the previous 9T cell reduces and becomes the same as that of the PG9T SRAM cell. This is because the same bias condition of the column half- selected cells in the previous 9T and PG9T cells yields the equivalent leakage current.

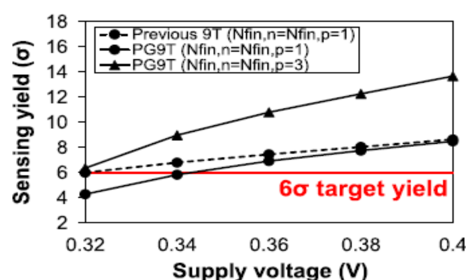

Fig.3.4 Sensing yields for different supply voltages

The read energy becomes the same as that of the proposed PG9T SRAM owing to the same WL swing and BL discharge. In the aspects of the bit cell area and energy consumption per write operation, the PG9T SRAM cell outperforms the previous 9T SRAM cell with column-based VVSS, because they are independent of the direction of VVSS.

IV. LITERATURE REVIEW ON SRAM

4.1 Systematic approach of FinFET based SRAM bitcell design for 32nm node and below

S. C. Song et al [2009] developed a Fin configuration (i.e., Fin thickness, space, height, and number) in the bitcell involves considerations on both layout and electrical optimization[1]. Once optimized through the proposed method, FinFET bitcell can provide higher cell current, lower leakage current and much lower Vccmin. SRAM bitcell is considered as a first functional block in SOC to be implemented using FinFET. Continuous SRAM bitcell size scaling, however, has posed significant challenges, such as increasing leakage current and degraded cell stability.Critical issues of SRAM bitcell scaling, such as demand for continuous bitcell size scaling and electrical stability problem, can be resolved by using FinFET based bitcell[1].

4.2 Large-Scale SRAM Variability Characterization in 45 nm CMOS

Z. Guo et al [2009] developed a Fast and accurate validation of SRAM read stability and write ability margins is crucial for estimating yield in large SRAM arrays. This work presents a method for large-scale characterization of read stability and write ability in functional SRAM arrays using direct bit-line measurements[2]. Large-scale SRAM read/write metrics are measured and compared against conventional SRAM stability metrics.To satisfy the functionality of hundreds of millions of SRAM cells in current on-die cache memories, the design has to provide more than 6 standard deviations of margin for parameter variations.

4.3 Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond

H. Kawasaki et al [2009] developed a FinFET integration challenges and solutions are discussed for the 22 nm node and beyond. Fin dimension scaling is presented and the importance of the sidewall image transfer (SIT) technique is addressed. Diamond-shaped epi growth for the raised source-drain (RSD) is proposed to improve parasitic resistance degraded by 3-D structure with thin Si-body[3]. The issue of Vt mismatch is discussed for continuous FinFET SRAM cell-size scaling.The FinFET is considered a leading candidate because the double- gate structure allows superior electrostatics. In SRAM, since each fin adds a fixed increment of effective device width, the β-ratio discreteness will be a possible issue to achieve enough margin in both read and write operations(Rpara) reduction and Vt adjustment are concerns especially for a high performance logic circuit.

4.4 P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Subthreshold Operation

C. H. Lo et al [2011] developed a SRAM has been under its renovation stage recently, aiming to withstand the ever-increasing process variation as well as to support ultra-low-power applications using even subthreshold supply voltages. P- P-N-based 10T SRAM cell, in which the latch is formed essentially by a cross- coupled P-P-N inverter pair[4]. This type of cell can operate at a voltage as low as 285 mV while still

demonstrating high resilience to process variation. Its noise margin has been elevated in not only the hold state, but also the read operations. The voltage down-scaling in many low-power applications, designing a new and robust SRAM cell with the capability of operating at a subthreshold voltage while consuming low leakage power during the standby mode is highly demanded.

4.5 Design and Iso-Area Vmin Analysis of 9T Subthreshold SRAM With Bit- Interleaving Scheme in 65-nm CMOS

M. H. Chang, et al [2012] developed a 9T bit cell is proposed to enhance write ability by cutting off the positive feedback loop of a static random-access memory (SRAM) cross-coupled inverter pair. In read mode operation, an access buffer is designed to isolate the storage node from the read path for better read robustness and leakage reduction. The bit-interleaving scheme is allowed by incorporating the proposed 9T SRAM bit cell with additional write wordlines (WWL/WWLb) for soft-error tolerance.The supply voltage is below the transistor threshold voltage, the variability of SRAM increases severely in design and process parameters regarding proper ratio of device strengths [5].

V. COMPARATIVE ANALYSIS

Table 5.1 Comparative analysis on various static random access memory architectures

AUTHOR	YEAR	ALGORITHM	ADVANTAGE	DISADVANTAGE
S. C. Song et al	2009	FinFET bitcell can provide Higher cell current, lower leakage current and much lower Vcc min with smaller bitcell area and as compared to planar bitcell, which allows continuous scaling of SRAM bitcell.	It provide higher cell current, lower leakage current and lower Vcc min.	scaling and electrical stability problem.
Z. Guo et al	2009	The functionality of hundred s of millions of SRAM cells in current on-die cache memories, the design has to provide more than 6 standard deviations of margin for parameter variations.	Large-scale read/write metrics are measured.	Low VMIN measurement.
H. Kawasaki et al	2009	The FinFET is considered a leading candidate because the double-gate structure allows superior electrostatics	Improve parasitic resistance.	Low read and write operation.
C. H. Lo et al	2011	In P-P-N-based 10T SRAM cell, the latch is formed essentially by a cross-coupled P-P-N	Ultra low cell leakage. High immunity to the data dependence bitline leakage.	Low read and write delay.

VI. CONCLUSION

In this paper, PG9T SRAM cell characterized by smaller area, improved variation tolerability, and low energy consumption compared with previously proposed SRAM cells.The performance between previous and proposed SRAM cells based on the 22-nm FinFET technology at the minimum operating voltage.Thus affording improved write ability. The energy consumption per read operation of the proposed SRAM cell is much lower than those of the previous SRAM cells.To the elimination of unnecessary BL discharge through the use of a column-based VVSS. In addition, the proposed SRAM cell has a smaller area and consumes less energy per write operation than the previous 9T, CP10T, and PPN10T SRAM cells. These features of the proposed SRAM cell afford a high integrated memory, better noise immunity, and low energy consumption.

VII. ACKNOWLEDGMENT

Our sincere thanks to the management of Info institute of engineering for providing the research lab for our work.

REFERENCES

[1] S. C. Song et al., "Systematic approach of FinFET based SRAM bitcell design for 32nm node and below," in Proc. IEEE Int. Conf. IC Design Technol., May 2009, pp. 165–168.

[2] Z. Guo, A. Carlson, L. T. Pang, K. T. Duong, S. J. K. Liu, and B. Nikolic, "Large-scale SRAM variability characterization in 45 nm

CMOS," IEEE J. Solid- State Circuits, vol. 44, no. 11, pp. 3192–3714, Nov. 2009.

[3] H. Kawasaki et al., "Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond," in Proc. IEEE Int. Electron Devices Meeting (IEDM), Dec. 2009, pp. 289–292.

[4] C.-H. Lo and S.-Y. Huang, "P-P-N based 10T SRAM cell for low-leakage and resilient subthreshold operation," IEEE J. Solid-State Circuits, vol. 46, no. 3, pp. 520–529, Mar. 2011.

[5] M. H. Chang, Y. T. Chiu, and W. Hwang, "Design and iso-area Vmin analysis of 9T subthreshold SRAM with bit-interleaving scheme in 65-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 7,

[6] M. E. Sinangil, H. Mair, and A. P. Chandrakasan, "A 28nm high-density 6T SRAM with optimized peripheral-assist circuits for operation down to 0.6V," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2011, pp. 260–262.

[7] C. Shin et al., "Performance and area scaling benefits of FD-SOI technology for 6-T SRAM cells at the 22-nm node," IEEE Trans. Electron Devices, vol. 57, no. 6, pp. 1301–1309, Jun. 2010, doi: 10.1109/TED.2010.2046070.

[8] J. Maiz, S. Hareland, K. Zhang, and P. Armstrong, "Characterization of multi- bit soft error events in advanced SRAMs," in IEEE IEDM Tech. Dig., Dec. 2003, pp. 21.4.1–21.4.4.

[9] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 650–658, Feb. 2009.