Low Power and Low area based Dual Power Lines for—A CMOS Receiver Design

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Abstract:Today there are many more designing are available for a CMOS receiver. Not only their effectively work and circuit complexity increases. For limiting of I/O pins reducing individual nodes and increases proportionally nodes. This problem address by proposing power line communications (PLCs) at the designing level, specifically the dual use of power pins and power distribution networks for application/ observation of simulated data as well as delivery of power. In this paper we simulate and proposed the PLC receiver the transmission of data with super imposing power lines. The main design objective of the proposed PLC receiver is the unique design operation under variations and droops of the supply voltage with increased high data speed. The proposed PLC receiver is designed in CMOS 0.18-μm technology under a supply voltage of 1.8V. The simulation results show that the receiver can capable to send data rate is 1 Gb/s. The receiver can dissipate total static power is 1.302mW under 1.8 V supply.The threshold value is set to 0.55 mV (or 2.5% of the supply voltage) and the signal values are interpreted as logic 0 (1) if it is lowering (greater) than -0.083 (1.717 V) under the supply voltage of 1.8 V. Note with the comparison of tolerance to the supply voltage that range of ±46%. The area of layout is also less as of it covers 100.3µm × 23.4 µm.

IndexTerms:**Design-for-testability (DFT), PLC at ICs, NMOS Design, PLC receiver, power line communications (PLCs). -**

I. INTRODUCTION

In new generation of VLSI technologies many more changes are in there i.e. deep sub micrometer, testing, debugging, and diagnosis of VLSI circuits then they become moreexpensive and difficult. In addition to maximum circuit complexity for a deeper sub micrometer technology, process variationslarger, interconnection delays are also greater, transistor switching time, and higher leakage current also contribute to make the testing more challenging [1]. It is a basic &general consensus among testing engineers that accessibility, i.e., observabilityand controllability, to internal nodes for both 3-D and 2-D ICs is essential to address the problems of testing [6]. In Conventional design-for-testability (DFT) methods, i.e. scan design, internal nodesand provide dedicated or shared signal paths between I/O pins [14]. As the complexity increases of circuit, the number of internal nodes increases proportionally, anddue to the limited number of available I/O pins, individual internal nodes are less accessible [2].
One promising approach to provide ubiquitous accessibility to internal nodes is the dual use of power pins and power distribution networks (PDNs) for data communications as well as power delivery, which are essentially, power line communications (PLCs) at the IC level [1].

II. LITERATURE REVIEW

In the part of hardware designing many designers has given their design concept on the PLC based CMOS receiver. In this follows the previous work has done on same technology CMOS 180nm in which the measurement results show that the receiver can tolerate a voltage drop of up to 0.423 V for a data rate of 10 Mb/s. The receiver dissipated power is 3.26mW @ 1.8V supply and the used core area for receiver is 74.9µm× 72.2µm. To the best of the knowledge, in an IC environment,PLC was exclusively reported in [1] Fig. 1 shows the conceptual and experimented PLC system in an IC environment considered for their research [7]. On the same path A test instrument sends the data superimposed on the supply voltage of a system board [3]. The signal travels through a power pin(s), the power area of a package, and the PDN, and then it reached at the intended node(s) [10]. To use power pins to simultaneously carry data signals while delivering its power. A direct superposition of a data signal on a power pin would fail due to an inherent high noise level on power lines and precludes the possibility for multiple data channel. To address the problem, we suggest adoption of the direct sequence-code division multiple access (DS-CDMA) and UWB (Ultra Wideband) communication technologies [11].
This paper presents a superimposed dual PLC receiver, whose main design concentration is robust operation under supply voltage variations and sinks [8]. The proposed power line communication receiver was designed and fabricated in CMOS 180nm technology under 1.80V supply voltage.

At rest this paper has organized as follows. Section II provides the basic background identification of the proposed work. Section III describes the proposed PLC receiver with the help of blocks diagram. Section IV presents the simulation results. Section V explains the conclusions and the future works for PLC.

III. PROPOSED POWER LINE COMMUNICATION RECEIVER:

The proposed PLC receiver receives the input data by superimposed on power lines. The receiver has also designed in CMOS 0.18nm technology with a supply voltage of 1.8 V. It consists of three building blocks, and this section describes the design of each building block.

(a) Level Translator

The level translator shown in Fig. 1 can be behaved as a common source amplifier where PMOS behaves diode connected load as, in which input is fixed to a bias voltage V_{bias}. In the proposed configuration for mixing of VDD + $V_{(D)}$where VDD is supply voltage and $V_{(D)}$transient response based message signal. For the superimposing of these two signal in a single power line we have used OR logic. The level translator propagates the data signalimposed on the supply voltage *VDD* to the output while lowering the dc voltage level of the signal to*VDD*/2 [7]. When Vbias is offering low voltage MN2 gate is opened and signal will pass a common source amplifier to the output section. To propagate the data signal superimposed on the supply voltage to the output, the output should be sensitive to supply voltage variations and the respective output of level translator is given in Fig. 2. This proposed configuration also works for Power supply rejection ratio (PSRR) of respective amplifier circuit. Here we also kept the W/L ratio of M1 transistor is two time larger than M2 transistor.

$$\text{PSRR} = \frac{A_V}{A_{Vdd}} \qquad (1)$$

Thus, the PSRR of a common source amplifier is expressed as

$$\text{PSRR} \approx -\frac{g_{m1}}{g_{Vm2}} \qquad (2)$$

So the equation 2 is telling for lower PSRR the gm_1 smaller than the gm_2. Thismeans that the bias voltage and the W/Lratio of MP1 shouldbe set to small, while operating MP1 in saturation. Since thedesired dc voltage level at the output of the sensing circuitis *VDD*/2, the condition sets the overdrive voltage of MN2. A large W/L ratio for MN2 increases the current ID, and so it is a compromise between low-power dissipation and low PSRR [5].

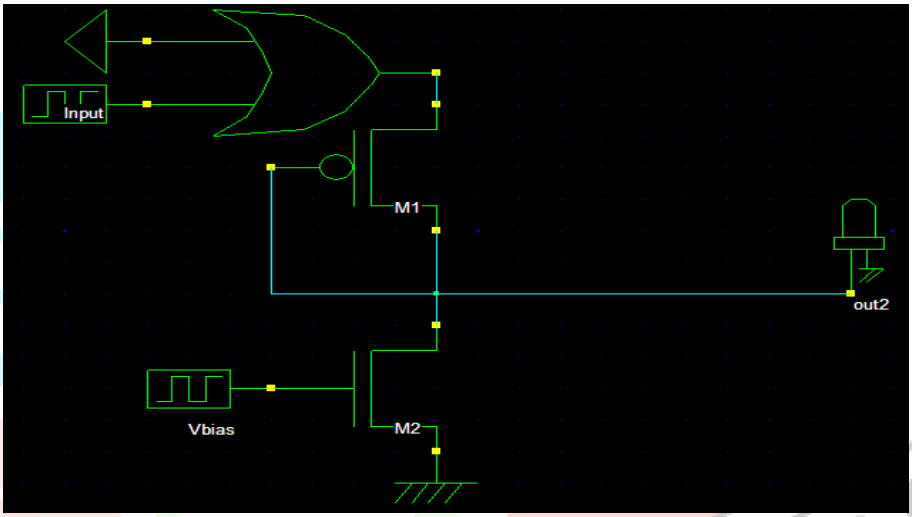

Fig: 1 Schematic of Level translator

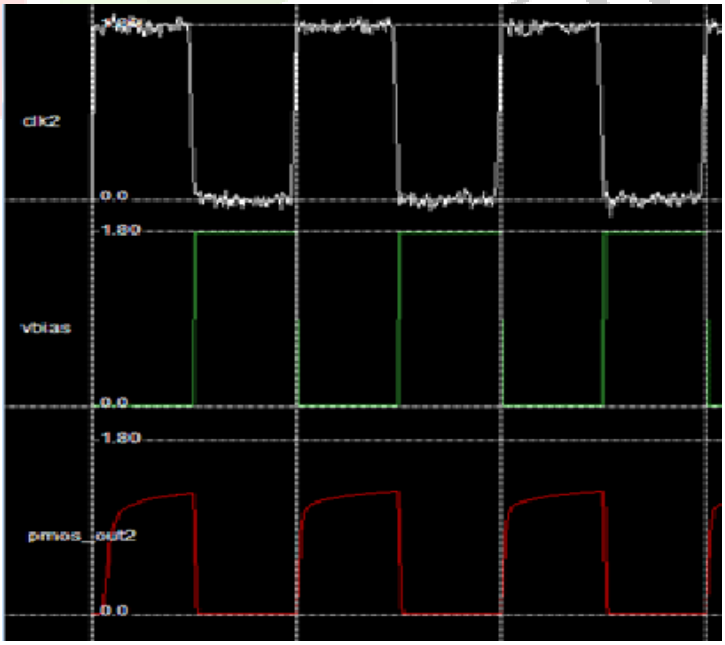

Fig: 2 Level translator Output waveform

(b) Signal Separator

As the proposing of differential amplifier as a balanced topology and also act as a mixer for dual input over a single power line. This design supports low power designing for RF, UWB and IR range communication device. Here one clock signal (clk 3) provided as a reference

voltage of two grounded NMOS (M9 & M10). This clock pulse will be inverse switching mode to the Vbias cause will be given the lower additive noise figure and more linear output waveform. The input signal of the signal separator(differential amplifier & mixer) is the data signal offset with *VDD*/2, and the signal separator amplifies the data signal while removing the dc offset voltage and also has design to overcoming of hysteresis. The signal separator shown in Fig. 3 is a differential amplifier designed by fully NMOS, which reducing the space consumes by PMOS and other passive components. The design stands for extract the dc value of the signal without requiring of filter. The differential amplifier rejects the common-mode rejection signal of the two inputs or the dc value. It also converts a dual mixed input into dual separated outputs in fig. 4.

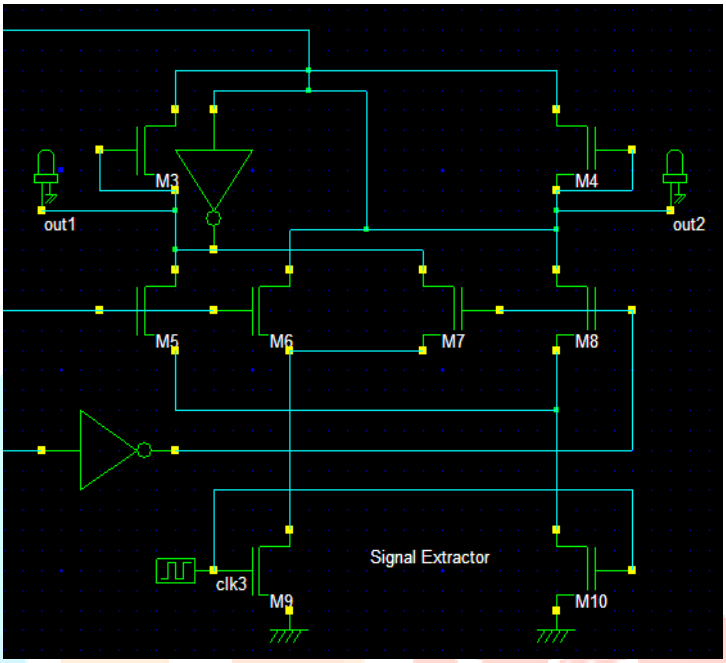

Fig: 3 Schematic of Signal Separator

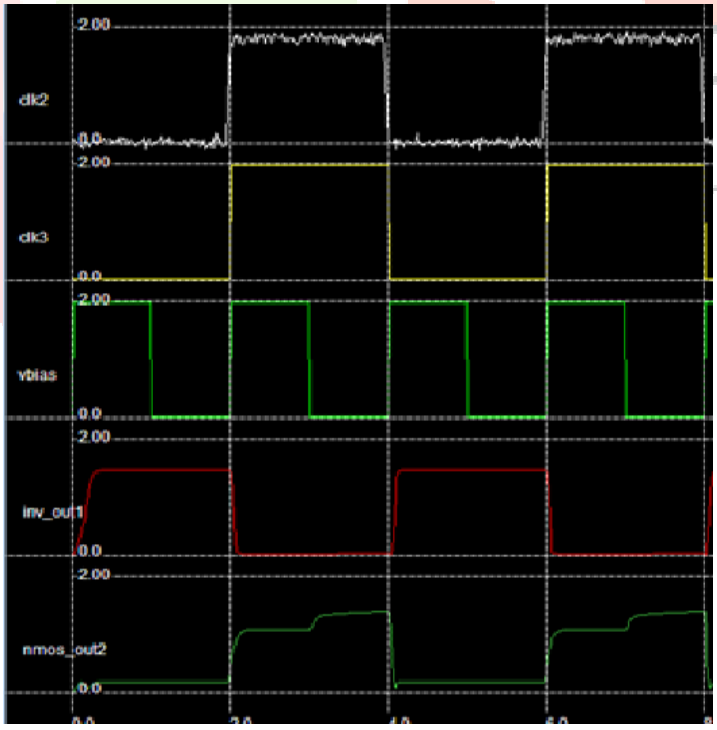

Fig: 4 Signal separator output waveform

(c) Logic Renovator

In fig 5, four stacked parallel input Mosfets M11-M14 and their respective gate electrodes are coupled tothe trigger input IN. Depending on the transition of IN, both MOS transistors, signals are generated Which are controlled by the transistor size ratio M15/M11 and M16/M13. M15 and M16makes an inverter to provide a sharp transition at OUT. MP1and MN1 form a feedback structure to control the switchingof the transistors in the circuit. If IN is low then M15 is offand M16 is on, OUT is low. As IN increases, M11 begins toturn on

and VN starts to decrease. The trip point is definedWhen IN=Vtn2+VN that is When M13 turns on. When M3turns on, drain of M3 starts decreasing and turns NMOSMN1 off. Once M13 is on, the transition is very fast. If the transistor size of M13 is large compared to M14 and M16 thentrip point (VIH) is accurately decided by the ratio of M15/M14. Similarly VIL is decided by the ratio of M15/M11. This proposed configuration has two parallel connections and each one is working vice versa for final result. At low supply voltage this circuit provides considerable hysteresis values, given in Fig. 6 showing the final output waveform of proposed circuits as compare with the base paper [1].

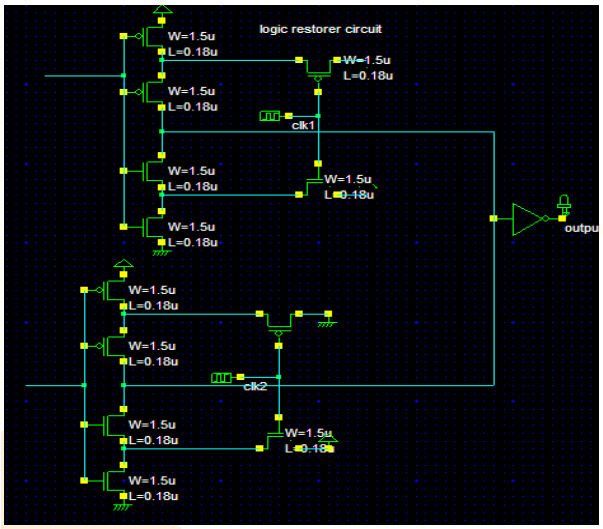

Fig: 5 Schematic of Logic Renovator

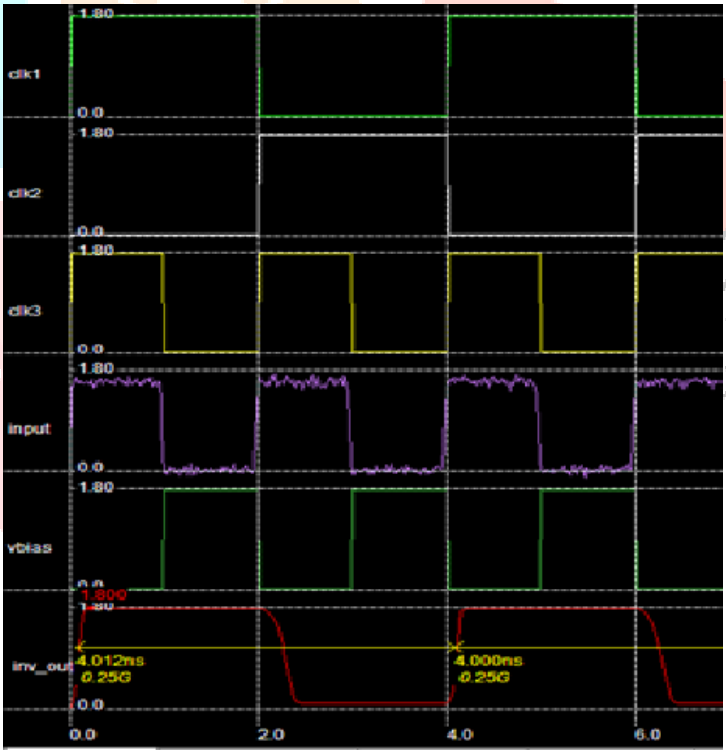

Fig: 6 Simulation results

IV. SIMULATION RESULTS:

The proposed PLC receiver is designed in CMOS 0.18-μm technology with a supply voltage of 1.8 V.The threshold value is set to 0.55 mV (or 2.5% of the supply voltage). This means that a signal value is interpreted as logic 0 (1) if it is lowering (greater) than -0.083 (1.717 V)under the supply voltage of 1.8 V. Note that the threshold value is well below the tolerable range of ±46% of the supply voltage. The area of layout is also less as of it covers 100.3µm × 23.4µm in Fig: 7.

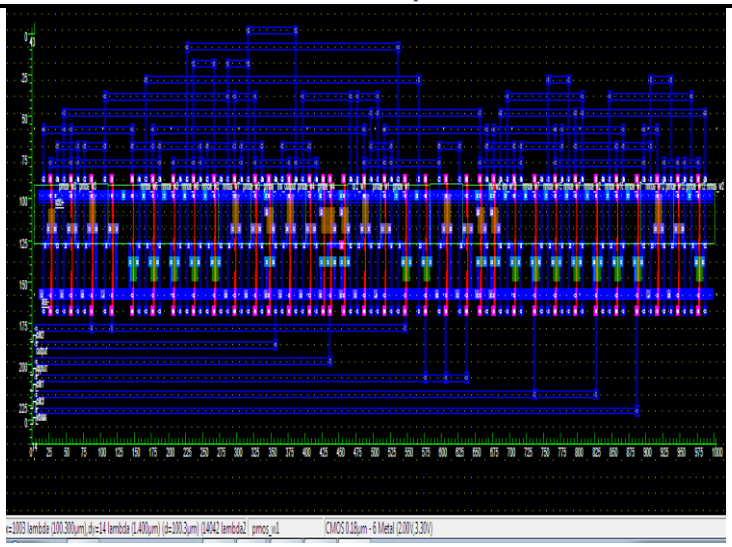

Fig: 7 Layout diagram of Receiver

V. COMPARISION TABLE

Parameters	This work	Previous Work
Technology	0.18 µm	0.18 µm
Supply Voltage	1.8V	1.8 V
Pulse amplitude	0.5V	90.0 mV
Pulse duration	4ns	8 ns
Power consumption	1.302mW	2.4 mW
Data Rate	1 Gbps	250Mbps

VI. CONCLUSION:

A receiver for Power line communication, which can be applicable to high data rate communications, such as UWB applications, scan design,system debugging, and fault diagnosis, was investigated in this paper. The proposed PLC system adopts a binary Amplitude shift key modulation scheme [4], and the receiver consists of three basic building blocks. In that the level translator shifts the dc level of the data signal to a half of the supply voltage. The signal separator, based of a mixer and differential amplifier, removes the dc voltage from the data signal, which mitigates supply voltage fluctuations and sinks. The logic renovator, based on a differential Schmitt trigger, extracts logic values from the data signal while improving the noise immunity and removing of all hysteresis of the receiver [6]. By the calculation for data rate:

Data rate $\leq 2\times$ Bandwidth

Data rate $= 2 \times BW \times \log_2 M$

Here the range of frequencies we got that 0.25 GHz and M are 2 bits values so by the above formula

$= 2 \times 0.25 \times 10^9 \times 2$

$= 1$ Gbps

As of future work in PLC receiver will be concentrate on designing section. In that it can be design by different physical changes and it can be increase higher data transmission rate. Apart from these the proposed circuit has given far better result as previous work for low power application and for high speed.

VII. REFERENCES

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