Design of Low-Power 2–4 Mixed-Logic Line Decoders with Clock based Technique

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Abstract: ***The paper shows the design of decoder for lower leakage current and lower power dissipation is proposed.. In present scenario, power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. The chip density and higher operating speed leads to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products. These paper describes the various 2:4 decoder. The technique used for the 2:4 decoder are 14 transistor using LP, LPI and 15 transistor HP , HPI are discussed and implemented.***

Keywords: CMOS,LP, LPI,HP,HPI

I. INTRODUCTION

Presently a day's energy decrease is a noteworthy issue in the innovation world. The low power configuration is real issue in superior advanced framework, for example, chip, computerized flag processors (DSPs) and different applications. Chip thickness and higher working rate prompt the outline of extremely complex chips with high clock frequencies. So planning of low power VLSI circuits is a mechanical need in these because of the popularity for convenient buyer gadgets items. Decoder is a combinational rationale circuit that changes over a paired number an incentive to a related example of yield bits. Uses of decoders are wide; they incorporate information de-multiplexing, memory address interpreting, seven portion show and so on. A decoder is a straightforward circuit that changes over a code into an arrangement of signs. It is named as decoder since it changes the huge coded information into various basic blends which can be utilized to drive any flag, however we will start our investigation of encoders and decoders since they are more straightforward to outline. Dynamic guidelines happen just inside a sub-set of all directions.

In advanced frameworks, directions and also numbers are passed on by methods for double levels or heartbeat trains. A decoder is a rationale circuit that changes over a N-bit twofold information code into M yield lines to such an extent that just a single yield line is initiated for every last one of the conceivable blends of data sources. The decoder distinguishes or perceives or identifies a specific code. The N data sources can be a 0 or a 1, there are 2N conceivable info blends or codes. For every one of info mix just a single of the M yields will be dynamic (HIGH), all different yields will stay inert (LOW). A few decoders are intended to deliver dynamic LOW yield, while the various yields stay HIGH. A typical kind of decoder is the line decoder which takes a n-digit twofold number and translates it into 2n information lines. The easiest is the 1-to-2 line decoder

The ever growing number of transistors integrated on a chip and the increasing transistors switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive

packing and cooling technologies, increase cost and decreases system reliability.Power dissipation is defined as the rate of energy delivered from source to system/device. Power minimization is one of the primary concerns in today VLSI design methodologies because of the main reasons. One is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to higher power dissipation and it can lead to reliability and IC packaging problems. The low power requirements of present electronic systems have challenged the scientific research towards the study of technological, architectural and circuital solutions that allow a reduction of the energy dissipated by an electronic circuit. One of the main causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and a parasite. Such part of the total power dissipated by a circuit is called dynamic power. In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching has been proposed in the last years. In such approach, the process of charging and discharging the node capacitances is carried in a way so that small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.

II. LITERATURE REVIEW

Since most recent couple of decades the fundamental difficulties were Area, cost, and execution. In any case, nowadays control is an imperative factor rather than cost, execution and region. The gadget which expends less power regardless of speed, for example, heart pacemaker, RFID and so forth chips away at the guideline of adiabatic rationale. The point of lessening in control utilization is application particular. The creators have endeavored to diminish the power by joining the adiabatic and reversible system [1]. The power devoured in customary CMOS configuration can be given as,

$$P=CL.VDD^2. f$$

Here the power (P) is relative to exchanging recurrence (f), capacitance (CL), and square of supply voltage (VDD). Power utilization can be diminished by limiting force supply, capacitance and exchanging recurrence of activity. Yet, when this parameter decreases, it might decay the execution of the circuit. Configuration utilizing adiabatic rule helps in decreasing force utilization at the cost of reduce performance. A strategy in view of adiabatic method utilizes an air conditioner control supply as opposed to dc for vitality recuperation. Hypothetically adiabatic circuits devour zero power, it demonstrates vitality misfortune due to nonzero obstruction in the switches. There are such a large number of papers which depict distinctive kinds of adiabatic procedure, for example, ECRL, 2PASCL, PFAL and so on by which we can decrease control utilization of the circuit [2]. These strategies devour less power as contrast with different CMOS circuits.

III. DESIGN TECHNIQUE

I. DECODER

Proposed 2-to-4 decoder with empower input is built with AND entryways, it turns out to be more prudent to create the decoder yield. A 2-to-4 decoder is empower when E=1. Reality table of a 2-to-4 decoder is given in Table I and the general square outline is appeared in figure 2. The Boolean door based execution of 2-to-4 decoder required four AND entryways and two NOT rationale entryways

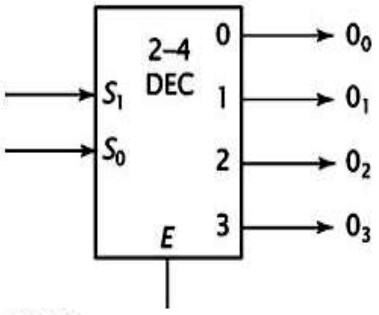

Fig1. General block diagram of 2-to-4 decoder

2:4 LINE DECODER

Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g., SRAM) [7]–[9]. This brief develops a mixed-logic methodology for their implementation, opting for improved performance compared to single-style design.

TABLE I : TRUTH TABLE OF THE 2–4 DECODER

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

TABLE II: TRUTH TABLE OF THE INVERTING 2–4 DECODER

A	B	I0	I1	I2	I3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

A 2–4 line decoder generates the 4 minterms *D*0−3 of 2 input variables *A* and *B*. Its logic operation is summarized in Table I. Depending on the input combination, one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2–4 decoder generates the complementary minterms *I*0−3, thus the selected output is set to 0 and the rest are set to
1, as shown in Table II. In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gate Fig. 1(a), whereas an inverting decoder requires 2 inverters and 4 NAND gates Fig. 1(b), both yielding 20 transistors

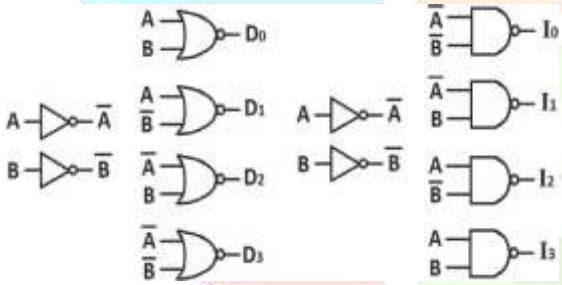

Fig 2. : 20-transistor 2–4 line decoders implemented with CMOS logic.
(a) Non inverting NOR-based decoder. (b) Inverting NAND-based decoder

Mixed Logic Line

Transmission gate logic (TGL) can efficiently implement AND/OR gates [5], thus it can be applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3(a) and (b), respectively. They are full-swinging, but not restoring for all input combinations. Regarding PTL, there are two main circuit styles: those that use nMOS-only pass transistor circuits, like CPL [3], and those that use both nMOS and pMOS pass transistors, like DPL [4] and DVL [6]. The style we consider in this work is DVL, which preserves the full swing operation of DPL with reduced transistor count [10]. The 2-input DVL AND/OR gates are shown in Fig. 3(c) and (d), respectively. They are full swinging but non-restoring, as well.

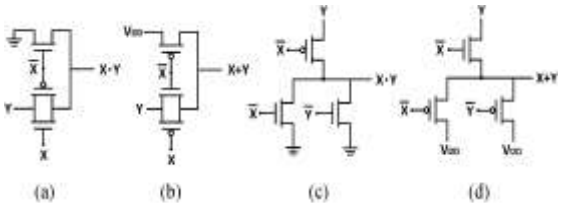

Fig 3. Three-transistor AND/OR gates considered in this work. (a) TGL AND gate. (b) TGL OR gate. (c) DVL AND gate. (d) DVL OR gate.

Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. As shown in Fig. 3, we labelled the 2 gate inputs *X* and *Y*. In TGL gates, input *X* controls the gate terminals of all 3 transistors, while input *Y* propagates to the output node through the transmission gate. In DVL gates, input *X* controls 2 transistor gate terminals, while input *Y* controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to *X* and *Y* as the control signal and propagate signal of the gate, respectively.

IV. ADIABATIC CIRCUITS

The term “adiabatic” refers to the thermodynamic process that exchanges no energy with environment, and therefore there is no occurrence of power or energy dissipation. During the switching process, adiabatic technology reduces the power or energy dissipation and reuses some part of the energy by recycling it from the load capacitance.

Adiabatic circuits are basically low power circuits which use to conserve the energy by returning back its output energy to input, so that the same energy can be used for next operation.
Fig. 4 and Fig. 5 shows the Charging and Discharging in conventional CMOS circuit and Adiabatic System.

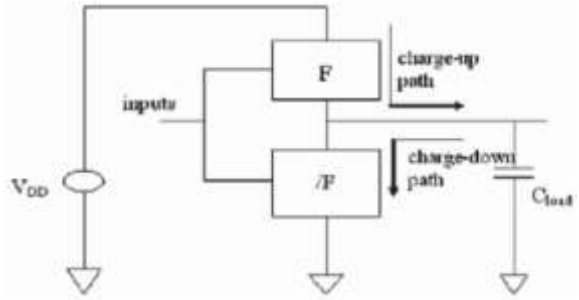

Fig 4. Charging and Discharging in Conventional system

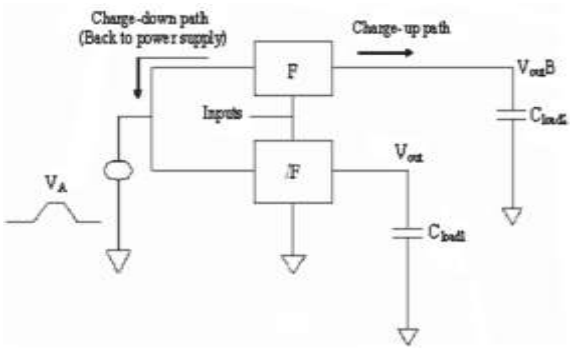

Fig 5. Charging and Discharging in Adiabatic system

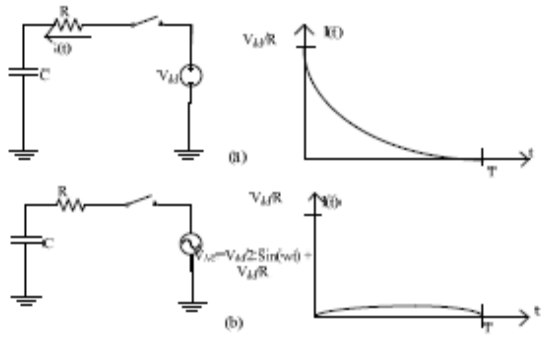

Fig. 6. (a) Switching of CMOS (b) Switching of Adiabatic Logic

Adiabatic circuits aims to conserve the charges by following essential rules

1) Avoiding turning on of transistor whenever there is a potential difference across the drain and source (VDS>0).

2) Avoiding turning off of Transistor whenever there is a flow of current through drain and source. (IDS~=0).

3) The current should not pass through diode.

Adiabatic Logic Types

V. SIMULATION

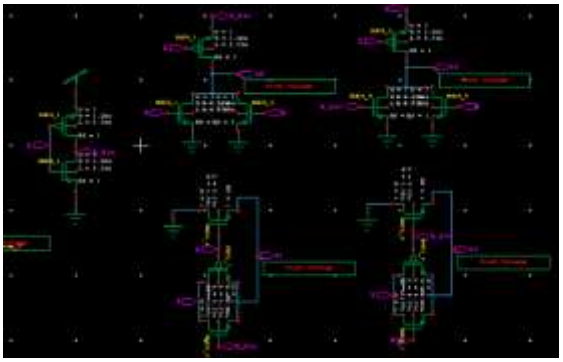

Fig.7 (a) Schematic of 2:4 Decoder LP

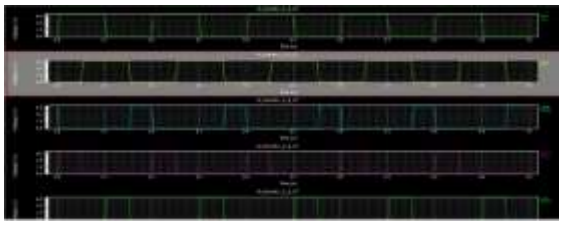

Fig. 7(b) Output result of 2:4 Decoder LP

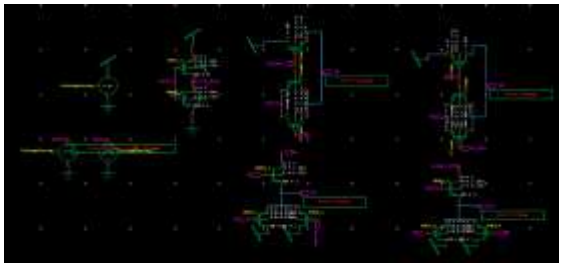

Fig.8(a) Schematic of 2:4 Decoder LPI

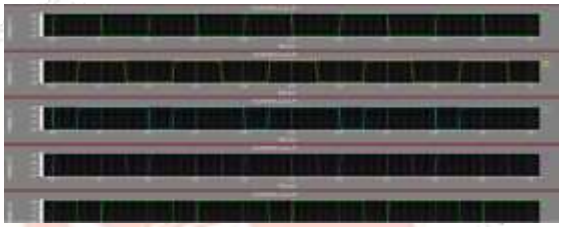

Fig. 8(b)Output result of 2:4 Decoder LPI

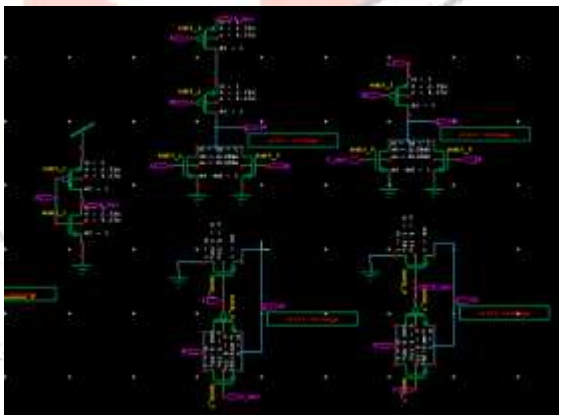

Fig.9 (a) Schematic of 2:4 Decoder HP

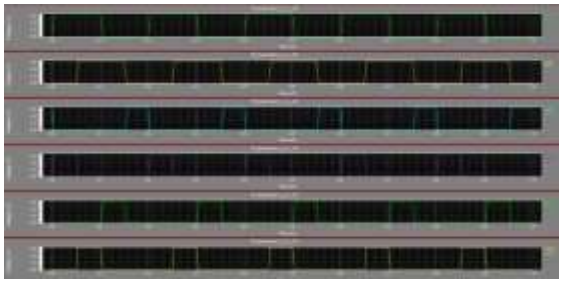

Fig.9 (b) Output result of 2:4 Decoder HP

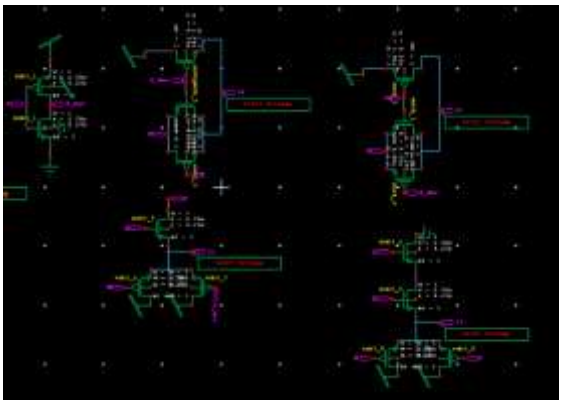

Fig.10 (a) Schematic of 2:4 Decoder HPI

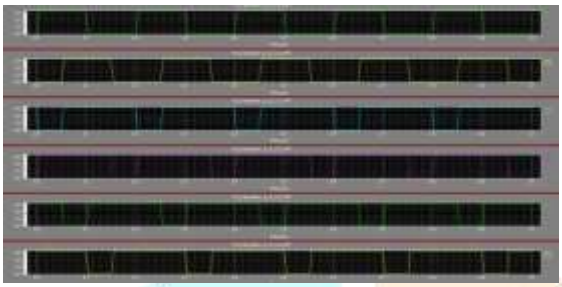

Fig.10 (b) Output result of 2:4 Decoder HPI

Conclusion:

Thus the various 2:4 decoder are studied and implemented. TGL and DVL cmos logic is studied. The use of these logic to implement basic gate to implement decoder The new design with respect to adiabatic technique reduce the power dissipation.Adiabatic design is optimize way of design for low power circuits.

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