RECTANGULAR WINDOW FUNCTION BASED DESIGN AND IMPLEMENTATION OF ADVANCED APPROXIMATE ADDER DESIGN UNDER 125NM CMOS TECHNOLOGY FOR FFT APPLICATIONS

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Abstract—The Adders are one of the key components in arithmetic circuits. The addition of two binary numbers is the fundamental and most often used arithmetic operation. In nearly all digital IC designs today, the addition operation is one of the most essential and frequent operation. Instruction sets for DSP's and general purpose processors include atleast one type of addition. In this Approximated Address is implemented using Transmission Gate, Pass Transistor, power Gating, Waveform Shaping and its power analysis and FFT analysis for Hamming Window are taken at 125nm technology.

Keywords—Transmission gates, Pass transistors, CMOS logic, 125nm Technology, Predictive Technology Model, *Supply voltage*

I. INTRODUCTION

A. Transmission Gate

A transmission gate, or analog switch, is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The solid-state switch is comprised of a p MOS transistor and n MOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off. In principle, a transmission gate made up of two field-effect transistors, in which – in contrast to traditional discrete field-effect transistors – the substrate terminal (bulk) is not connected internally to the source terminal.

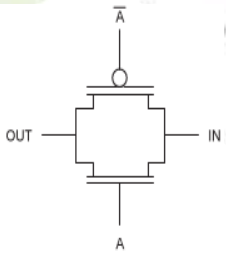


Fig. 1 : A Simple Transmission Gate

B. Pass Transistor

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input.

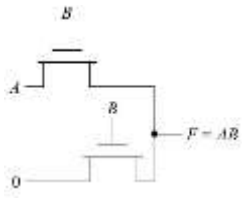


Fig. 2 : A Simple Pass Transistor

C. Power Gating

Power gating is a low power technique in deep sub micron technologies. Power gating is performed by shuting down the power for a portion of the design in order to reduce the static(leakage) power in design. Power switch(ps) cell is basic element which is used in power gating technique to shutting down the power for the portion of the design. The ps cell is also known as power management cell. Power gating is used to save the leakage power when the system is not in operation. This is accomplished by adding a switch either to VDD or VSS supply. When the design is power gated it literally means the block is powered OFF. Powering OFF a design block is the most beneficial technique of all the low power techniques because you dissipate near zero power. Near zero because the switching circuit used for implementing power gating still dissipate leakage power even in power gating mode. The control to the power gating switching circuit is generated by the Power gating control block.

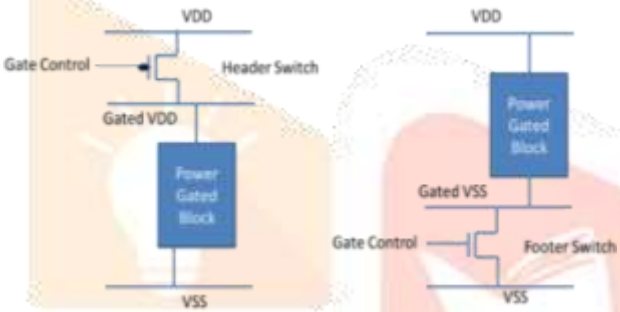


Fig. 3: A Simple Power Gating Circuitry

II. BACK GROUND

A. DSP Filter

In signal processing system ,they perform so many mathematical operation in digital filter for sampled ,in discrete-time-signal to reduce some aspects of that signal. The various types of filter are electronic filter ,analog filter which is operating on continuous-time analog signals and the filters are under electronic circuit. For sample the input signal ,a digital filter is usually consists of analog to digital converter ,which was comes under microprocessor and some components such as storing the data in the memory, and filter co- efficient etc., finally the output stage was done by digital to analog converter.

Digital filters are use in our everyday life in a form of electronics and it is used as a essential element such as radios, mobile phones, AV receivers for general purpose microprocessor, used in high performance applications instead of using FPGA or ASIC due to other delays in implementation we convert analog-to-digital and digital-to-analog conversions and anti-aliasing filters to reduce some problematic latency.

Then the order is greater of n or m .infinite impulse response behavior is in the form of recursive filter ,then the denominator is equal to unity.(i.e) FIR or finite impulse response has no feedback .the digital filter analysis behaviour is identified by the variety of mathematical techniques .one characteristics of the filters will respond only to a simple input such as an impulse. for more complex signals we will extend this information to compute the filter's response .the kronecker delta function is a measurement of how a filter will respond for the impulse response and it is denoted by h[k] or hk ,the sequence of filter coefficients:

$$Yn = \sum_{K=0}^{N} h_k \, x_{n-k}$$

IIR filters are recursive in nature ,the output depends on current of both previous inputs as well as previous outputs .the transfer of the discrete-time systems in digital filter is converting to a constant-coefficient equation(LCCD) via the z-transform.the ratio of two polynomials of the transfer function is in discrete frequency-domain. a signal extracts from the frequency spectrum is in a form of mathematical algorithm and many of the digital filters are based on the fast fourier transforms .state-space model is the another form of a digital filter. state-space filter is used as kalman filter. it is published in the year 1960,by Rudolf kalman.

Attenuation is based by the traditional linear filters .when nonlinear filters are designed ,the transfer filters having energy which allows the energy to move user in designed way .so that the new frequency bands of effects or unwanted noise are moved, either it is lower or higher in frequency ,it will spread on the frequency ranges. In filter design degrees of freedom are introduced and it is a energy transfer filters then it is opposite for traditional filter designs. The non linear dynamics of digital energy transfer are very easy to implement.

B. FFT (Fast Fourier Transform)

A fast Fourier transform (FFT) is an algorithm to sample a signal over a period of time (or space) and divides it into frequency components. These components are single sinusoidal oscillations at distinct frequencies each with their own amplitude and phase. Over the time period measured, the signal contains 3 distinct dominant frequencies.

Fast Fourier transforms are widely used for many applications in engineering, science, and mathematics. The basic ideas were popularized in 1965, but some algorithms had been derived as early as 1805. In 1994, Gilbert Strangdescribed the FFT as "the most important numerical algorithm of our lifetime. There are many different FFT algorithms based on a wide range of published theories, from simple complex-number arithmetic to group theory and number theory.

The DFT is obtained by decomposing a sequence of values into components of different frequencies. This operation is useful in many fields but computing it directly from the definition is often too slow to be practical. An FFT is a way to compute the same result more quickly: computing the DFT of N points in the naive way, using the definition, takes O(N)2 arithmetical operations, while an FFT can compute the same DFT in only O(N log N) operations. The difference in speed can be enormous, especially for long data sets where N may be in the thousands or millions. In practice, the computation time can be reduced by several orders of magnitude in such cases, the improvement is roughly proportional to n{ /}/ log n.

This huge improvement made the calculation of the DFT practical; FFTs are of great importance to a wide variety of applications, from digital signal processing and solving partial differential equations to algorithms for quick multiplication of large integers.

Let x0, ..., xN−1 be complex numbers. The DFT is defined by the formula {X_{k}=sum_{n=0}^{N-1}x_{n}e^{-i2\pi kn/N}\qquad k=0,\dots ,N-1.}

$$X_k = \sum_{n=0}^{N-1} x_n e^{-i 2\pi k n / N} \quad k=0,\ldots,N-1$$

Evaluating this definition directly requires O(N2) operations, there are N outputs Xk, and each output requires a sum of N terms. An FFT is any method to compute the same results in O(N log N) operations. All known FFT algorithms require (N log N) operations, although there is no known proof that a lower complexity score is impossible. Evaluating the DFT's sums directly involves N2 complex multiplications and N(N−1) complex additions, of which O(N) operations can be saved by eliminating trivial operations such as multiplications by 1. The radix-2 Cooley–Tukey algorithm, for N a power of 2, can compute the same result with only (N/2)log2(N) complex multiplications and N log2(N) complex additions. In practice, actual performance on modern computers is usually dominated by factors other than the speed of arithmetic operations and the analysis is a complicated subject but the overall improvement from O(N2) to O(N log N) remains.

The best known use of the Cooley–Tukey algorithm is to divide the transform into two pieces of size N/2 at each step, and is therefore limited to power-of-two sizes, but any factorization can be used in general . These are called the radix-2 and mixed-radix cases, respectively . Although the basic idea is recursive, most traditional implementations rearrange the algorithm to avoid explicit recursion. Also, because the Cooley–Tukey algorithm breaks the DFT into smaller DFTs, it can be combined arbitrarily with any other algorithm .

Indeed, Winograd showed that the DFT can be computed with only O(N) irrational multiplications, leading to a proven achievable lower bound on the number of multiplications for power-of-two sizes; unfortunately, this comes at the cost of many more additions, a tradeoff no longer favorable on modern processors with hardware multipliers. In particular, Winograd also makes use of the PFA as well as an algorithm by Rader for FFTs of prime sizes.

$$nk=nk = -\frac{(k-n)^2}{2} + \frac{n^2}{2} + \frac{k^2}{2}$$

Hexagonal Fast Fourier Transform aims at computing an efficient FFT for the hexagonally sampled data by using a new addressing scheme for hexagonal grids, called Array Set Addressing (ASA).

C. Noise

In signal processing, noise is a general term for unwanted (and, in general, unknown) modifications that a signal may suffer during capture, storage, transmission, processing, or conversion.Sometimes the word is also used to mean signals that are random (unpredictable) and carry no useful information; even if they are not interfering with other signals or may have been

introduced intentionally, as in comfort noise. Noise reduction, the recovery of the original signal from the noise-corrupted one, is a very common goal in the design of signal processing systems, especially filters. The mathematical limits for noise removal are set by information theory, namely the Nyquist–Shannon sampling theorem.

D. Carrier to Noise Ratio

In telecommunications, the carrier-to-noise ratio, often written CNR or C/N, is the signal-to-noise ratio (SNR) of a modulated signal. The term is used to distinguish the CNR of the radio frequency pass band signal from the SNR of an analog base band message signal after demodulation, for example an audio frequency analog message signal. If this distinction is not necessary, the term SNR is often used instead of CNR, with the same definition. Digitally modulated signals (e.g. QAM or PSK) are basically made of two CW carriers (the I and Q components, which are out-of-phase carriers) . In fact, the information (bits or symbols) is carried by given combinations of phase and/or amplitude of the I and Q components. It is for this reason that, in the context of digital modulations, digitally modulated signals are usually referred to as carriers.

Therefore, the term carrier-to-noise-ratio (CNR), instead of signal-to-noise-ratio (SNR) is preferred to express the signal quality when the signal has been digitally modulated. High C/N ratios provide good quality of reception, for example low bit error rate (BER) of a digital message signal, or high SNR of an analog message signal. The carrier-to-noise ratio is defined as the ratio of the received modulated carrier signal power C to the received noise power N after the receiver filters.

E. Signal to Noise Ratio

Signal-to-noise ratio (abbreviated SNR or S/N) is a measure used in science and engineering that compares the level of a desired signal to the level of background noise. S/N ratio is defined as the ratio of signal power to the noise power, often expressed in decibels. Signal-to-noise ratio is sometimes used metaphorically to refer to the ratio of useful information to false or irrelevant data in a conversation or exchange. For example, in online discussion forums and other online communities, off-topic posts and spam are regarded as "noise" that interferes with the "signal" of appropriate discussion. Signal-to-noise ratio is defined as the ratio of the power of a signal

III. EXISTING SYSTEM

In this paper a new high speed Approximate Adder will be introduced, which will reduce the hardware complexity and make justice with SPAA metrics. Adders are one of the key components in arithmetic circuits. Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. For applications related to human senses, approximate arithmetic can be used to generate sufficient results rather than absolutely accurate results. Approximate design exploits a tradeoff of accuracy in computation versus performance and power.

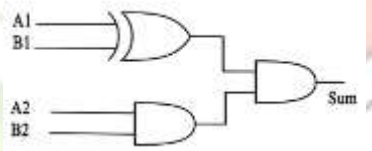
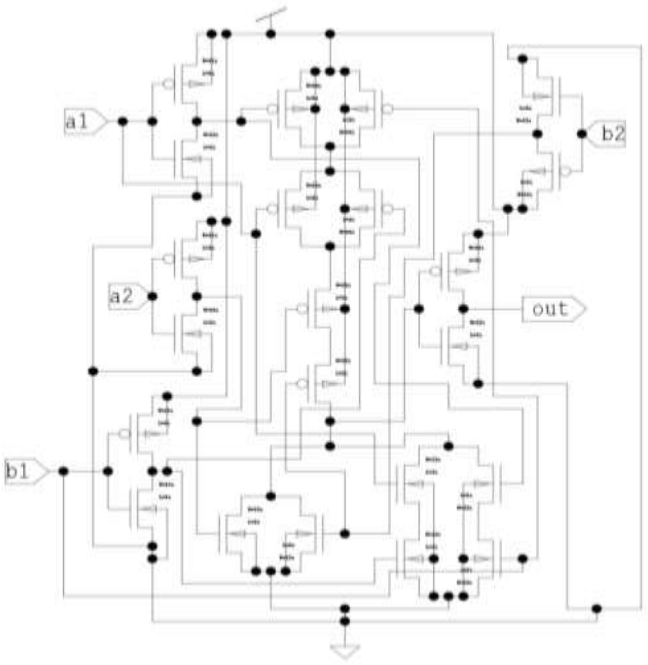


Fig . 4 : Approximate Adder

IV PROPOSED WORK

The two transistors, an n-channel MOSFET and a p-channel MOSFET, are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a NOT gate (inverter), to form the control terminal. The values at n-gate and p-gate are expected to be opposite to each other. If p-gate is 0 while n-gate is 1, then the value found at source is transmitted to drain. If p-gate is 1 while p-gate is 0, then the connection is broken, so the value at drain is left floating. In all other cases, drain receives an error output — unless source is floating, in which case drain is floating as well. The circuits are implemented using the transmission gates and pass transistor logic.



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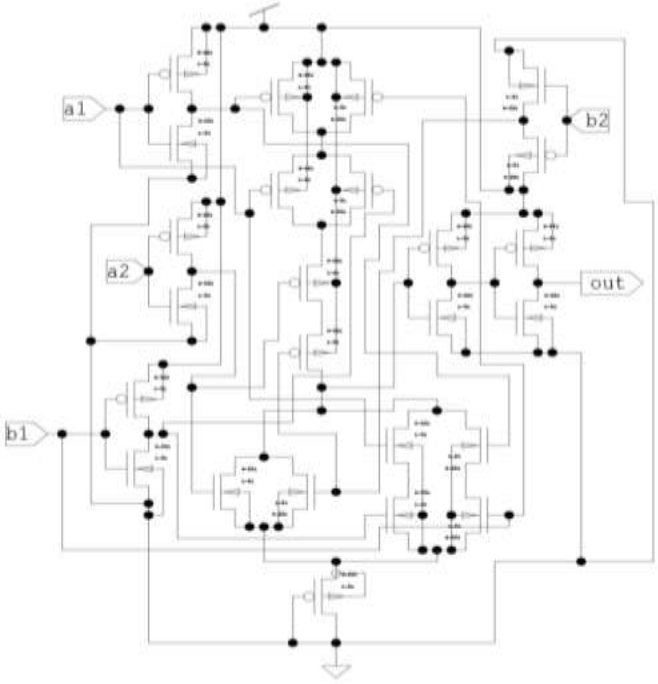

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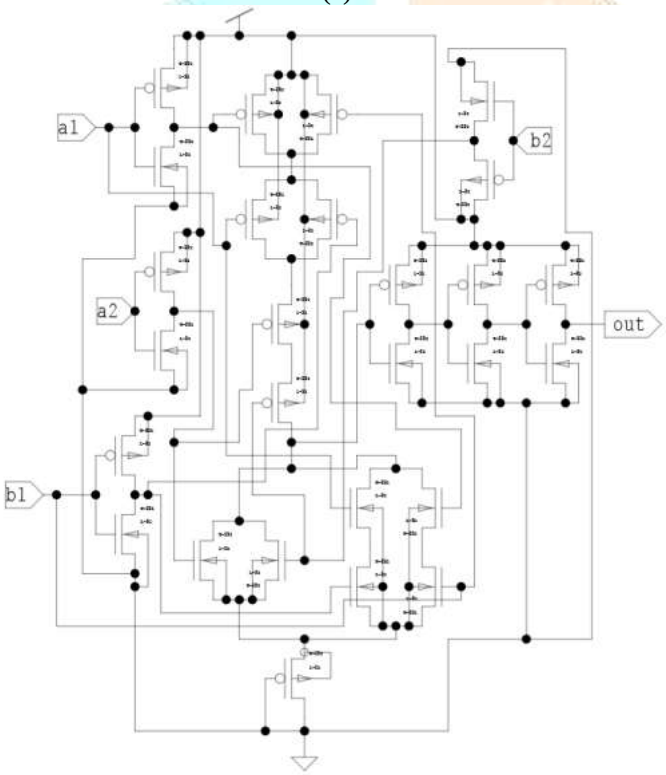

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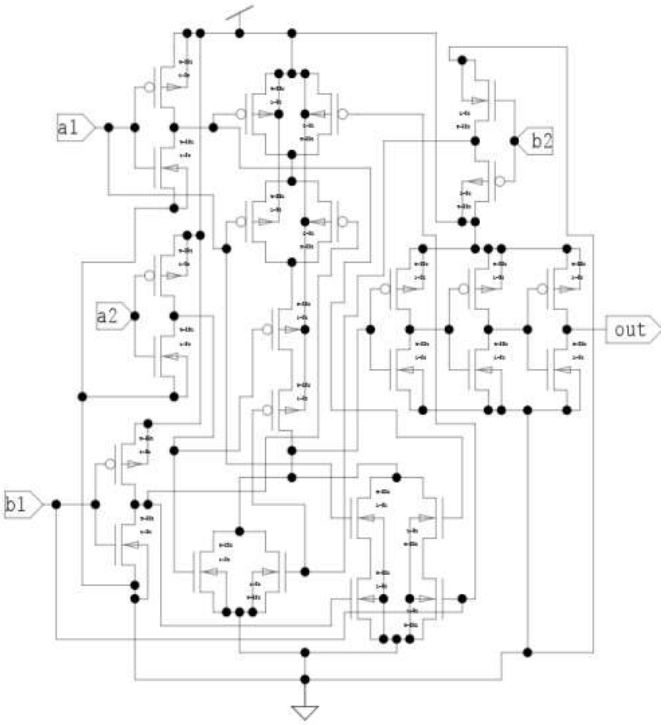
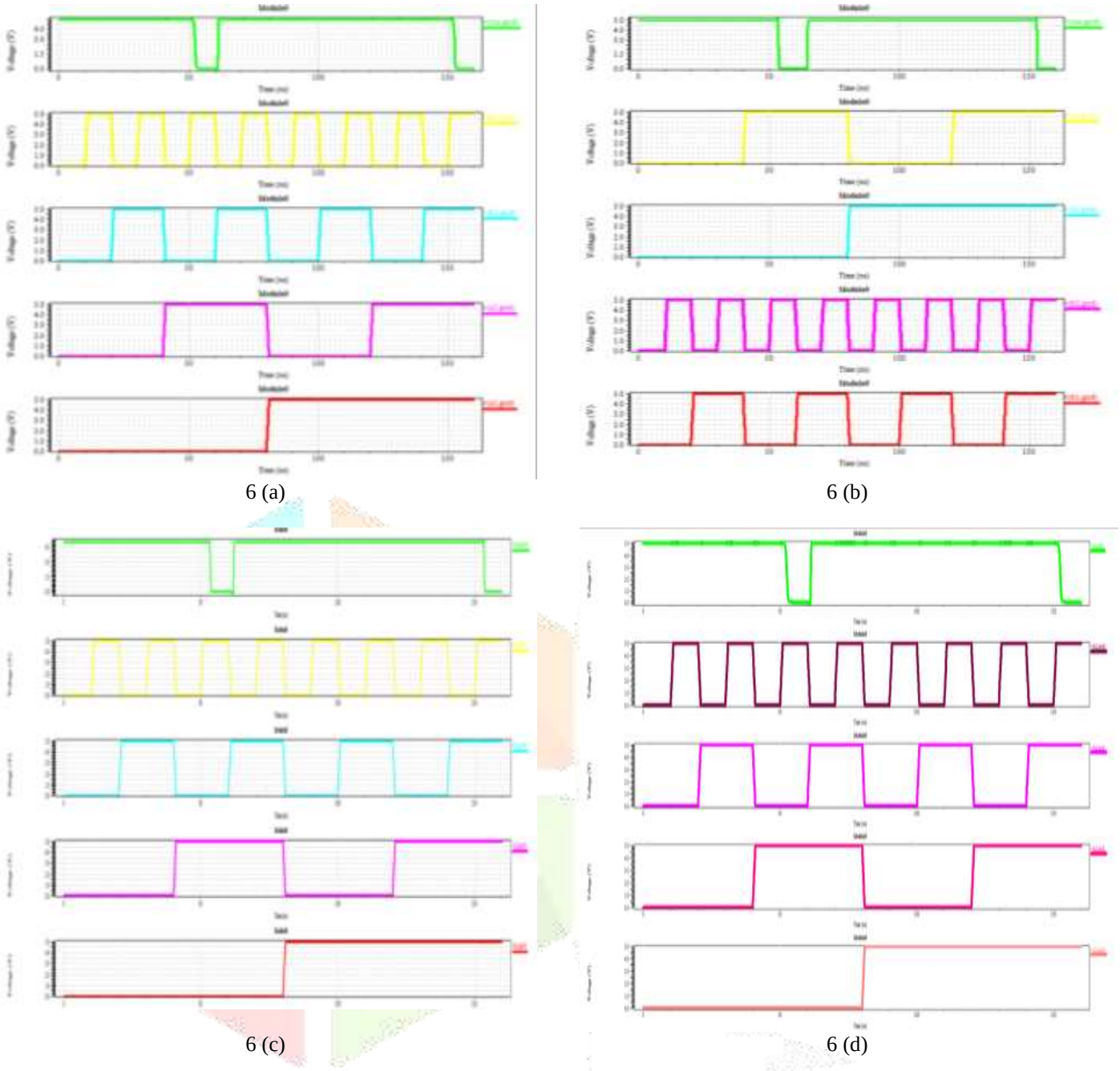


5 (d)

Figure 5. (a) Design of Approximate Adders Using Transmission Gates (AATG) at 125nm technology. The design was implemented for the low power and low area circuits (b) The approximate Adders was implemented using Power Gating (AAPG) for the best output analysis (c) The Approximate Adder output Waveform was shaped using the grounded PMOS technology (AAWT) (d) the approximate Adders was designed successfully using pass Transistor (AAPT) logic for the fast processing of inputs. This paves a way for the fast propogation of the inputs to the outputs.



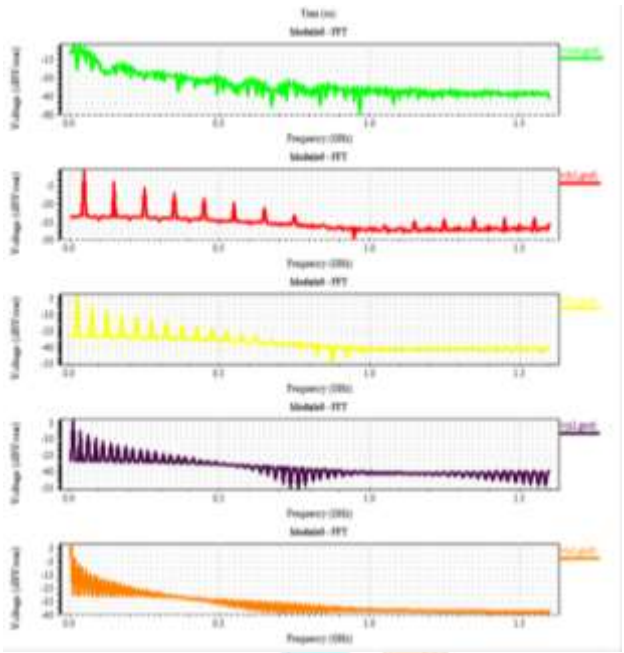
6 (a) 6 (b)

6 (c) 6 (d)

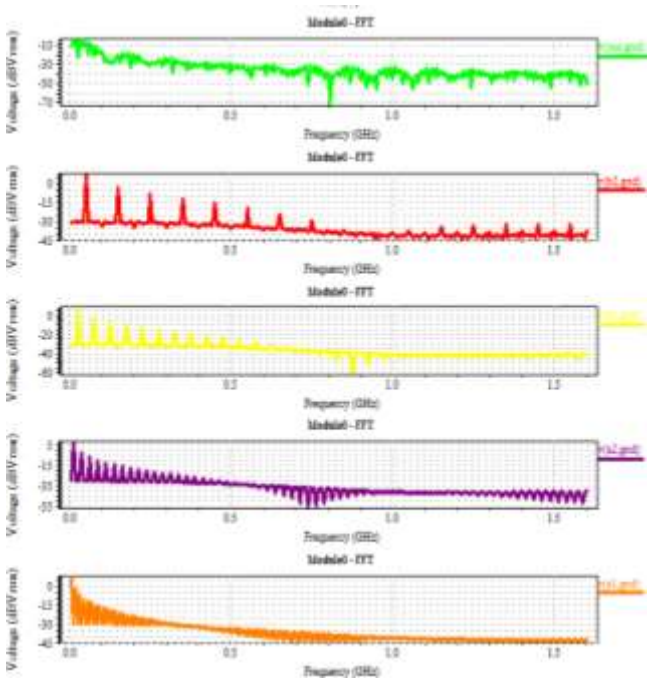
Fig. 6 (a) Waveform for the design of Approximate Adders Using Transmission Gates (AATG) at 125nm technology 6 (b) Waveform of an approximate Adder which was implemented using Power Gating (AAPG) for the best output 6 (c) Waveform Shaping using the grounded PMOS technology (AAWS) 6 (d) Wave form of the approximate Adders was designed successfully using pass Transistor logic (AAPT) for the fast processing of inputs

A. Window Function

In signal processing, a window function also known as an apodization function or tapering function is a mathematical function that is zero-valued outside of some chosen interval. For instance, a function that is constant inside the interval and zero elsewhere is called a rectangular window, which describes the shape of its graphical representation. When another function or waveform/data-sequence is multiplied by a window function, the product is also zero-valued outside the interval: all that is left is the part where they overlap, the "view through the window". A more general definition of window functions does not require them to be identically zero outside an interval, as long as the product of the window multiplied by its argument is square integrable, and, more specifically, that the function goes sufficiently rapidly toward zero.



7 (a)



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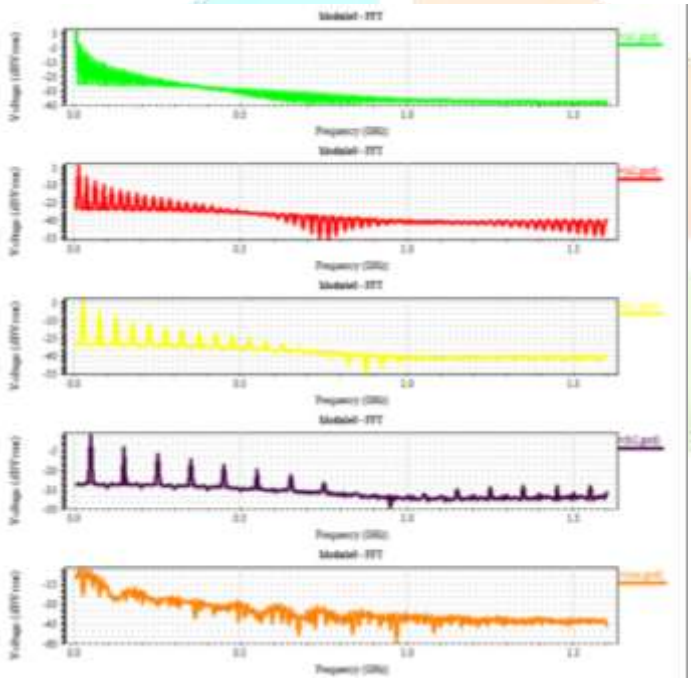

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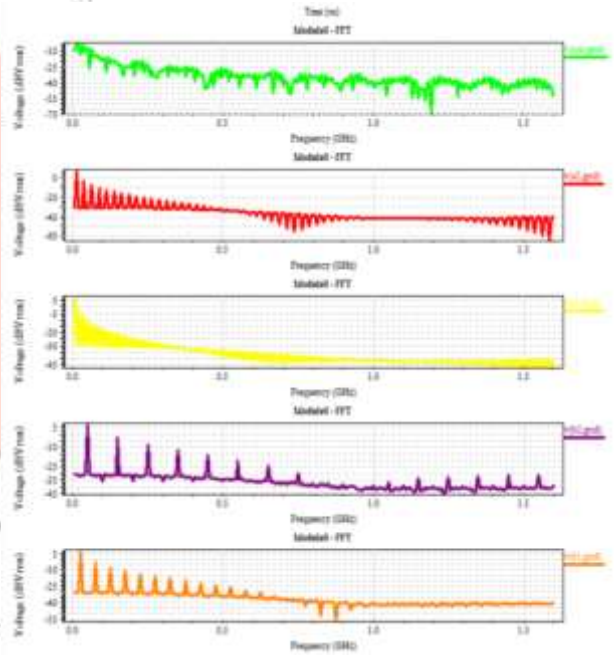

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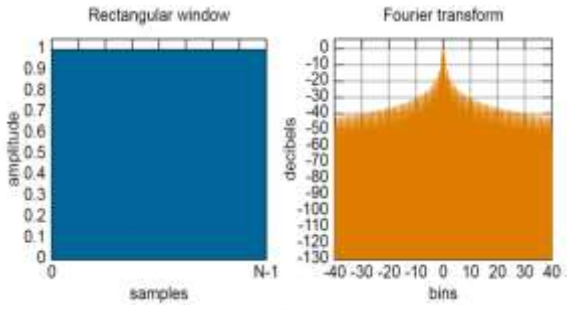

7 (e)

Fig. 7 : Rectangular Window function for the approximate adders $W_R(n)=1$ within the limits $-(N-1/2) <= n <= (N-1/2)$. The rectangular window (sometimes known as the boxcar or Dirichlet window) is the simplest window, equivalent to replacing all but *N* values of a data sequence by zeros, making it appear as though the waveform suddenly turns on and off. The figure 7 (a-d) corresponds to 5 (a-d). And the 7 (e) is the simple rectangular window function .

B. Power Analysis of Various Approximate Adders

TYPE	V5	AVERAGE POWER	MAX POWER	MIN POWER
AATG	0 to 1.6e-007	6.48e+000watts	3.40e-002 at time 8.09e-008	7.15e-008 at time 14e-007

AAPT	0 to 1.6e-007	1.48e+001watts	3.42e-002 at time 8.09e+008	1.30e-007 at time 9.25e+008
AAPG	0 to 1.6e-007	9.23e+000 watts	3.33e-002 at time 8.09e-008	1.14e-007 at time 1.13e-007
AAWS	0 to 1.6e-007	7.78e+000 watts	3.42e-002 at time 8.09e-008	1.77e-007 at time 1.05e-007

C. Truth Table

A1	A2	B1	B2	P1	P2	P3	P4	P5	P6	N1	N2	N3	N4	N5	N6	Y
0	**0**	**0**	**0**	OFF	OFF	ON	OFF	OFF	ON	ON	ON	OFF	ON	ON	OFF	1
0	**0**	**0**	**1**	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	1
0	**0**	**1**	**0**	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	1
0	**0**	**1**	**1**	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	1
0	**1**	**0**	**0**	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	OFF	1
0	**1**	**0**	**1**	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	0
0	**1**	**1**	**0**	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	1
0	**1**	**1**	**1**	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	1
1	**0**	**0**	**0**	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	1
1	**0**	**0**	**1**	OFF	ON	OFF	OFF	ON	ON	ON	OFF	ON	ON	OFF	OFF	1
1	**0**	**1**	**0**	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	1
1	**0**	**1**	**1**	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	1
1	**1**	**0**	**0**	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	1
1	**1**	**0**	**1**	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	1
1	**1**	**1**	**0**	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	1
1	**1**	**1**	**1**	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	0

V CONCLUSION

Thus the Approximate Adders is done using model file ML125 and its output waveform and the FFT analysis for Hamming window is taken. And its power analysis for different techniques is also taken. These techniques are performed for various types such as Transmission Gate, Pass Transistor, Power Gating and Waveform Shaping are done. What cannot be seen from the graphs is that the rectangular window has the best noise bandwidth, which makes it a good candidate for detecting low-level sinusoids in an otherwise white noise environment. Interpolation techniques, such as zero-padding and frequency-shifting, are available to mitigate its potential scalloping loss.

Further enhancement can be done by using various low power logic and design in the lower nm technology. The further reduction of the CMOS technology, the transistor behavior is changed and it can be used to analyse various parameters which can be used for the different kinds of DSP applications.

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