Low Power High Speed Optical Interconnection Network at 1550nm Wavelength

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***Abstract*— In this paper, we transmitted the electrical power using vertical cavity surface emitting laser with wavelength range 1550nm due to this we use the International Technology Roadmap for Semiconductors (ITRS) is used as a reference data to fulfill the requirements of electrical Integrated Circuits must satisfy to successfully perform copper interconnects (IEs). By using opti-system software we ultimately solve the power dissipation and obtain high-performance models.**

Keywords- **Integrated optoelectronic circuits, optoelectronics, optical interconnects (ICs), silicon photonics.**

I. INTRODUCTION

In future communication systems it is identified that some challenges in the steps of VLSI IC's. The two major challenges and issues regarding interconnect challenges is power dissipation and delay, which can also be obtained by using faster interconnect elements in different parts of a processor.

Optical interconnects (OIs) will provide a solution to the communication integrated circuit after replacing the electrical interconnect with high speed optical interconnect using optical waveguides. Generally the three levels of interconnect can comes under which are as follows:

1. Board – to – Board
2. Chip – to – Chip
3. Intrachip

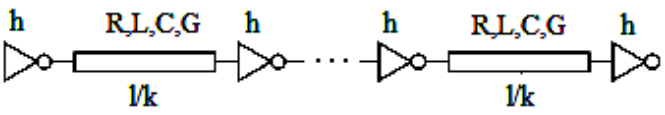
While at present the major development is being done on the optical interconnect which is in future also. To support the sufficient density of interconnections and integration with CMOS circuit processing, OIs should be monolithically fabricated using CMOS compatible silicon-based materials and processes. Until recently, such devices did not exist. Over the past some years, a significant results has been achieved in the development of silicon-based building blocks for on-chip OIs, including light sources waveguides, modulators and detectors.
At present some results comes under regarding optical interconnect but that is not justified, so the research regarding optical interconnect is being done at present. In this research paper, the International Technology Roadmap for Semiconductors (ITRS) is used as reference for data, the EI performance, the complete paper is covered in various part which are as follows: a basic theory of transmission line when considered as a distributed RLCG model is discussed in section 2. OIs VERSUS EIs is shown in section 3, section 4 explains the results. In section 5 conclusion justifies the paper work, section 6 shows the references.

II. Basic Theory

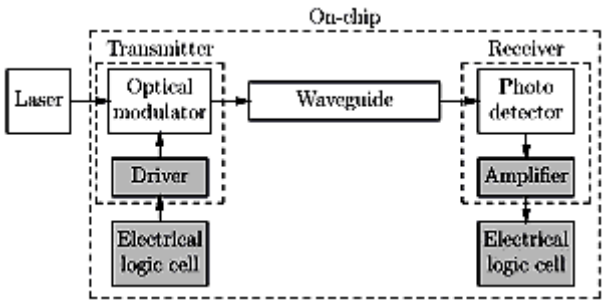
Modern on-chip EIs utilizes copper wires surrounded by a low k-dielectric to transmit a signal. If we consider long wires used in global interconnects than we see it has higher RC time constants, which increases the delay (rise time, peak time, settling time and maximum overshoot), power dissipation and crosstalk.

In sub micrometer CMOS, generally repeaters (or electrical signal amplifiers) are mainly used to break long routing wires into smaller parts, as shown in Fig. 1(a).

Repeaters generally used to drive smaller segments, thereby reducing the interconnect delay which increase speed and making a overall delay linear with the line length rather than simultaneous. The delay due to the interconnect wires becomes smaller by increasing the number of repeaters, but there is a delay and power parameters associated with the repeater circuitry. Therefore, To fixed interconnects geometry, there must exists an optimal repeater size in circuitry and spacing to achieve a minimum delay in overall circuit. In the following discussion, only EIs with optimized repeaters are considered.



(a)



(b)

Fig.1. (a) Repeater insertion in an R,L,C,G interconnect. (b) Block diagram of an on-chip optical data path.

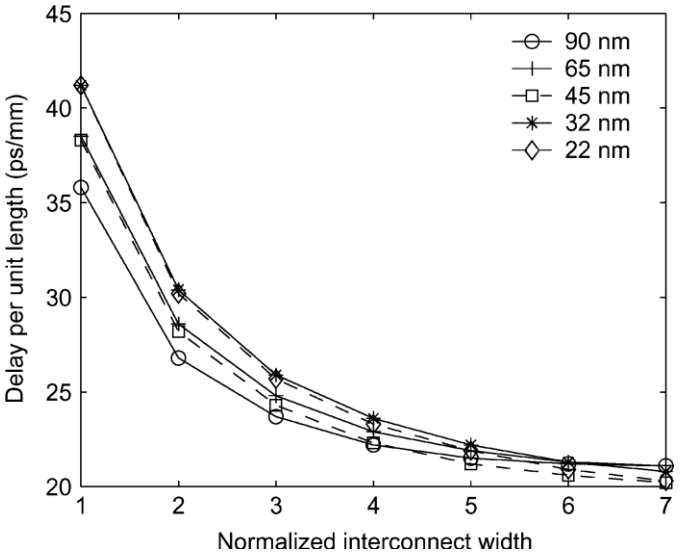
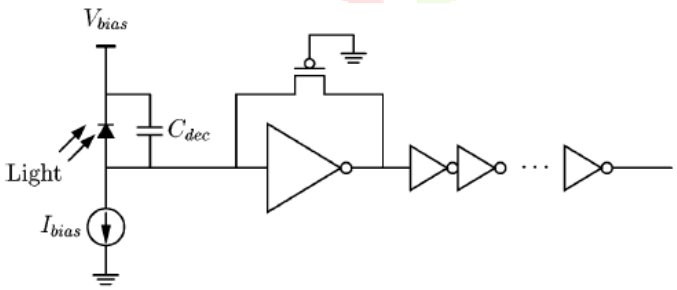


Fig.2. Propagation delay of EI at different technology nodes versus normalized interconnect width.

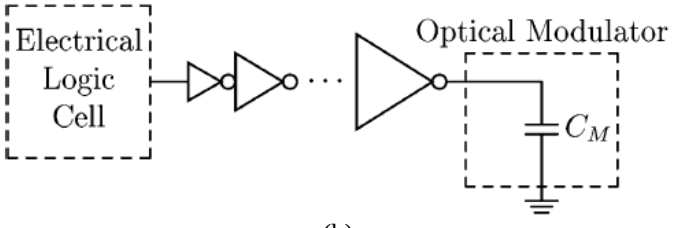
During modeling metal wire interconnects which work in multi gigahertz clock rates, it is very important to consider four impedance characteristics of the wire- resistance, capacitance and inductance.

In this paper, we used an RLCG interconnect with same spaced repeaters is examined for different technology nodes. Three degrees of freedom—the wire width, and the number and size of the repeaters—are explored to determine the minimum signal propagation delay. Generally the delay model for the electrical interconnect is used to consider the effects of repeater output capacitance and transition time response. Two of the main parameters characterizing on-chip interconnects are the propagation delay and the interconnect bandwidth density.

III. OIs VERSUS EIs



(a)



(b)

Fig. 3 Circuit Schematic of (a) Optical receiver and (b) Modulator driver

An optical interconnection network is used for connecting various optical and electrical devices which is used for transmitter and receiver end. First in fig 3 (b) modulator driver is used for transmitting the optical signal after converting from electrical to optical and in fig 3 (a) the optical signal is detect by optical receiver by using photo diode and than it is converted into electrical signal at the end point of receiver.

IV. RESULTS

Total electrical power transmitted and received is $500*10^{-3}$ Watt. , at wavelength 1550nm and $250*10^{-3}$ Watt. At frequency 1200nm. Optical Fiber Length of 10µm having different power at different wavelength given below.

Table 1. Table shows power obtained at the output of VCSEL. at different wavelength.

S.NO	FREQ.	POWER IN WATT. (10^{-3})	POWER IN dBM
1	1550	2.899	4.623
2	1200	3.745	5.735
3	1150	3.907	5.919

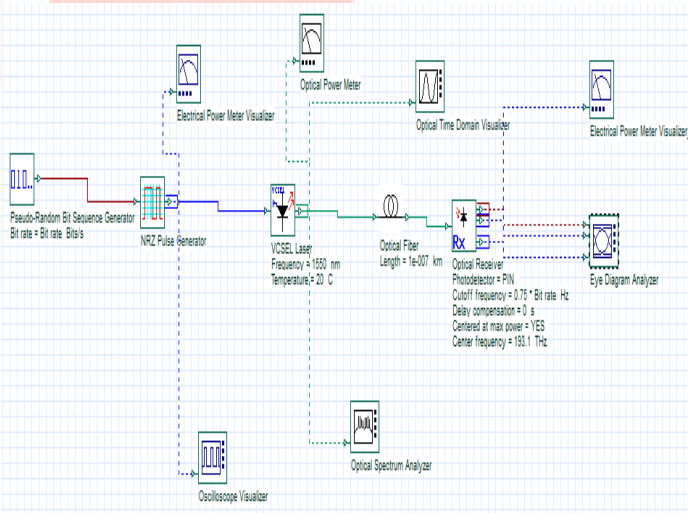


Fig. 4 Circuit Diagram of VCSEL with wavelength range 1550nm.

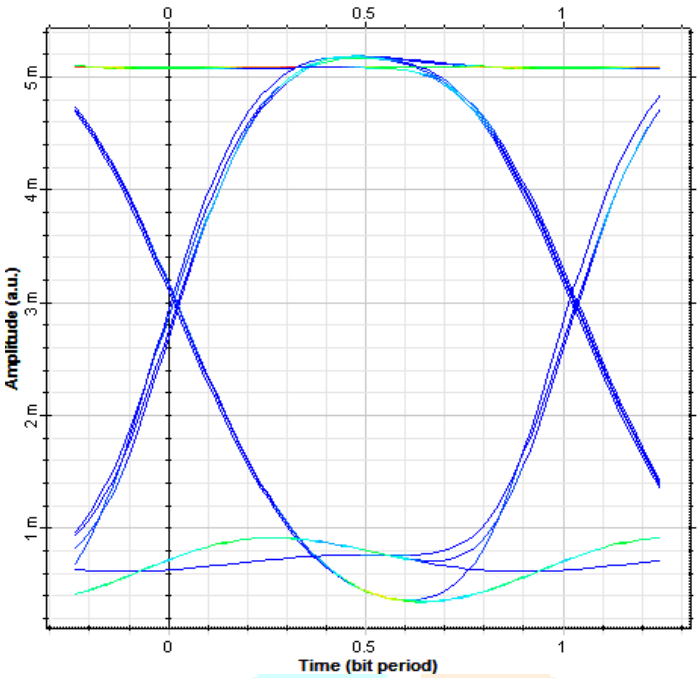


Fig. 5 Eye Diagram at freq. 1550nm

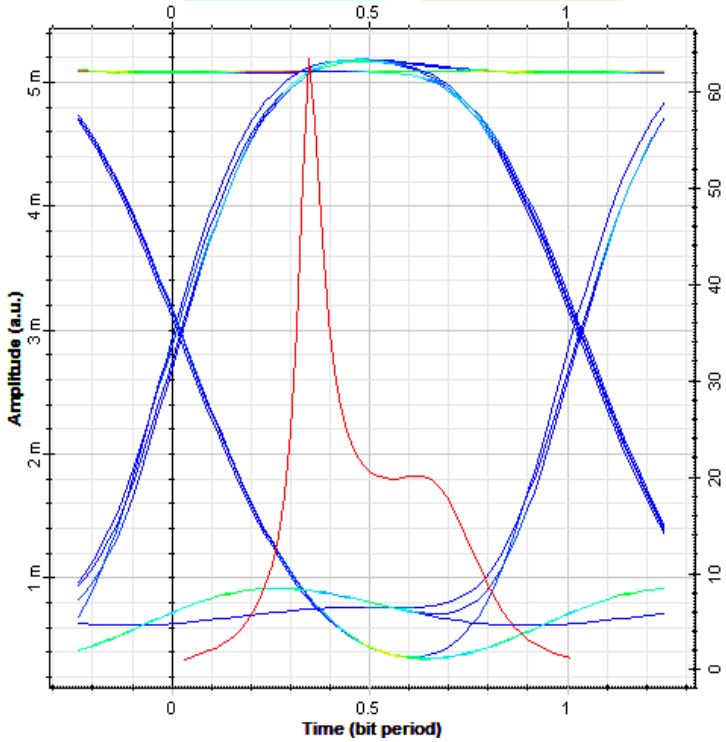


Fig. 6 Q Factor at freq. 1550nm

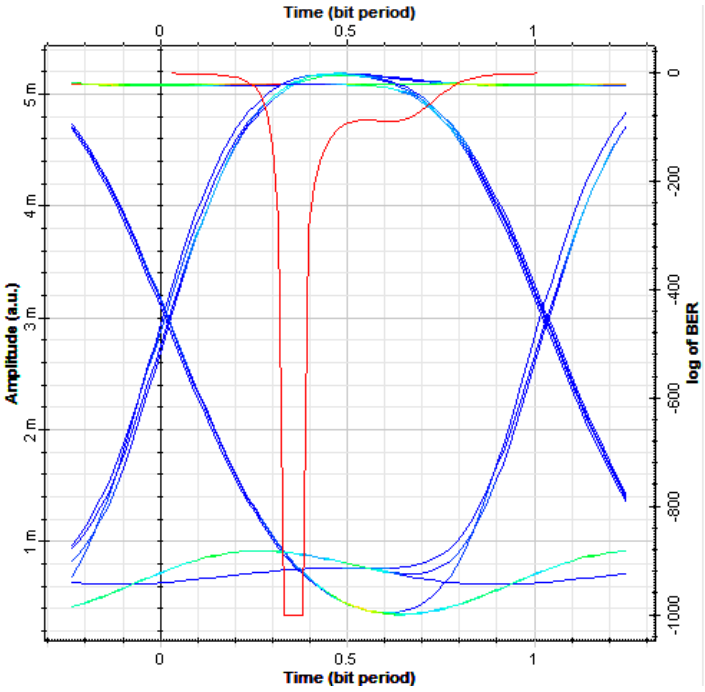


FIG. 7 MIN BER AT FREQ. 1550NM

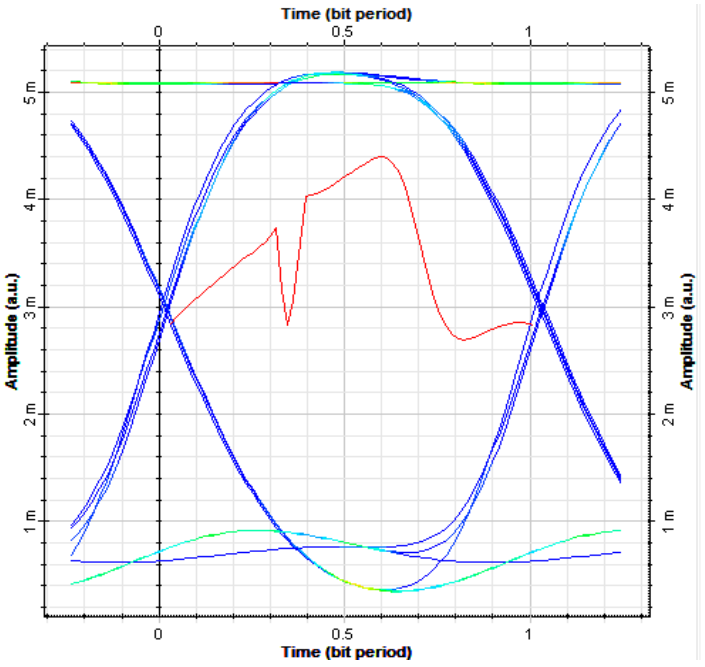


FIG. 8 THRESHOLD VOLTAGE AT FREQ. 1550NM

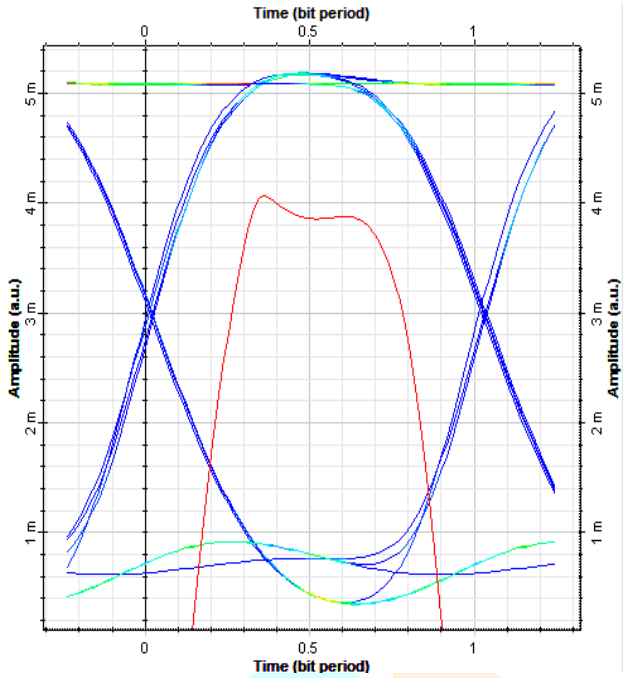


FIG. 9 HEIGHT AT FREQ. 1550NM

V. CONCLUSION

In this paper, the performance characteristics of optical multimode fiber with 1cm length, clearly shows the power dissipation in the network. In this VLSI On-Chip Optical Interconnect, we consider both optical transmitter and optical receiver components in the circuit which provide the outputs in terms of power and delay which clearly shows the power dissipate in 1cm optical multimode fiber is in µw.

VI. CONCLUSION

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