Design and Performance Analysis of VLSI Circuits in 180nm Technology

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Abstract: The proposed 3T NAND and 3T NOR gate gives the better performance measures in terms of reduced dynamic power, area and high speed than 4T NAND and 4T NOR gate respectively. Finally, a Single Transistor Clocked Explicit Pulse Triggered Flip Flop (STCEPFF) circuit is Designed with the proposed 3T NAND gate.

IndexTerms **- 4TNAND, 3TNAND, 4TNORN, 3TNOR gate, low power, low area, delay and VLSI.**

I. INTRODUCTION

This presents an area and energy efficient universal NAND and NOR gates. The proposed three transistors (3T) based gates are just as effective for dynamic power control in CMOS VLSI circuits for system on a chip (SoC) applications. The proposed 3T NAND and 3T NOR gate gives the better performance measures in terms of reduced dynamic power, area and high speed than 4T NAND and 4T NOR gate respectively. Finally, a Single Transistor Clocked Explicit Pulse Triggered Flip Flop (STCEPFF) circuit is implemented with the proposed 3T NAND gate.
In order to realize ultra low power SoC applications, circuits should be operated with low power dissipating gates. In reality, all the essential logic functions being derived from collections of interconnected NANDs or NORs, digital control systems have been constructed almost with either NAND or NOR gates. Low power and high reliability needs along with cost/performance advantages make NAND flash memory the ideal data storage solution for portable electronics. The significance of a universal gate is that programs chips can be built up of only one kind of gate, either NAND or NOR gate making manufacturing process simple and reducing the numbers of different processors required to make a computer. The benefit of utilizing a combination of low-power components in conjunction with low-power design methodologies is more important now than ever before. Low power requirements continue to grow extensively as components become battery powered, smaller and require more functionality.

The system specifications are processor Intel (R) core (TM) i5-4570 CPU@3.20GHz.,3.20GHz.Installed memory (RAM) 4 GB (usable memory is 3.43GB) and system type: 32-bit operating system (OS).

This paper is formed as follows Section II presents the literature review on NAND gate, NOR gate and Single Transistor Clocked Explicit Pulse Triggered Flip flop Section III presents the methodology for 4TNAND, 3TNAND gate, 4TNOR, 3TNOR gate and Single Transistor Clocked Explicit Pulse Triggered Flip flop and also discussed the low power analysis. Section IV shows the simulation results and they are discussed clearly, finally the paper is concluded with Section V.

II. LITERATURE REVIEW

New approach for designing and realizing compact digital circuits by engineering (Metal-Oxide Semiconductor Field-Effect Transistor) MOSFET gate electrode is proposed. The novelty is the use of gate engineered single devices in the pull-up (PU) and pull down (PD) paths of a static (Complementary Metal-Oxide Semiconductor) CMOS gate instead of multiple transistors as used in conventional CMOS implementations of circuits. Herein, two input NAND, NOR, and exclusive-OR (XOR) gates employing the proposed gate engineering concept are designed and simulated. Engineered gate N-type MOS and P-type MOS are used for Pull Down and pull-up circuits, respectively. Mixed mode simulations have shown that the proposed technique realizes NAND, NOR and XOR operations perfectly and it can be extended to realize other combinational and sequential circuits easily [1].

The scaling of device dimensions has been used till date to improve the performance of devices. The scaling has improved the speed, power consumption, and packing density of integrated circuits. However, the further scaling of devices below 22/18 nm is extremely difficult due to severe short channel effects [2]. An alternative approach is to go for the multifunctional devices, wherein a transistor even can perform a circuit action. For example, a single transistor realizing an inverter action or a transmission gate action results in significant area reduction [3, 4]. A typical two input static CMOS NAND/NOR gate needs four transistors and an exclusive-OR (XOR)/XNOR gate needs eight transistors for their realizations using the conventional static CMOS technology. Various design techniques are available to reduce the transistor count of logic gates such as rationed logic, pseudo-N-type MOS (NMOS), transmission gate-based logic, differential cascade voltage switch logic, dynamic gates [5] etc. Most of these techniques need either n-logic or p-logic blocks for evaluation of inputs wherein p-logic and n-logic blocks are same as used in the static CMOS-based gates.

Sordan et al. [6] designed logic gates with a single grapheme transistor. Although this structure designs a two input NAND, XOR, and OR logic gates with a single transistor but it needs an input stage to ensure that applied gate voltage is average of two input voltages. This input stage leads to an extra area in the design of the circuit. In addition to that the operating voltage of 50 V is used, which is significantly large than the operating voltage of currently used sub-micron technology. Xu et al. [7] also uses similar concept to design logic gates with single molecular FETs, except the operating voltage is in smaller ranging from −2 to 2 V. Furthermore, XOR/XNOR gates can be designed with four transistors only [8, 9].

The logic gates NAND/NOR were mimicked by enzyme biocatalyzed reactions activated by sucrose, maltose and phosphate. The subunits performing AND/OR Boolean logic operations were designed using maltose phosphorylase and cooperative work of invertase/amyloglucosidase, respectively. The final output signal was amplified by a self-promoting biocatalytic system [10].
An architectural-based scaling strategy is presented which indicates that the optimum voltage is much lower than that determined by other scaling considerations. This optimum is achieved by trading increased silicon area for reduced power consumption [11].
The clock system is one of the most power consuming components in a VLSI circuit, accounting for 30–60% of the total power dissipation [12]. As flip–flops are the basic elements of the clock system, their choice and design has a profound effect both on reducing the power consumption and on providing more slack time for the time budget in high-performance systems. Thus, in order to achieve a high-performance system, the design of flip–flops is important. Performing better than traditional master–slave flip–flops, Pulse-triggered flip–flops are indicates by a simple structure, negative setup time and soft edge [13]. Various kinds of pulse-triggered flip–flops were recently proposed [14–16], including implicit-pulsed flip–flops and explicit-pulsed flip–flops. The pulse alternator of the explicit-pulsed flip–flop can be inter mutual by neighboring homogeneous flip–flops, contributing to less power dissipation than implicit-pulsed ones [17]. Dual-edge flip–flops can reduce the clock frequency to half that of the single-edge flip–flop while maintaining the same data throughput, so power dissipation is decreased [18].

III. DESIGN METHODOLOGY

1. CMOS 4T NAND

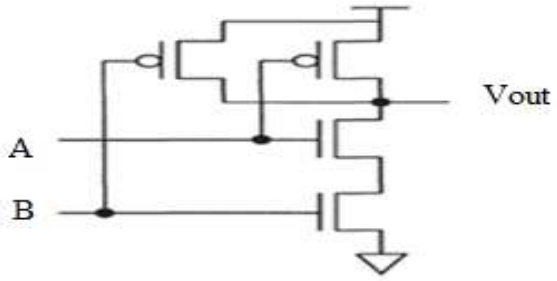

Figure 1: Conventional of CMOS 4TNAND gate

In Figure 1 Conventional of CMOS 4TNAND gate PMOS and NMOS transistors black diagram at inputs A, B and output is Vout. Koomey's law describes a long-term trend in the history of computing hardware and has actually been somewhat faster than Moore law.

2. CMOS 4T NOR gate

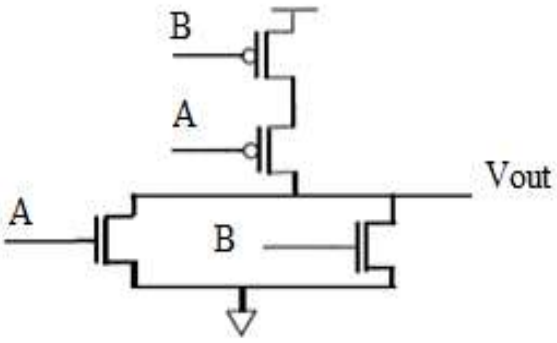

Figure 2: Conventional of CMOS 4T NOR gate

In Figure 2 CMOS 4TNOR gate block diagram PMOS and NMOS transistors black diagram at inputs A, B and output is Vout.

3. Single Transistor Clocked EPFF (STCEPFF)

In the circuit of EPFF shown in Figure 3, the 0-to-1 and 1-to-0 transitions follow different paths to the output. The 0-to-1 transitions need both the stages of the flip flop to reach the output whereas 1-to-0 transitions require only the second stage to reach the output. Hence the 0-to-1 propagation delay is high. An attempt is made to reduce this delay in Single Transistor Clocked Explicit Pulse triggered flip flop (STCEPFF).

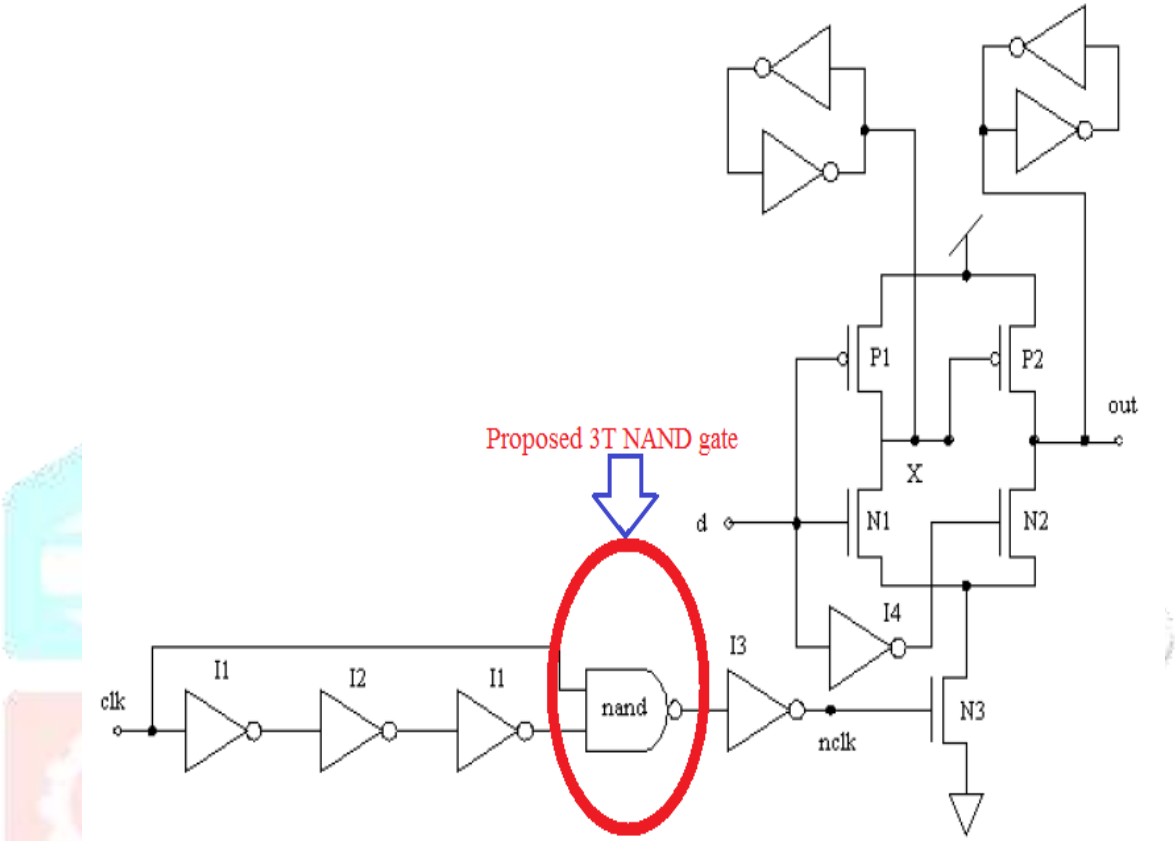

Figure 3: Single Transistor Clocked Explicit Pulse Triggered Flip flop (STCEPFF) circuit

4. Low Power analysis

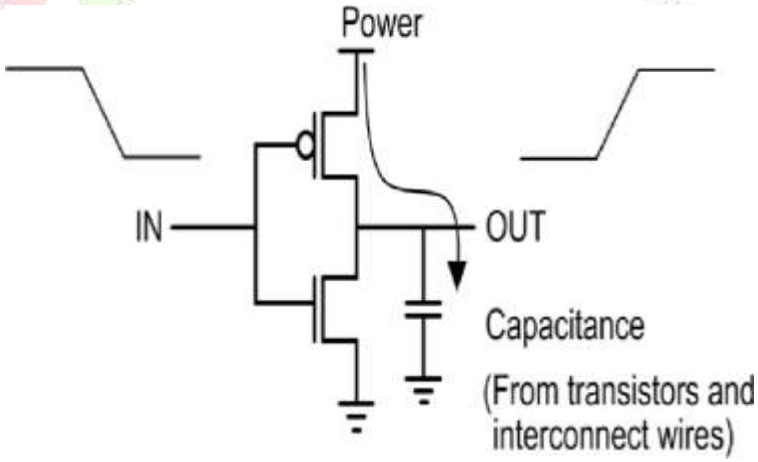

Figure 4: Dynamic Power.

Dynamic power is the power consumed when the material is in active mode. Whenever the device is in active mode the power dissipated in the device is called as Static power, but the signal values are unchanged.

$$P_{Dynamic} = (0.5)\alpha * c_L * v_{dd}^2 * f \quad (1)$$

Where α is a switching activity factor, c_L is a load capacitance, V_{dd} is a voltage (drain to drain), f is a frequency.

IV. SIMULATION RESULTS

In Figure 5 Conventional 4T NAND gate PMOS and NMOS transistors schematic diagram consist of width are 800nm and 400nm respectively, Load capacitance is 10fF at supply voltage 1.8V, pulse width 2nsec and period 1nsec at input A , pulse width 4nsec and period 2nsec at input B. Both Rise time and fall time 100fsec using cadence 180nm technology.

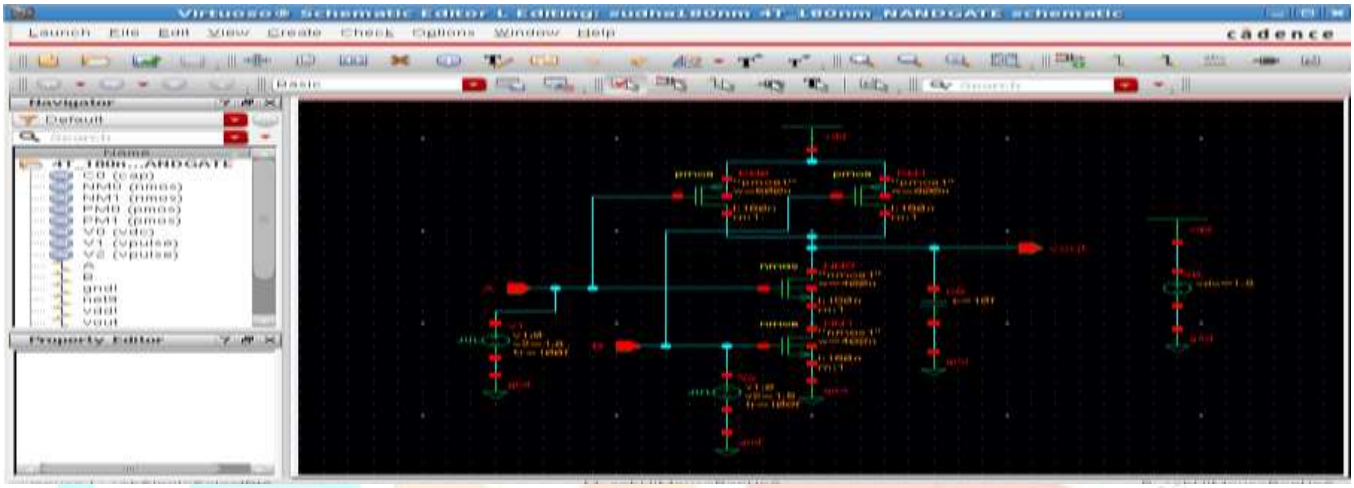

Figure 5: Conventional 4T NAND gate schematic diagram

Table 1 :Specification of 4T & 3T NAND gate in 180nm Technology

Specification	PMOS (nm)	NMOS (nm)
Library name	gpdk180	gpdk180
Length	180	180
Total width	800	400
Finger width	800	400
Source to Drain metal width	400	400
Temperature	27^0 c	
Load Capacitance	10 fF	

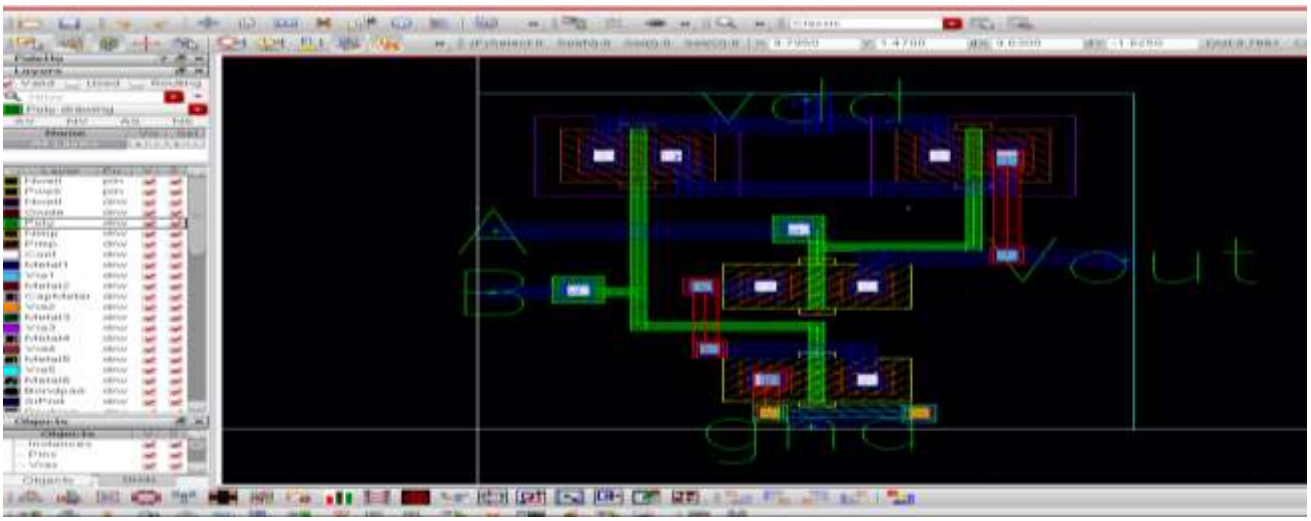

Figure 6: Conventional 4T NAND gate Layout diagram

In Figure 6 Conventional 4T NAND gate Layout diagram is combination of PMOS and NMOS transistors Layout diagram consist of width are 800nm and 400nm respectively, Green color is poly silicon and blue color is Metal1, where V_{dd} , A, B, Vout and ground are connected to Metal1, 4T NAND gate Layout diagram in 180nm Technology.

Figure 7: Conventional 4TNAND gate output waveform at the frequency 100MHz

Shown in Figure 7, 4TNAND gate output waveform red color is output signal, green color is input signal A and blue color is input signal B at the frequency of 100MHz in 180nm technology.

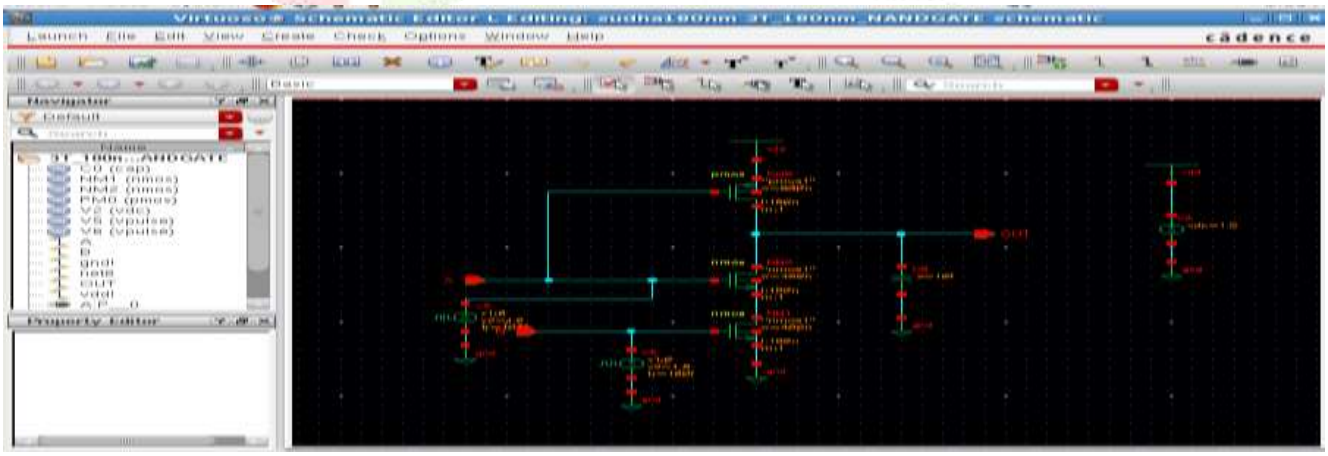

Figure 8: Proposed 3T NAND gate schematic diagram

In Figure 8 Propossed 3T NAND gate PMOS and NMOS transistors schematic diagram consist of width are 800nm and 400nm respectively, Load capacitance is 10fF at supply voltage 1.8V, pulse width 2nsec and period 1nsec at input A, pulse width 4nsec and period 2nsec at input B. Both Rise time and fall time 100fsec using Cadence 180nm technology.

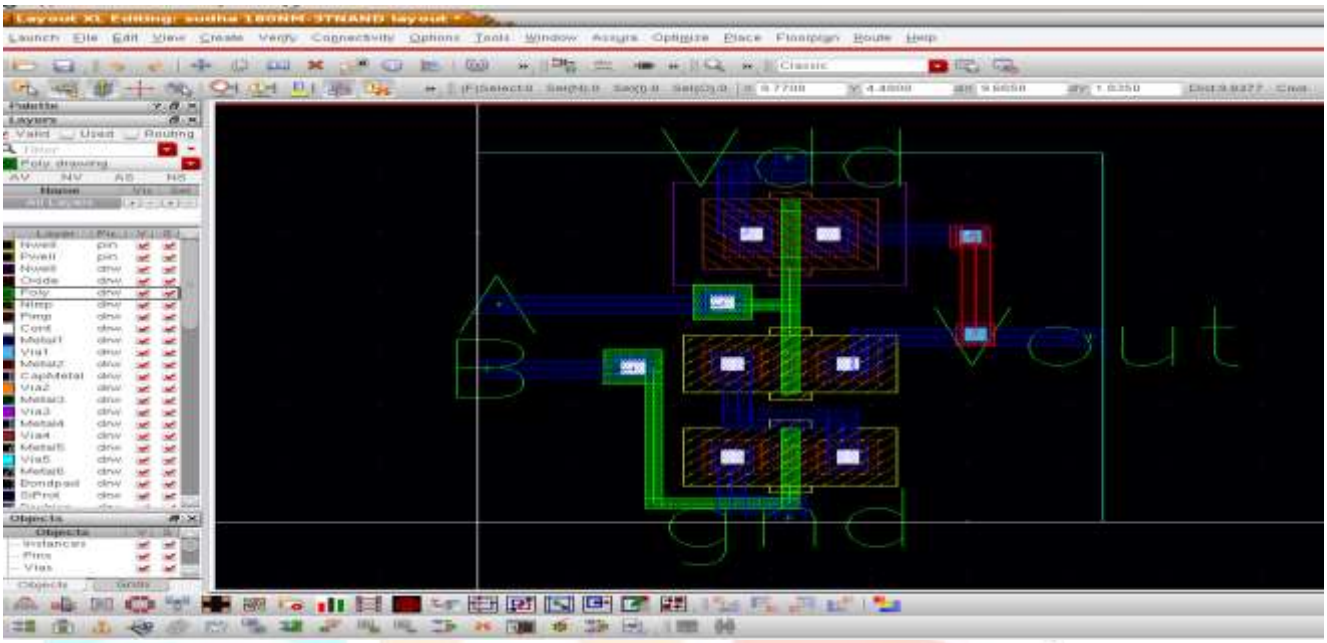

Figure 9: Proposed 3T NAND gate Layout diagram

In Figure 9 Proposed 3T NAND gate Layout diagram is combination of PMOS and NMOS transistors Layout diagram consist of width are 800nm and 400nm respectively, Green color is poly silicon and blue color is Metal1, where V_{dd} , A, B, Vout and ground are connected to Metal1, 3T NAND gate Layout diagram in 180nm Technology.

Figure 10 : Proposed 3TNAND gate output waveform at the frequency 100MHz

Shown in Figure 10, Proposed 3TNAND gate output waveform red color is output signal, green color is input signal A and pink color is input signal B at the frequency of 100MHz in 180nm technology.

Table 2 :Specification of 4T & 3T NOR gate in 180nm Technology

Specification	PMOS (nm)	NMOS (nm)
Library name	gpdk180	gpdk180
Length	180	180

Total width	800	400
Finger width	800	400
Source to Drain metal width	400	400
Temperature	27^0 c	
Load Capacitance	10 fF	

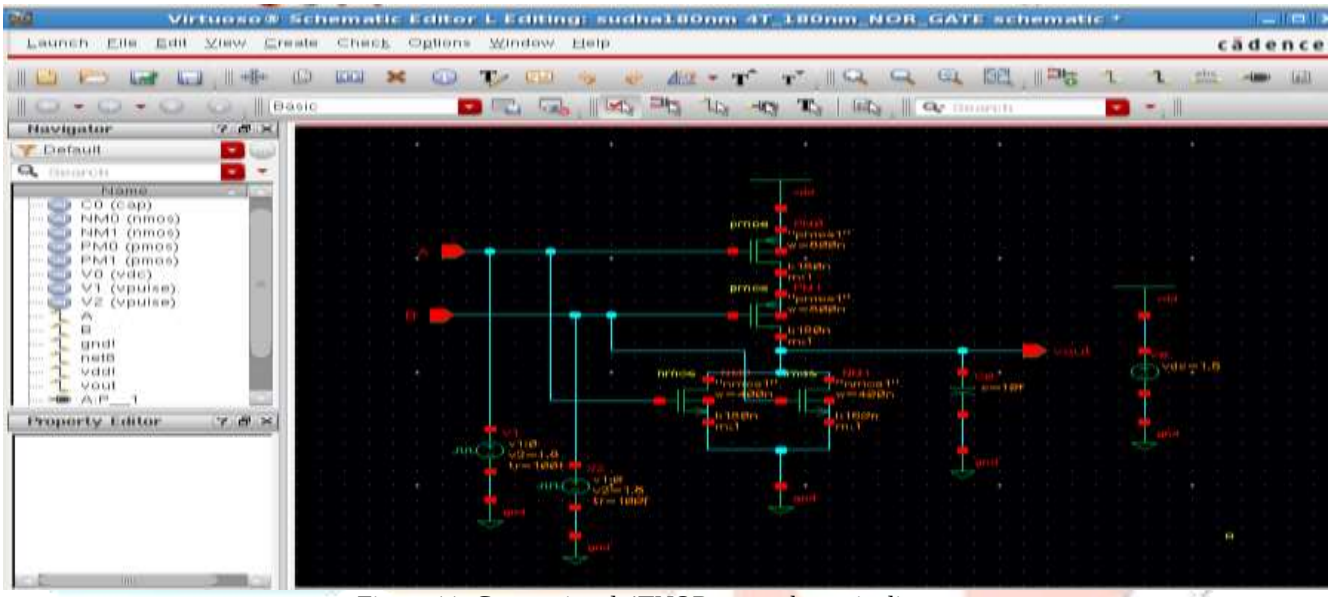

Figure 11: Conventional 4TNOR gate schematic diagram

In Figure 11, Conventional 4T NOR gate PMOS and NMOS transistors schematic diagram consist of width are 800nm and 400nm respectively, Load capacitance is 10fF at supply voltage 1.8V, pulse width 2nsec and period 1nsec at input A, pulse width 4nsec and period 2nsec at input B. Both Rise time and fall time 100fsec using cadence 180nm technology.

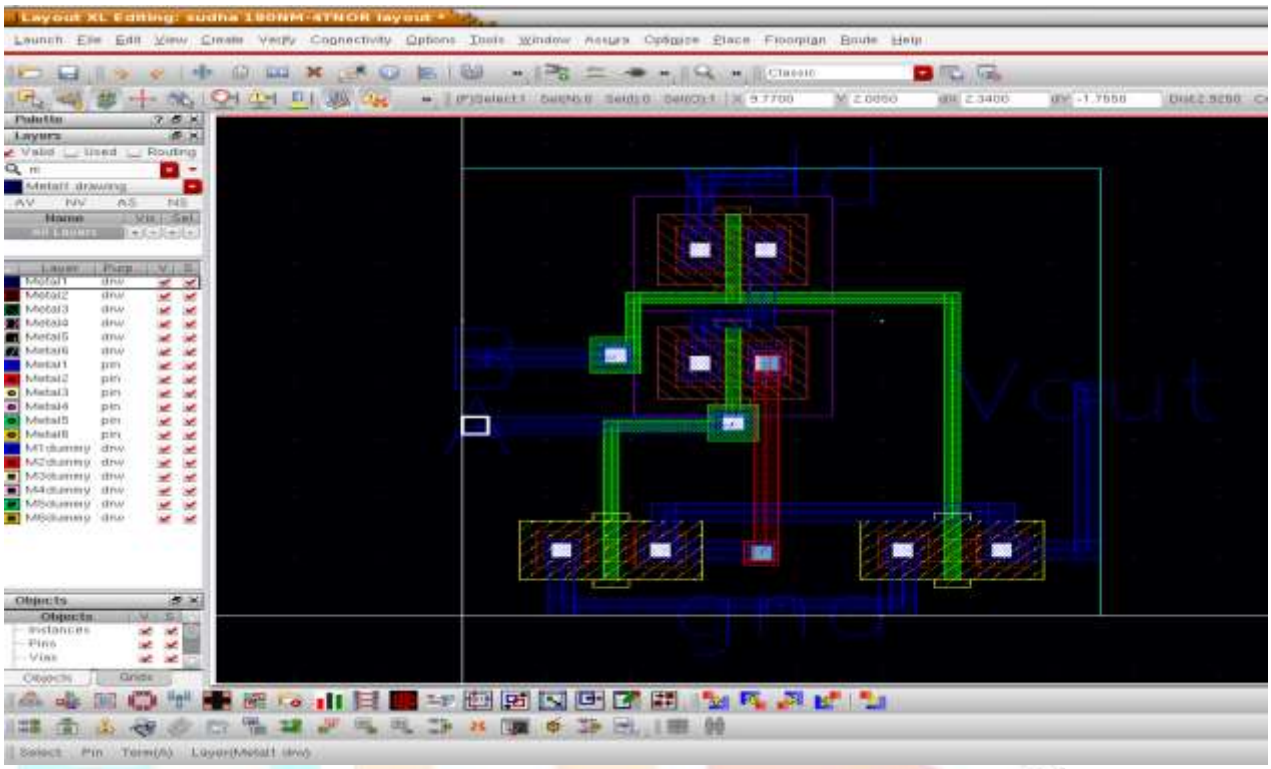

Figure 12: Conventional 4T NOR gate Layout diagram

In Figure 12 Conventional 4T NOR gate Layout diagram is combination of PMOS and NMOS transistors Layout diagram consist of width are 800nm and 400nm respectively, Green color is poly silicon and blue color is Metal1,where V_{dd} , A, B, Vout and ground are connected to Metal1, 4T NOR gate Layout diagram in 180nm Technology.

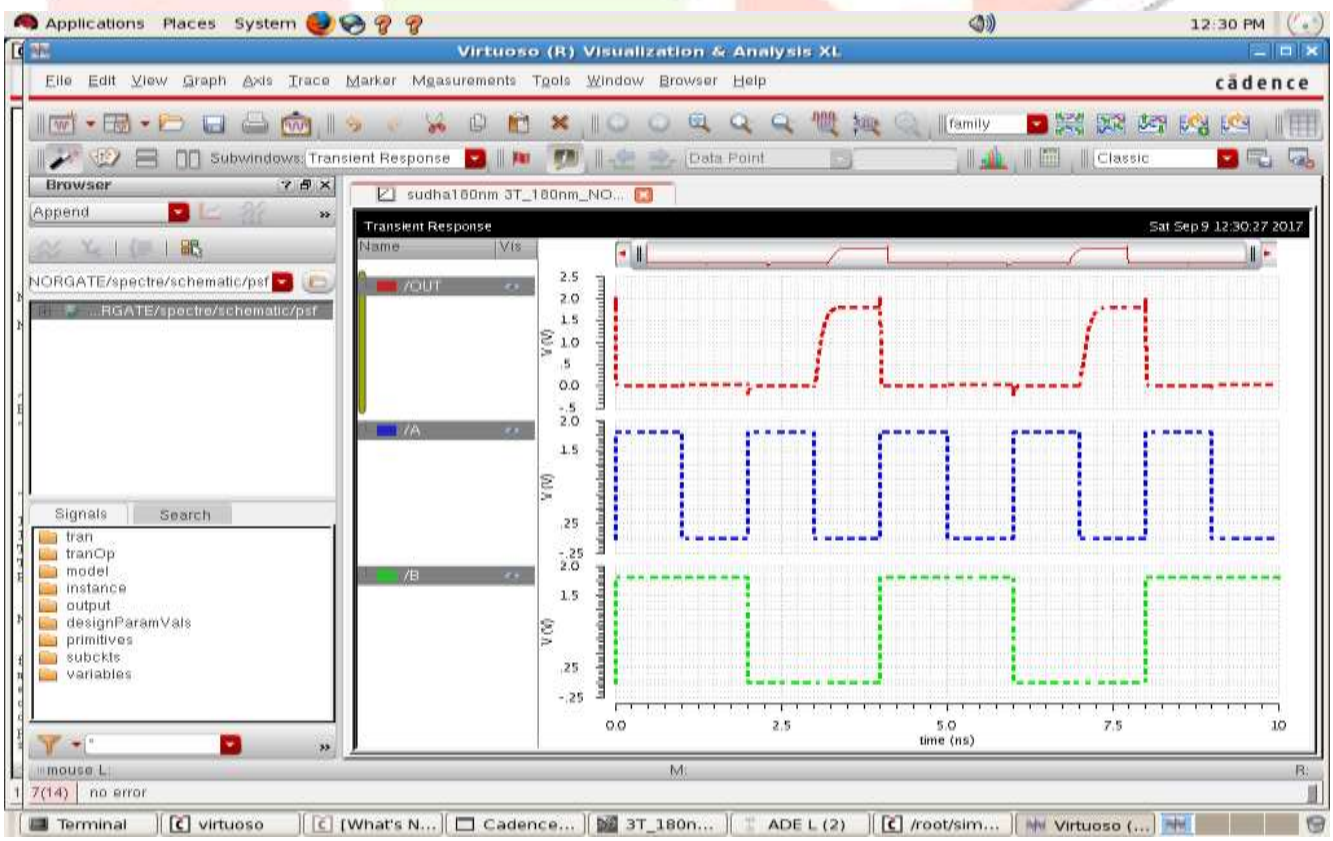

Figure 13: Conventional 4TNOR gate output waveform at the frequency 100MHz

As Shown in Figure 13, Conventional 4TNOR gate output waveform red color is output signal, blue color is input signal A and green color is input signal B at the frequency of 100MHz in 180nm technology.

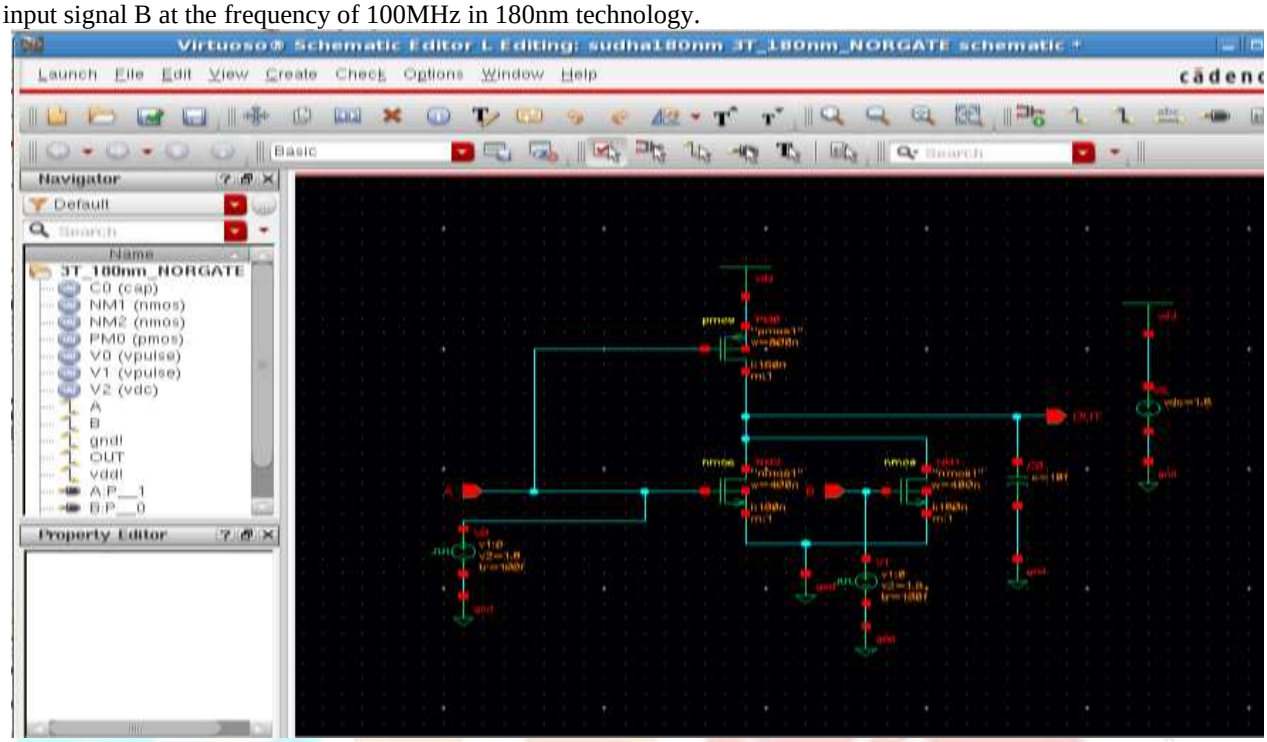

Figure 14: Proposed 3TNOR gate schematic diagram in 180nm technology

In Figure 14 Proposed 3T NOR gate PMOS and NMOS transistors schematic diagram consist of width are 800nm and 400nm respectively, Load capacitance is 10fF at supply voltage 1.8V, pulse width 2nsec and period 1nsec at input A, pulse width 4nsec and period 2nsec at input B. Both Rise time and fall time 100fsec using cadence 180nm technology.

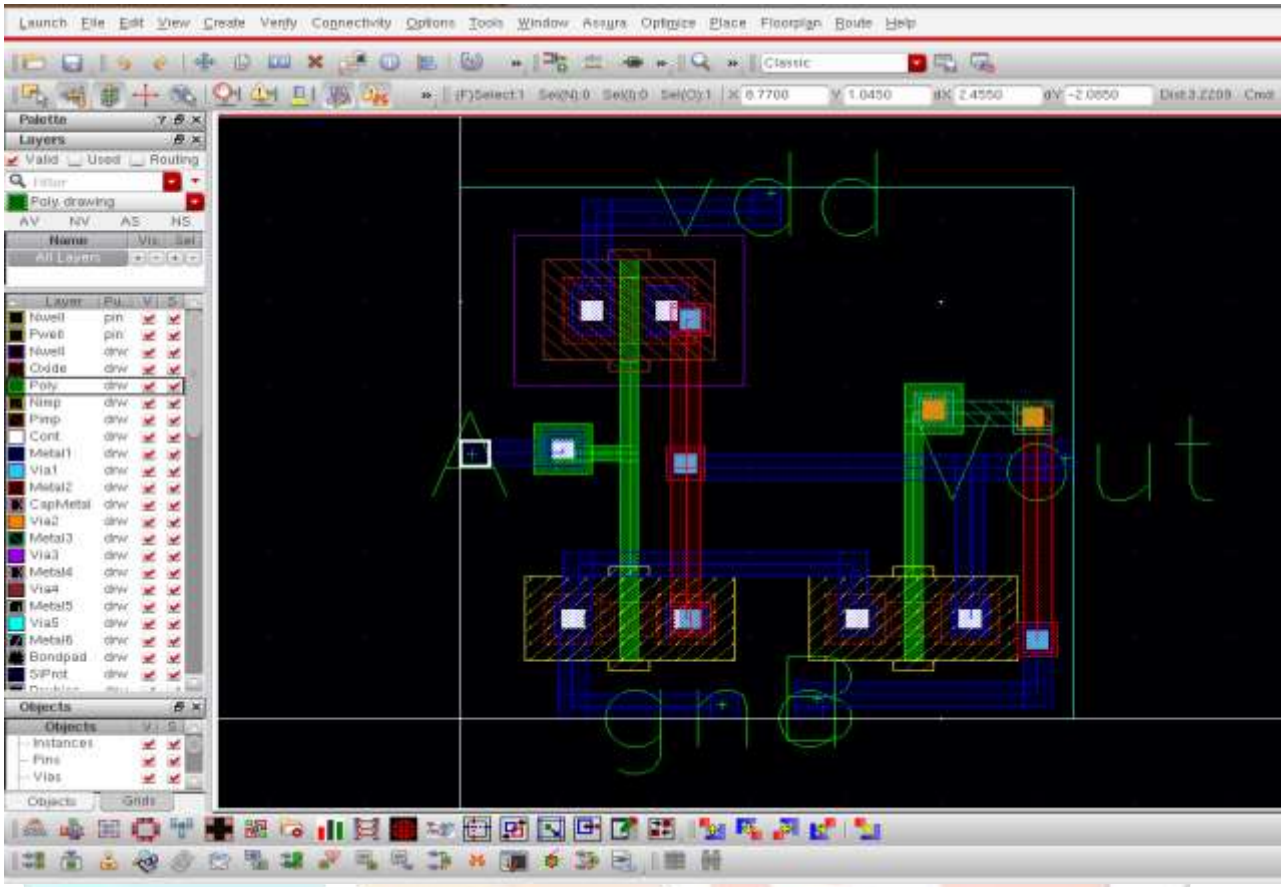

Figure 15: Proposed 3TNOR gate Layout diagram in 180nm technology

In figure 15 Proposed 3T NOR gate Layout diagram is combination of PMOS and NMOS transistors Layout diagram consist of width are 800nm and 400nm respectively, Green color is poly silicon and blue color is Metal1,where V_{dd} , A, B, Vout and ground are connected to Metal1, 3T NOR gate Layout diagram in 180nm Technology.

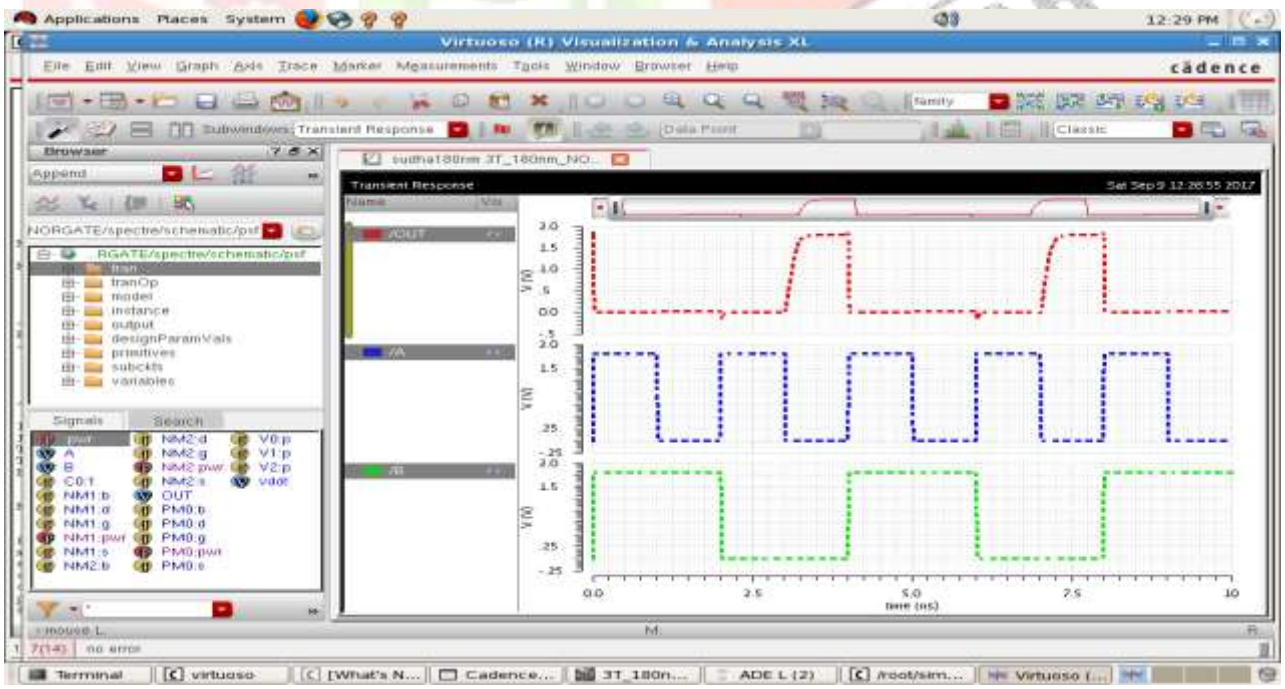

Figure 16: Proposed 3TNOR gate output waveform at the frequency 100MHz

Shown in Figure 16 Proposed 3TNOR gate output waveform red color is output signal, blue color is input signal A and green color is input signal B at the frequency of 100MHz in 180nm technology.

Table 3: Comparison of Power and Delay 4T,3T NAND and 4T,3T NOR gate

S No	NAND gate			NOR gate		
Parameter	Conventional of 4T NAND gate [1]	Proposed of 3T NAND gate	% of power , delay and PDP reduced	Conventional 4T NOR gate [1]	Proposed of 3T NOR gate	% of power , delay and PDP reduced
Transistor Count	4T	3T	-	4T	3T	-
Delay (pS)	79.13	66.19	16.35%	29.36	24.96	14.98%
Power (µW)	16.5	14.59	11.57%	179.7	112.8	37.22%
PDP(fJ)	1.3056	0.9657	26.03%	5.2759	2.8154	46.63%

It is observed that in the Table 3. The proposed 3T NAND and 3T NOR gate gives the better performance measures in terms of reduced dynamic power, area and high speed than 4T NAND and 4T NOR gate respectively.

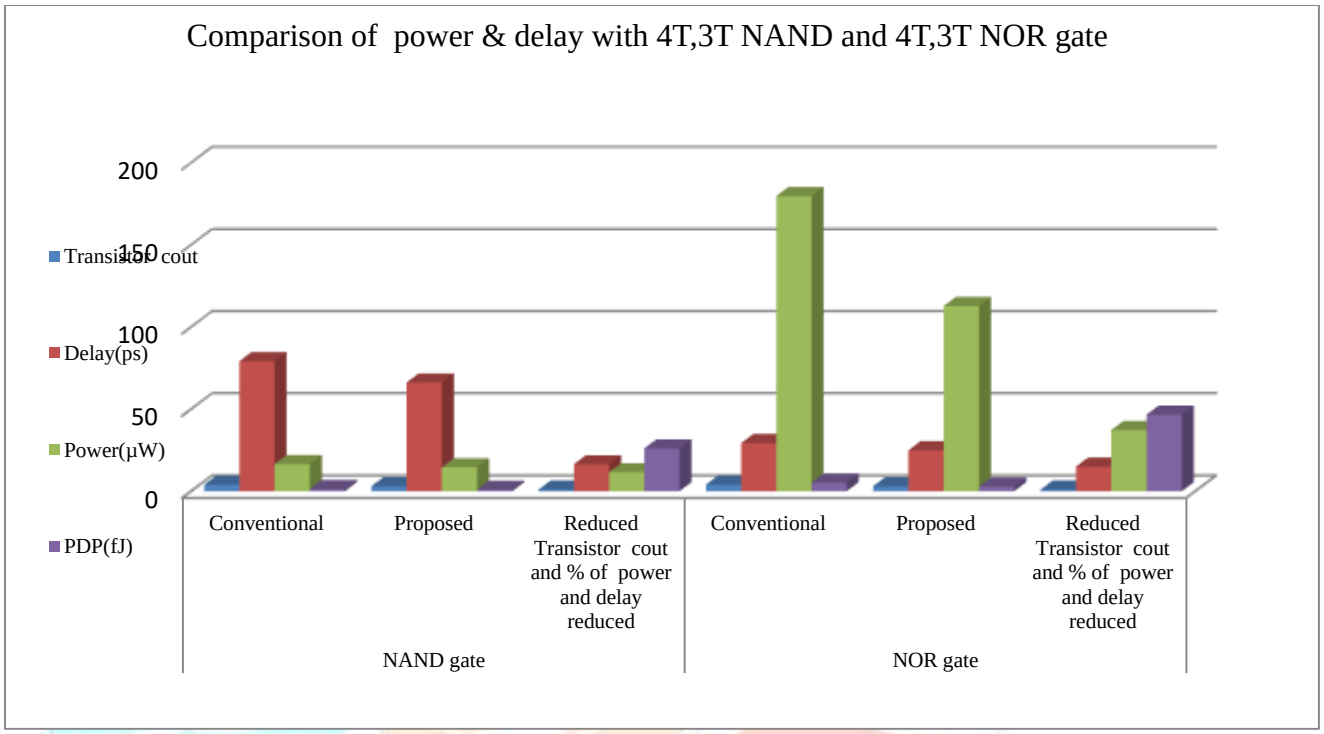

Figure 17: Comparison of power & delay with 4T, 3T NAND and 4T,3T NOR gate

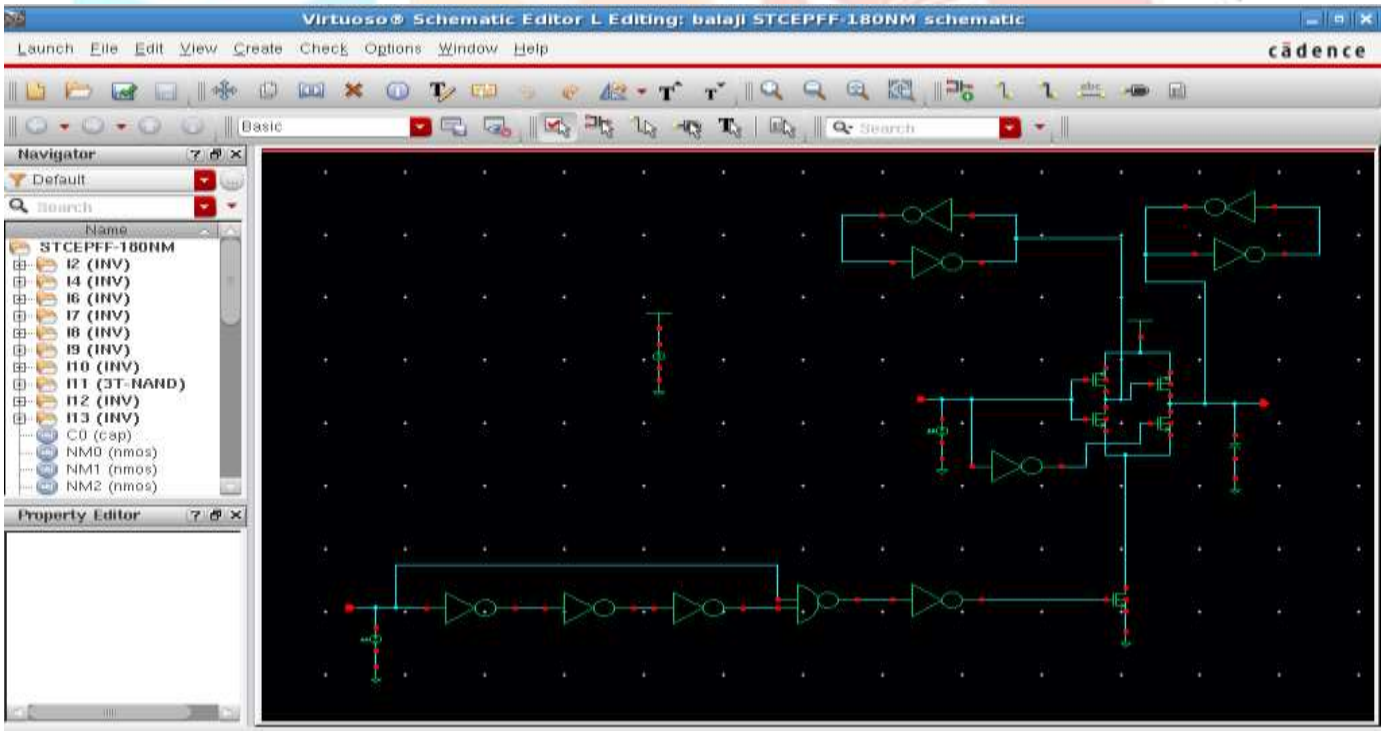

Figure 18 Single Transistor Clocked Explicit Pulse Triggered Flip flop using proposed 3T NAND gate

The schematic of STCEPFF is shown in Figure 18. In this circuit, the output of the first stage drives only one transistor P2. This reduces the capacitance load on the internal node X, which in turn reduces the 0-1 propagation delay. Also, the NMOS transistor N2 of the second stage is driven by a CMOS inverter that produces the complement of data input d.

Furthermore, the clock pulse is made to drive only a single transistor N3 unlike three transistors in EPFF. Hence STCEPFF consists of two cascaded static latches sharing one clocked transistor. The internal node X is asserted or disserted according to the input data d

during the transparent interval. The internal nodes switch only when the input changes. At the rising edge of the clock, N3 turns ON for a short time interval, which is the transparency period, and the circuit acts like two cascaded inverters allowing the input data to propagate to the output. After the transparency period, N3 switches off preventing the propagation of the input to the output. The output state is maintained by the keeper.

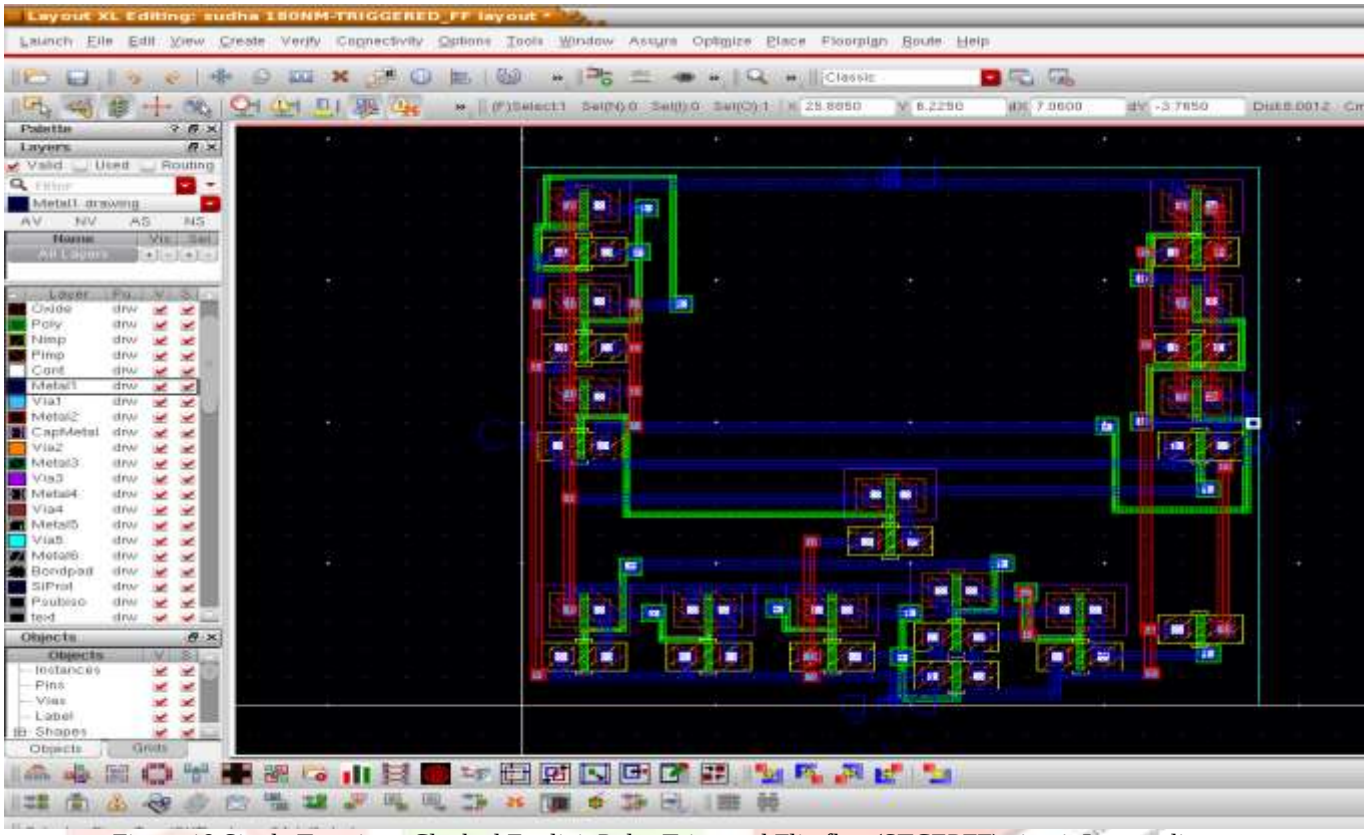

Figure 19 Single Transistor Clocked Explicit Pulse Triggered Flip flop (STCEPFF) circuit Layout diagram

As shown in Figure 19 STCEPFF Layout diagram is combination of PMOS and NMOS transistors consist of width are 800nm and 400nm ,Green color is poly silicon and blue color is Metal1, where clock, V_{dd}, Output and ground are connected to Metal1, Single Transistor Clocked Explicit Pulse Triggered Flip flop (STCEPFF) circuit Layout diagram in 180nm Technology at 1.8 Volts.

Figure 20: Output Waveform of Single Transistor Clocked Explicit Pulse Triggered Flip flop (STCEPFF) circuit using 3T NAND gate output waveform at frequency 100MHz.

The PMOS and NMOS transistors schematic diagram consist of width are 800nm and 400nm, Load capacitance is 10fF at supply voltage 1.8 V. Both Rise time and fall time (100f) sec using Cadence 180nm technology.

Table 4 Comparison of power and delay for proposed 3T NAND Gate & STCEPFF

S.No	Dynamic power(µW)	Delay(nS)
(STCEPFF) circuit	359.1	1.926

It is observed from the Table 4, Comparison of proposed Single Transistor Clocked Explicit Pulse Triggered Flip flop (STCEPFF) circuit used 3T NAND gate dynamic power is 359.1 µW and delay is 1.926 nS in 180nm technology.

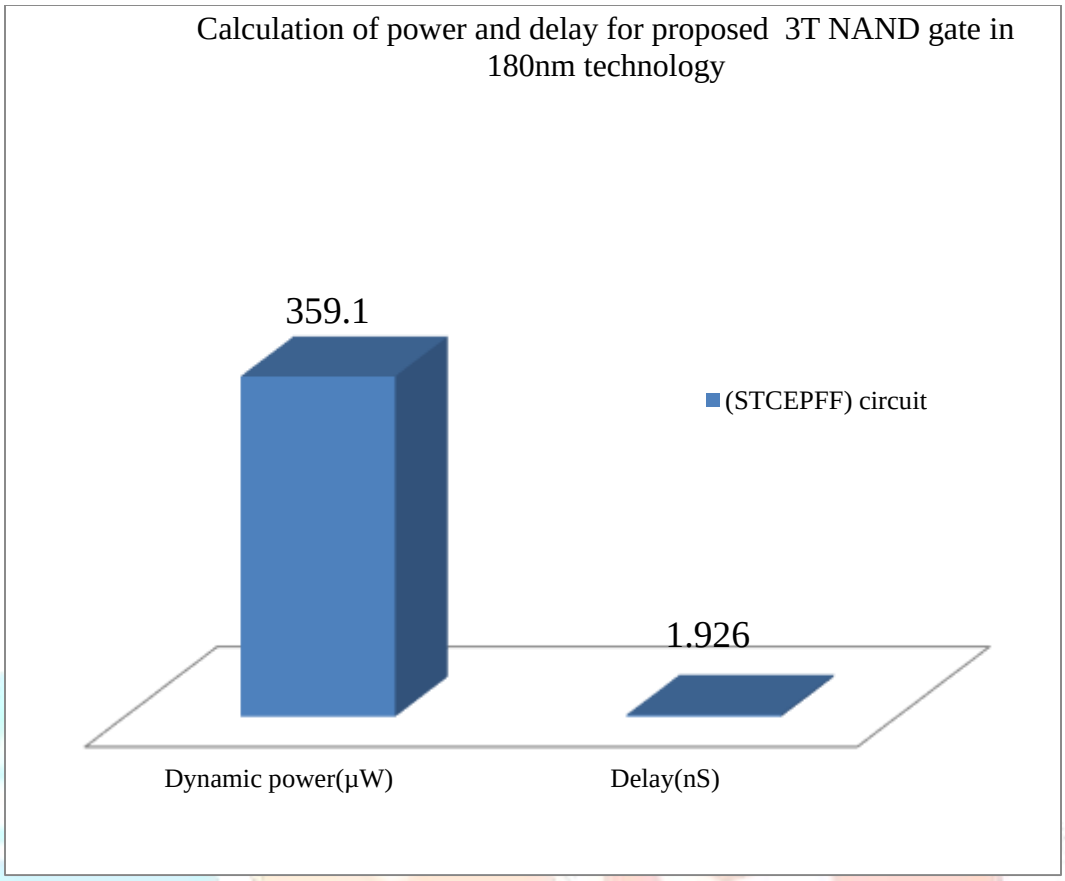

Figure 21: Calculation of power and delay for proposed 3T NAND gate in 180nm technology.

V. CONCLUSION

The proposed 3T NAND and 3T NOR gate gives the better performance measures in terms of reduced dynamic power, area and high speed than 4T NAND and 4T NOR gate respectively. Finally, a Single Transistor Clocked Explicit Pulse Triggered Flip Flop (STCEPFF) circuit is implemented with the proposed 3T NAND gate

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