Ripple Eliminator Control for AC-DC Power Converter Performance Improvement

Ms. Mamatha R V Ms. Sangeetha G R
Ms. Yashaswini G M Ms. Vennala N
BE Students, Dept. of EEE, Sai Vidya Institute of Technology, Bangalore

Prof. Shilpa Patil
Assistant Prof Department of EEE, SVIT, Bangalore, Karnataka

ABSTARCT

Abstract— The concept of ripple eliminators proposed in this paper to reduce ripple in DC systems. The power quality problem is formulated as a control problem to actively divert the ripple current on the dc bus. The main focus of this paper is to reduce the ripple in AC DC power converts. An advanced controller is proposed for one possible implementation of ripple eliminators is carried out on this paper. Entire strategy is implemented on Matlab/Simulink results are presented to verify the effectiveness of the strategy with comparison to with and without ripple eliminator for AC DC power converter.

In this paper, a single-phase Pulse width modulation-controlled rectifier is taken as an example to investigate how active control strategies can improve the power quality of dc systems, reducevoltage ripples, and, at the same time, reduce the usage of electrolytic capacitors.

Keywords— ripple currents diversion, Ripple eliminators, voltage ripples, Hysteresis control, flexibility and capacitive banks

1.INTRODUCTION

The current ripples must be maintained less than 10% of the rated current for batteries. In general, bulky capacitors or ultra-capacitors are often connected to reduce the ripple current and smooth the external voltage on batteries and fuel cells. Large electrolytic capacitors are also often needed to level and smooth the DC-bus voltage of inverters and rectifiers.

However, Rectifiers and Inverter in many applications like hybrid electrical vehicles and wind power systems,commonly used and DC voltages are not ideal but have a significant amount of harmonic components.

Because of the harmonic components in the voltages and the resulting ripple currents, ripple power has become a major power quality issue in DC system. The ripple voltages for systems powered by photovoltaic panels, batteries and fuel cells, large ripple currents and ripple voltages could considerably reduce the lifetime and long-term reliability of photovoltaic panels, batteries and fuel cells.

External voltage with larger ripples caused during the charging mode of a battery, could lead to an immoderate chemical reaction. Proliferated renewable energy systems greatly promote the development of DC distributed power system, which enjoys flexible system configurations, high efficiency, and high-density power delivery capability. In such DC systems, ripple power is often not a major concern because a DC current is constant and there is not an issue of phase differences between voltages and currents. During the discharging mode, ripple currents drawn from a fuel cell can degrade the system efficiency significantly and even make it unstable [9]. For volume critical and/or weight-critical applications, such as electrical vehicles and aircraft power systems, the volume and weight of electrolytic capacitors could be a serious problem.

Because of limited lifetime of electrolytic capacitors,they are one of the most vulnerable components in power electronic systems.

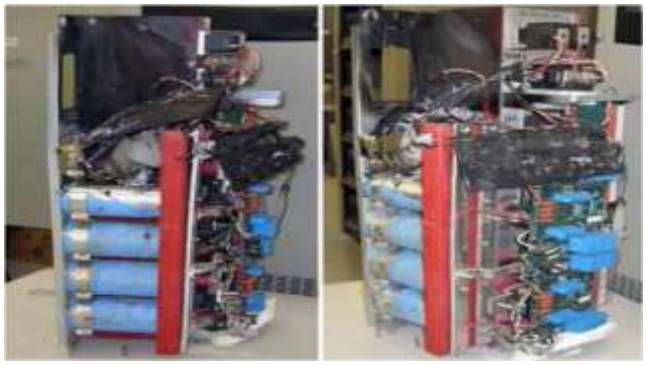

FIGURE 1.UPS inverter damaged caused by degradation of electrolytic capacitors.

As a result, in order to enhance the reliability of power electronic systems, it is highly desirable to minimize the usage of electrolytic capacitors. It is very attractive if highly-reliable small capacitors like film capacitors could be used to achieve low-level voltage ripples. According to more than half of faults of static converters are caused by degraded electrolytic capacitors. On the other hand, the presence of large voltage ripples is an essential factor that accelerates the degradation of electrolytic capacitors. Figure 1 shows a damaged UPS inverter assembly, the damage was caused by the ageing electrolytic capacitors. This may cause a big disruption in critical loads, which in turn could lead to a huge cost. However, in applications involving bulky electrolytic capacitors, it is often inevitable to have a tradeoff between minimizing the total capacitance required and suppressing voltage ripples. Another design degree of freedom, normally through active control, needs to be introduced to break this deadlock.

In principle, this power quality issue in DC systems stems from energy fluctuation, which can come from sources and/or loads of systems. Four main approaches have been developed in the literature to reduce or compensate energy fluctuation so that the voltage ripples can be reduced and the power quality in DC systems can be improved.

One approach is to inject harmonic currents to suppress the fluctuations of the input energy by changing the control strategy for the existing power switches in the system. The analysis in these papers is based on the fact that decreased pulsating input power leads to decreased ripple power and capacitor volume on the DC bus, which can be achieved by controlling the input current. it was proposed to inject third harmonic component to the input current so as to reduce the DC-bus capacitor in LED drivers. In, a similar concept was also adopted by distorting the input current to reduce the output capacitor. This approach benefits with no added power components but the disadvantage of this approach is the increased total harmonic distortion (THD) of the input current. The essence of injecting harmonic currents or distorting the input current is to obtain a varied duty cycle to control the power switches, which changes the amount of energy delivered to the load in each fundamental cycle.

The second approach is to use buck/boost DC/DC converters to construct two DC voltages across two capacitors that are connected in opposite polarity. The sum of pulsating energy stored in the two capacitors are nearly equal to the system pulsating energy and hence, the pulsated energy does not appear on the DC bus. Both the DC-bus voltage ripples and the required DC-bus capacitance can be reduced.

The third approach is to add an active energy storage circuit in parallel with the DC-bus capacitor to bypass the ripple currents originally flowing through the DC-bus capacitor. The strategy proposed in is such an example, with a circuit consisting of one capacitor, one inductor and two power switches. It absorbs and releases the ripple energy, respectively, during its two different half cycles. Due to the particular operating modes adopted, the current is compensated in terms of averaged values, instead of instantaneous values, so the remaining voltage ripples are still large although considerably reduced

The fourth approach is based on connecting an active compensator in series with the DC bus line. The compensator basically behaves as a voltage source to offset the voltage ripples. Note that only the DC voltage after the compensator becomes clean without noticeable low-frequency ripples but the DC voltage before the compensator still suffers from large low-frequency ripples. Due to the series connection, lines between the DC sources and loads should be cut off so that the compensator can be connected. However, for some DC systems, this can be a problem because of the widely-distributed sources and/or loads. Due to the series operation, the voltage stress of the added compensator is reduced. However, the current stress of the compensator is increased because the ripple power for a certain load is fixed.

. The main focus of this paper is to investigate how advanced control strategies could improve the

performance of shunt ripple eliminators for DC systems, rather than optimizing the system performance through topological design. It is foundthat the capability of diverting the ripple current away from the DC bus is the key for improving the performance. The boost topology in [25], where a flicker-free AC-DC LED driver with a flyback PFC converter was designed and the strategy, is takenas an example, because of its high efficiency compared to buck-type topologies, to demonstrate the performance improvement by designing a suitable controller. The following parts of this paper are presented as follows.In Section II, a single-phase H-bridge Pulse width modulation (PWM) rectifier is taken as an example to analyse the ripple energy and ripple voltage in a DC system. In Section III, the concept of ripple eliminators is further developed and the level of reduction of capacitance is quantied. In Section IV, the operation principle of the ripple eliminator under investigation is discussed and in Section V the controller of the ripple eliminator is developed based on repetitive control. Experimental results with comparison to a ripple eliminator reported in the literature are provided in Section VI. At the end, conclusions are made in Section VII.

II. ANALYSIS OF RIPPLE ENERGY AND RIPPLE VOLTAGE

In order to facilitate the analysis in this paper, a single-phase H-bridge PWM-controlled rectifier as shown in Figure 2 is used as an example, with all the components assumed to be ideal to simplify the analysis in the sequel. Most of the findings can be easily applied to other applications.

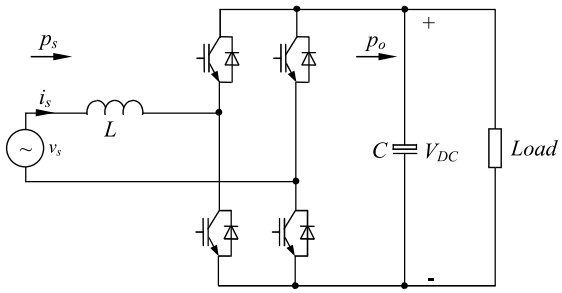

FIGURE 2. Single-phase H-bridge PWM-controlled rectifier

If the input current of the rectifier is regulated to be sinusoidal as *is*= ^ 2*Is* sin(w*t*) and in phase with the input voltage *vs* 2*Vs* sin(w*t*), then the input power is

$$p_s = v_s i_s = V_s I_s - V_s I_s \cos(2\omega t), \quad \text{- (1)}$$

where *Vs* and *Is* are the RMS values of the input voltage and current, respectively, and w is the angular line frequency. Note that the power drawn from the AC source consists of a constant *VsIs*and a second-order ripple com *VsIs*cos(2w*t*).

InordertoanalyzethevoltageripplesoftheDCbus,thenet changeoftheenergystoredintheDC-buscapacitorover achargingperiod(i.e.aquartercycleofthesupply),called the ripple energy, can be calculated as [10]

$E_r =$ vs Is/$_\omega$. (2)

As demonstrated in [10], the voltage ripple (peak-peak) on the capacitor *C* can be given as

$$\Delta V_{DC} \approx \frac{E_r}{C\ VDC0} \quad (3)$$

where *VDC*0 is the average value of the voltage *VDC*. It is clear that, when increasing the capacitor *C*, the DC-bus voltage ripple is decreased but this increases the weight, volume and cost of the system and decreases the reliability of the system, which should be avoided if possible.

III. RIPPLE ELIMINATORS AND THE LEVEL OF CAPACITANCE REDUCTION

In order to break the deadlock between minimizing the required capacitors and reducing voltage ripples, another design degree of freedom, called the ripple eliminator [19], can be introduced to replace the bulky DC-bus capacitor, as shown in Figure 3. The basic idea is to introduce an auxiliary capacitor *Ca* in the ripple eliminator so that the ripples on the DC bus can be transferred onto *Ca*. The voltage *Va*across the auxiliary capacitor *Ca* is allowed to vary within a wide range with a large ripple 4*Va*. This concept can be regarded as the general form of the strategies proposed in the literature Since the ripple eliminator is operated to divert the ripple energy on the DC bus to the auxiliary capacitor, there is no need to use a large electrolytic capacitor on the DC bus and

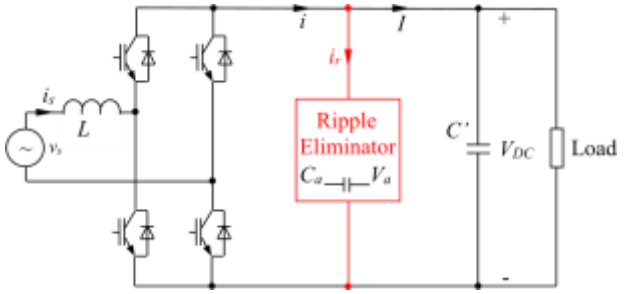

FIGURE3. The concept ofrippleeliminators

the ripple energy on the auxiliary capacitor should be the same as the DC-bus ripple energy in the ideal case. Applying (3) to the auxiliary capacitor, there is

$$C_a \approx \frac{E_r}{\Delta V_a V_{a0}} \quad (4)$$

where 4*Va* and *Va*0 are the peak-peak and average voltages of the auxiliary capacitor. Note that the ripple energy *Er* is determined by the DC bus and not affected by the added ripple eliminator. Note also that the auxiliary capacitor is designed
to allow large voltage ripples. Assume the ripple voltage ratio of the auxiliary capacitor Is to allow large voltage ripples. Assume the ripple voltage ratio of the auxiliary capacitor is

$$r_a \quad \frac{V_a}{\Delta \ V_{a0}} \quad (5)$$

Then (4) can be re-written as

$$C_a \approx \frac{E_r}{rV^2} \quad (6)$$

It is clear that for the same ripple ratio r_a, the capacitance is in inverse proportion to the square of the voltage across it, which means the auxiliary capacitance can be significantly reduced via increasing its operating voltage

If the same ripple energy E_r needs to be taken care of by a DC- bus capacitor C, as shown in Figure2,

then, according to (3), the voltage ripple ratio *r*of the DCbus is about

$$r \approx \frac{E_r}{CV^2}. \quad (7)$$

This means the auxiliary capacitor needed can be

$$C^a \approx \frac{r}{r_a}\left(\frac{V_{DC0}}{V_{a0}}\right)^2 C \quad (8)$$

$$R_d = \frac{r}{r}\left(\frac{V_{a0}}{V_{DC0}}\right)^2 = \frac{1}{1}\frac{V_a V_{a0}}{V_{DC} V_{DC0}} \quad (9)$$

The capacitance $C_a$can be reduced by1)allowing the voltage ripple ratio higher than that of the original DC bus, 2) adopt- in an operating voltage V_{a0} higher than V_{DC0} for C_a.The topology in adopts a higher voltage ripple ratio and the strategy in adopts both.

Here is a numerical example. If then auxiliar y capacitor voltage is chosen four times of the DC-bus voltage then the maximum allowable ripple voltage ratio of the auxiliary capacitor is *ra* =75%. Moreover, if the allowed ripple ratioof the original DC-bus voltage is *r* =5%, then the auxiliarycapacitor can be reduced by a factor of *Rd* = 240.Hence, it is not a problem to reduce the level of the totalcapacitance required by a factor of 100.

Note that is independent of applications. It sets thebasic guidelines for designing different ripple eliminators.Some other guidelines include:

1) a ripple eliminator needsto be able to provide bi-directional current path so that current can low through;

2) the remaining level of DC-bus voltage ripples is determined by the performance of the ripple eliminator so the ripple eliminator needs to be controlled properly;

3) The hold-up time requirement, voltage stress and current stress should be considered to choose suitable capacitors. If the maximum voltage of the capacitor is determined, then increased capacitance means longer hold-up time and lower current stress, which are preferred in some applications . As a result, there are several trade-offs that should be considered together when choosing the capacitors for certain applications. If all the ripple current in *i*is bypassed through the ripple eliminator then the DC-bus capacitor *C*0 only needs to take care of the switching ripples and hence small capacitors can be used.

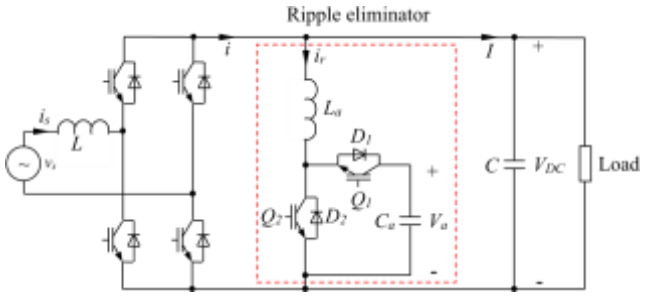

FIGURE 4. The ripple eliminator under investigation.

IV. THE RIPPLE ELIMINATOR UNDER INVESTIGATION

A. *OPERATION PRINCIPLES OF THE RIPPLE ELIMINATOR*

This topology was studied in], where a flicker free LED driver with a flyback PFC converter was designed and the strategy about how to remove the ripple energy through tracking the ripple current generated by the flyback converter was analysed in detail, and in and where an active filter for grid-tied PV applications was developed to reduce the low frequency current drawn from PV panels.It can also be regarded as one phase of an inverter with the DC bus provided by the auxiliary capacitor C_a so it is able to divert a bidirectional current $i_r$away from the DC bus. In this paper, a practical implementation of the ripple eliminator concept to be studied is shown in the dashed box of Figure 4, which is actually a bi-directional boost-buck converter.

In order to track the ripple current, switches Q_1 and Q_2 can be controlled in two different switching modes. One is only to control Q_2 (Q_1, resp.) in the positive (negative, resp.) half cycle of the ripple current, which corresponds to the charging (discharging) mode. In the charging mode, Q_2 is controlled by a PWM signal and Q_1 is always OFF, which provides the path for the positive half cycle of the ripple current i_r, and hence, the ripple eliminator is operated as a boost converter. In the discharging mode, Q_2 is always OFF and Q_1 is controlled by a PWM signal, which provides the path for the negative half cycle of the ripple current i_r, and the circuit is operated as a buck converter. Therefore, the direction of the current flowing through the auxiliary inductor can only be negative or positive in one switching period.

Another switching mode is to control the two switches complementarily. That means switches Q_1 and Q_2 are controlled by two inverse PWM signals to track the ripple current and the voltage across the auxiliary inductor can be V_{DC} and $V_{DC} - V_a$ depending on the ON-OFF combinations of these two switches. In one PWM period, if Q_1 is ON, Q_2 is controlled by an inverse signal to keep OFF and vice versa. Different from the previous operation mode, the inductor current can be positive or negative even during one switching period. This is a very good feature because the current can be tracked very well no matter at zero-crossing points or at large current ripple conditions. In the previous mode, the sharp turn at the zero-crossing points causes high harmonic content, which is hard forth e controller to track. Since the final control objective is to reduce DC-bus voltage ripples, it does not matter if the auxiliary current ripple is slightly large because of the high switching frequency. With the same system parameters, large ripple means a small inductor is needed, which can reduce the size of the ripple eliminator. In this paper, in order to fully use the ripple eliminator under different working conditions, Q_1 and Q_2 are operated complementarily to track the ripple current.

B. *SELECTION OF THE AUXILIARY INDUCTOR*

Apart from the auxiliary capacitor C_a, there is another passive component, i.e., the auxiliary inductor L_a, that affects the performance of the ripple eliminator. In this subsection, how to select the L_a is discussed.

Here, the duty cycle and the PWM period time are denoted as $d_r$and T_r, respectively. As two switches Q_1 and Q_2 are operated complementarily, the ON time of Q_2 is $d_rT_r$and the ON time of Q_1 is $(1 - d_r)T_r$in one PWM period. Since the PWM frequency is much higher than the line frequency, it can be assumed that the current increased (to withstand the positive voltage V_{DC}) and decreased (to withstand the negative voltage $V_{DC} - V_a$) in these two modes are the same in the steady state. In other words, the current ripple $4i_r$ is

$$4i_r = \frac{V_{DC}}{L_a} d_r T_r = -\frac{V_{DC} - V_a}{L_a}(1 - d_r)T_r. \quad (10)$$

Therefore, the duty cycle $d_r$can be obtained as

$$d_r = 1 - \frac{Vdc}{Va} \quad (11)$$

The substitution of (11) into (10) leads to

$$\frac{La\Delta ir}{VDC} = \left(1 - \frac{VDC}{Va}\right) \mathrm{Tr} \quad (12)$$

which can be re-written as

$$\mathrm{frLa}\Delta ir = \mathrm{VDC}\left(1 - \frac{VDC}{Va}\right) \quad (13)$$

As expected, the product of the switching frequency f_r, the inductance L_a and the current ripple $4i_r$ is a constant, which is determined by the DC-bus voltage and the auxiliary voltage. The auxiliary inductor current mainly includes the current ripple $1i_r$ and the ripple current to be injected into the DC-bus. Hence, the role of the DC-bus capacitor is to filter out this high frequency current ripple $4i_r$, which could be achieved by a small capacitor.

In this case, the amplitude of the current ripple $1i_r$ is not a major concern. As long as the low frequency component of the inductor current is equal to the second-order harmonic current on the DC bus, the ripple voltage on the DC bus can be effectively eliminated. The high frequency part of i_r, which is $1i_r$, can be large in order to reduce the inductance of L_a. However, a large $1i_r$ leads to a large current peak for the inductor and also aggravate the filtering burden of the capacitor C. Therefore, there is a trade off between L_a and $4i_r$. In this work, in order to ensure the inductor is operated in the critical continuous current mode, the amplitude of $4i_r$ is designed to satisfy

$$1i_r \leq 2I_{rm}, \quad (14)$$

where $I_{rm}$is the peak value of i_r. Considering (12), the auxiliary inductance should be selected to satisfy

$$\mathrm{La} = (1 - VDCa)VDC \quad (15)$$

On the other hand, the rising rate of the auxiliary inductor current should be greater than the maximum rising rate of the reference ripple current which appears at the zero-crossing point. If the reference ripple current is expressed as

$$i_r = I_{rm}\sin(2\omega t), \quad (16)$$

then the maximum rising rate of $i_r$can be obtained as

$$di_r$$

$$|_{t=0} = 2\omega I_{rm} = 4\pi f I_{rm}. \quad (17)$$

Accordingly, there exist

$$\frac{VDC}{La} \geq 4\pi f I_{rm}, \quad (18)$$

and

$$\frac{Va - VDC}{La} \geq 4\pi f I_{rm}. \quad (19)$$

Combining the above two equations, then

$$\dot{L}_a \leq \min \frac{V_{DC}}{4\pi f I}, \frac{V_a - V_{DC}}{4\pi f I} . \quad (20)$$

Combining it with (15), there is

$$\frac{(1 - \frac{V_{DC}}{V_a})V^{DC}}{2I_{rm}f_r} \leq L_a \leq \min \frac{V_{DC}}{4\pi f I_{rm}}, \frac{V_a - V_{DC}}{4\pi f I_{rm}}, \quad (21)$$

where *IrmfrLa*re_ects the voltage dropped on *La* caused by *Irm*at the switching frequency *fr*

V. CONTROL OF THE RIPPLE ELIMINATOR

A. FORMULATION OF THE CONTROL PROBLEM

As discussed before, the DC voltage ripple is caused by the pulsating input energy. After the ripple eliminator is introduced to divert the ripple current from the capacitor C, the DC-bus voltage then becomes ripple free, apart from switching ripples, and equal to the DC-bus voltage. Hence, the current to be diverted should b

$$i_r = -\frac{VsIs}{VDCo}\cos(2\omega t), \quad (22)$$

which is a second-order harmonic current. Note that the current $i_r$could be different for other DC systems but it does not affect the analysis above. The control objective of the ripple eliminator is then to instantaneously divert $i_r$in (23) away from the DC bus through the ripple eliminator so that the current flows through the load does not contain ripples other than switching ripples. In other words, the control problem is to instantaneously track the ripple current $i_r$that corresponds to the ripple power via controlling Q_1 and Q_2.

Tracking the $i_r$can be achieved in terms of either averaged values or instantaneous values, which corresponds to the DCM or CCM operation of the

ripple eliminator. Of course, the current tracking performance in CCM is better than that in DCM. Hence, the CCM operation is preferred. On the other hand, the inductor will have a relatively large size in order to keep the ripple current continuous. This can be mitigated if the ripple eliminator can be operated at high switching frequencies. For example, if MOSFETs instead of IGBTs are used to construct the eliminator, then the switching frequency can be very high, e.g., at 200 kHz, so that only a small inductor is needed. When it is operated in DCM, the inductor can be smaller but the maximum current flowing through the switches is much higher in DCM than that in CCM because of the average tracking. High current means high cost for switches.

In this paper, the CCM operation is chosen because of its high performance for current tracking. The ripple current tracking can be achieved in two steps: 1) to generate a reference ripple current and 2) to track the reference ripple current. Moreover, in order to make sure that the current tracking can be achieved properly, the voltage across the auxiliary capacitor C_a should be regulated as well. The proposed overall control strategy is shown in Figure 6, which is explained in detail in the following subsections.

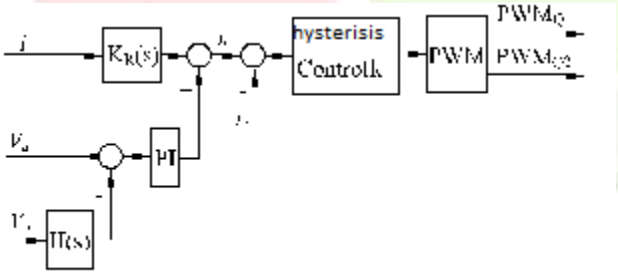

FIGURE 6. Control strategy for the ripple eliminator.

B. REGULATION OF THE AUXILIARY CAPACITOR VOLTAGE

The operation of the ripple eliminator relies on a properly regulated the voltage across the auxiliary capacitor, which is designed to allow a significant amount of ripples. For the purpose of maintaining the average DC component at a certain value, a low-pass filter can be adopted to remove ripples. Here, the following low-pass filter

$$H(s) = \frac{1-e^{-ts/2}}{Ts/2} \qquad (23)$$

In which τ is chosen as the system fundamental period ,isused to filter out other components so that the average value of the voltage can be extracted for control. Once the average voltage is obtained, it can be easily regulated at a given value $V_a^*$by using a PI controller, as shown in Figure 6, via charging or discharging the ripple eliminator. It is also possible to design the controller to regulate the maximum or minimum value of the voltage, as reported in [19].

C. GENERATION OF THE REFERENCE RIPPLE CURRENT i_r

The second-order harmonic current of the current *i*between the rectifier and the ripple eliminator can be extracted by using the following resonant filter

$$K^R(s) = \frac{Kh2\varepsilon h\omega s}{s^2+2\varepsilon h\omega s+(h\omega)^2} \qquad (24)$$

tuned at the second harmonic frequency with $\xi = 0.01$, $h = 2$, and $\omega = 2\pi f$. If the harmonic current has components at other frequencies, then $K_R(s)$ can be designed to include the corresponding term. For example, if there is a 3rd-order harmonic current, then $K_R(s)$ can include a term with $h = 3$. The extracted current can be added to the output of the PI controller that regulates the auxiliary capacitor voltage to form the reference ripple current i^*_r; see Figure 6.

D. DESIGN OF A CURRENT CONTROLLER TO TRACK THE SECOND-ORDER RIPPLE CURRENT

As explained before, the control problem is essentially a current tracking problem. Since the reference ripple current is periodic, the repetitive control strategy [29], [30] can be adopted to achieve excellent tracking performance with a fixed switching frequency, as shown in Figure 6.

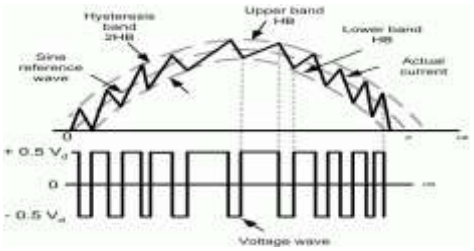

FIGURE 7. The hysteresis controller.

reference signal (if,ref or vf,ref) within a certain tolerance band. This control scheme is shown in a block diagram form in Figure 3. In this control scheme, a signal deviation (H) is designed and imposed on If ,ref or Vf,ref to form the upper and lower limits of a hysteresis band. The If or Vf is then measured and compared with If ,ref or Vf ,ref ; the resulting error is subjected to a hysteresis controller to determine the gating signals when exceeds the upper or lower limits set by (estimated reference signal + H/2) or (estimated reference signal – H/2). As long as the error is within the hysteresis band, no switching action is taken. Switching occurs whenever the error hits the hysteresis band. The APF is therefore switched in such a way that the peak-to-peak compensation current/voltage signal is limited to a specified band determined by H as illustrated by Figure 4. The advantages of using the hysteresis current controller are its excellent dynamic performance and controllability of the peak-to-peak current ripple within a specified hysteresis band.

TABLE 1. System parameters.

Parameters	Values
AC voltage (RMS)	230 V
System fundamental frequency	50 Hz
Switching frequency	10 kHz
Inductor L	2.2 mH
Inductor L_a	2.2 mH
Capacitor C	110 μF
Auxiliary capacitor C_a	165 μF
Voltage V_{DC}	400 V

VI. Simulation Result VALIDATION

In order to verify the proposed control method, a test rig that consists of a 1.1 kW single-phase PWM-controlled rectifier and three kinds of ripple eliminators was built. The system parameters are summarized in Table 1. In this study, the ripple voltage ratio is selected below 10% for all the auxiliary capacitor voltage references from 500 V to 700 V. According to (6), C_a should be around 160 μF and is chosen as C_a = 165μF. Of course, this ratio could be greater than 10% in order to further decrease the capacitance needed as long as the auxiliary capacitor voltage is higher than the DC-bus voltage to guarantee the successful operation of the eliminator.

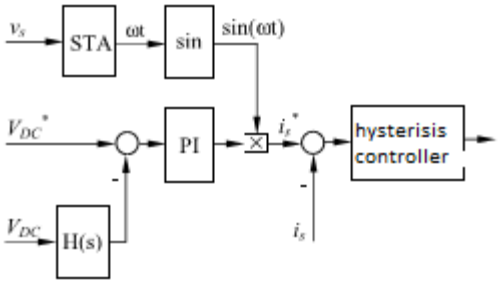

FIGURE 8. Controller for a single-phase PWM-controlled rectifier.

A. *CONTROL OF THE SINGLE-PHASE PWM-CONTROLLED RECTIFIER*

A controlledsingle phase PWM rectifier is adopted as an example for generating voltage/current ripples in a DC system. It is controlled to draw a clean sinusoidal current from the source that is in phase with the voltage source. This can be achieved with the controller shown in Figure 8, which mainly consists of three parts: 1) a synchronization unit to generate a clean sinusoidal current signal that is in phase with the source so that the reactive power drawn from the supply is controlled to be zero; 2) a PI voltage controller that maintains the voltage V_{DC} according to the DC-bus reference voltage V_{DC}*to generate the right amplitude for the current reference; and 3) a current controller to track the reference current that is formed according to the PI voltage controller and the synchronization signal.

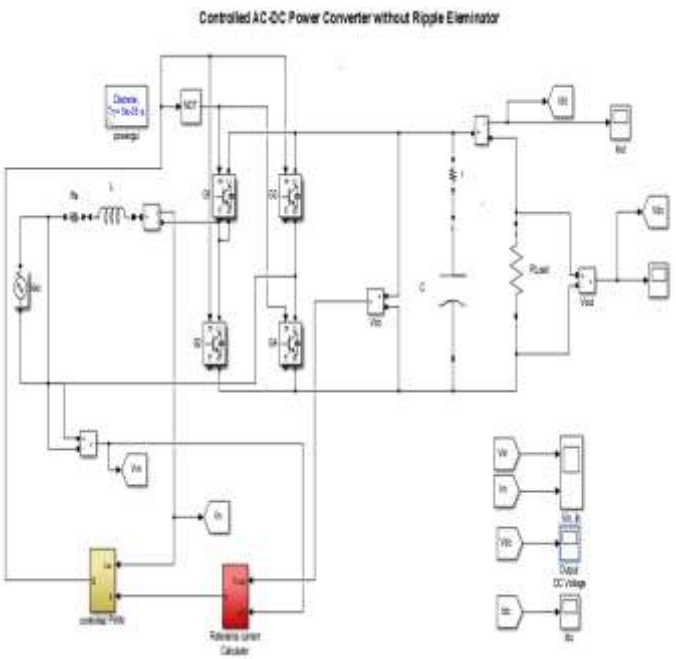

FIGURE 9. (A) Simulationcircuit of AC-DC rectifier without ripple eliminator

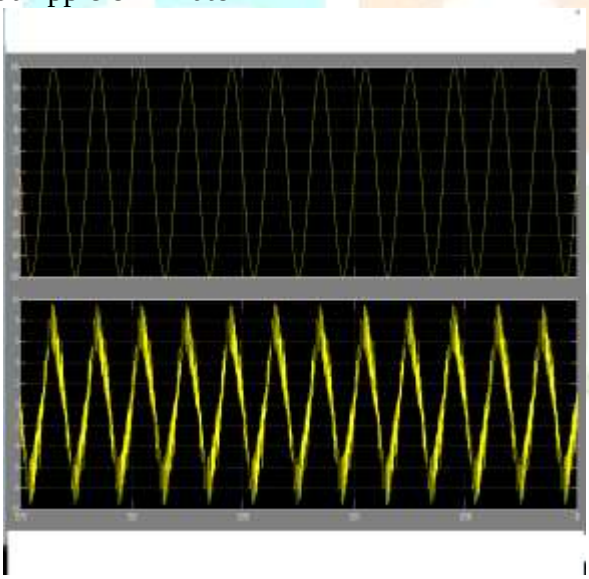

Figure 9. (B) Source voltage Vs and current Is without ripple eliminator

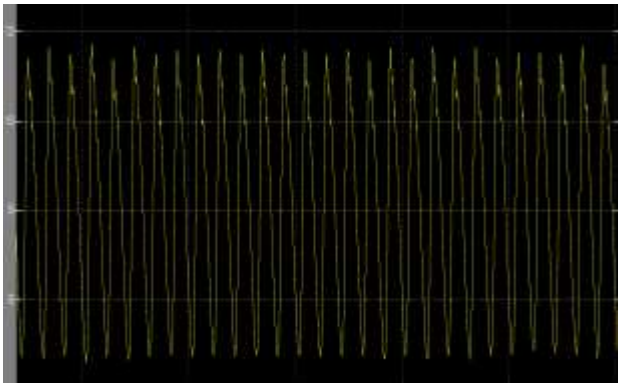

Figure 9. (C) Vdc load voltage with High Ripples when no ripple eliminator is applied.

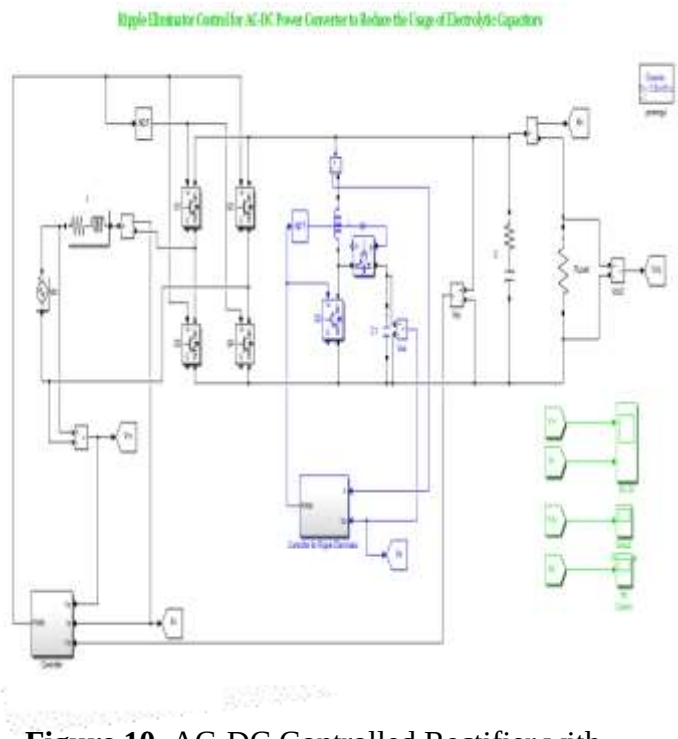

Figure 10. AC-DC Controlled Rectifier with Ripple Eliminator

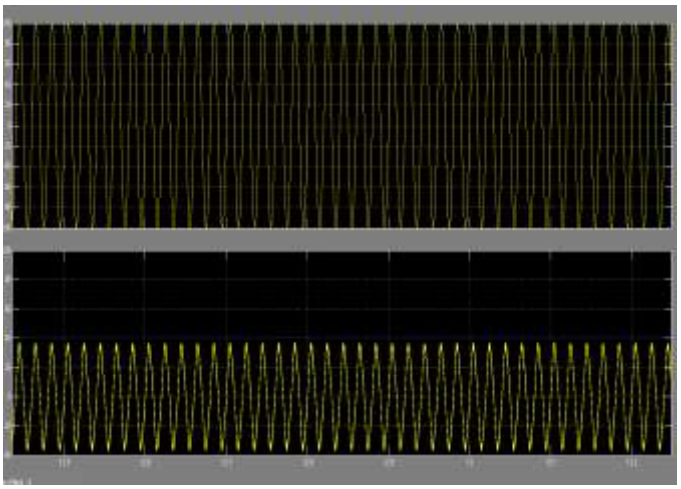

Figure 11 (A) input Vs and Is after Ripple eliminator applied to AC-DC converter

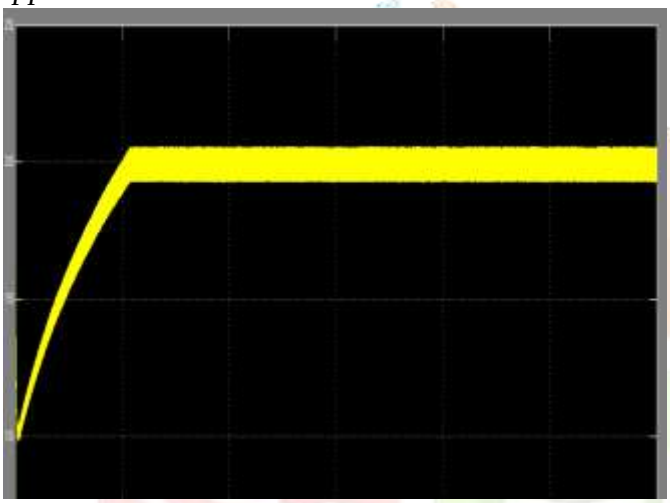

Figure 11 (B) *Steady state output Vdc with reduced ripples when Ripple eliminator applied*

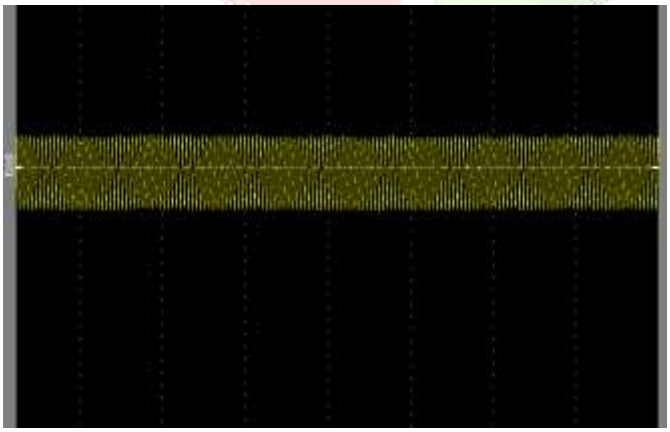

Figure 11(C) *Reduced ripples at load end when Ripple eliminator is activated*

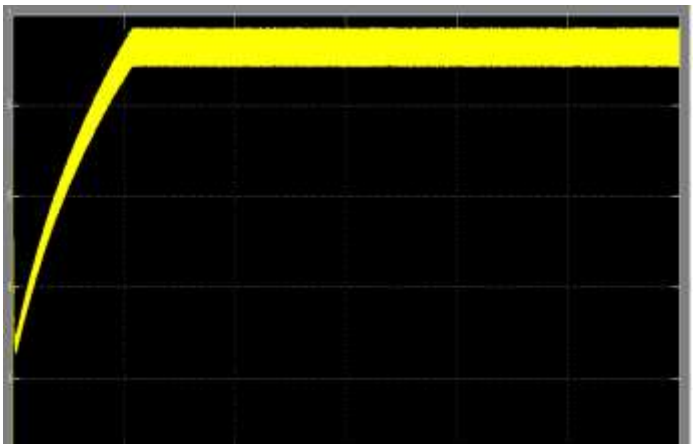

Figure 11 (D) *Reduced ripples at load current when ripple eliminator is activated*

B. VALIDATION

1) AC-DC Rectifier WITHOUT THE RIPPLE ELIMINATOR

Figure 9 shows the AC-Dc controlled rectifier circuit when modeled over Matlab/Simulink environment. Results. The input current was well regulated to be in phase with the source voltage to achieve the unity power factor. However, the ripple of the V_{DC} is around 70 V, which is often not acceptable in practice.

2) AC-DC Rectifier when RIPPLE ELIMINATOR ACTIVATED

Figure 10 shows Model based design of AC-DC controlled rectifier when applied with Ripple eliminator.

The Load side dc voltage presented have ripples in reduced quantity. Generally, it can be seen that the DC-bus voltage ripple was significantly reduced because of auxiliary capacitor connected in ripple eliminator.

4) COMPARISON

Both the circuits AC-DC rectifier with ripple eliminator and AC-DC rectifier without ripple eliminator simulated in Matlab/Simulink environment. The only difference in this topology is that the power switch Q_2 is swapped with the inductor L_a and the direction of the switch Q_1 is reversed.

In without ripple eliminator when observed the ripples at load ends is around 75V, which not acceptable and also reduce the life time of the system because many of the controlled rectifiers are used in automotive and solar energy application which more sensitive to the inputs.

Whereas in with ripple eliminator the load side voltage ripple is of 4V which very less compared to without ripple eliminator concept.
It means 95% ripples are reduced when compared to without ripple eliminator concept.
When observed the in with ripple eliminator the input voltage applied is 100V input and out observed is 200V DC output with drastic reduction in the voltage ripples.

VII. CONCLUSIONS

The concept of Ripple eliminators is implemented and results are validated. A controlled AC-DC power converter used as an example for validation of eliminators. The methodology of eliminators has been further developed to improve the power quality and reduce the voltage ripples in DC systems and, at the same time, reduce the capacitance needed and the usage of electrolytic capacitors.

Rectifier without ripple eliminator is developed and out voltage and current ripples are observed and after Rectifier with ripple eliminator is implemented and output results has presented. In both cases it is founded that the ripples at outvalue of without ripple eliminator is more when compared to with ripple eliminator.

The hysteresis control strategy is proposed to control one exemplar ripple eliminator, with the ripple energy provided by a single-phase PWM-controlled rectifier. It*instantaneously* compensates the ripple current on the DC bus so that the voltage ripples on the DC bus can be significantly reduced. All concept implementation is done over Matlab/Simulink.

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