High-Performance, Low Area and Low Power Consumption 32bit CSKA Implemented by Verilog HDL

K. Lakshmi Bhanu Prakash Reddy*, G. Reddy Hemantha*, Dr. S. Varadarajan*
*Assistant Professor, Aditya College of Engineering, Madanapalle,
*Research Scholar, JNTUA, Annthapuramu
*Professor, S V University, Tirupati,

Abstract

Adders are basic important logic blocks used in Digital Signal Processors, Digital filters and widely used in the Digital Integrated Circuits and also in Analog ICs. In this paper, a Carry Skip Adder structure that has a higher Performance, Low area as well as lower energy consumption compared with other adders is presented. The speed and reduction in the design area or space can be achieved by using "HYBRID MUX" and 4T XOR Gate instead of conventional MUX for skip logic and to generate partial products respectively in the existing method. In addition, instead of utilizing Compound gates (AND OR INVERT & OR AND INVERT), the proposed structure makes use of "HYBRID MUX" for the skip logic and automatically the number of transistors are reduced. Here with proposing a model evaluated with the comparison of their speed, delay, area & energy/power consumption with that various adders utilized a 45nm cmos technology. The results that are obtained by Xilinx 12.3 version tool. Simulation results reveals, about 44% and 39% better performance in the delay & energy, respectively compared with conventional one. The required design area reduced by reducing the usage of more no of transistors while designing the XOR gates. The Power Delay Product (PDP) is the lowest among all adders.

Keywords: Hybrid Mux, CSKA,4T XOR gate, nmos ,pmos , high speed, low area.

1. INTRODUCTION

The essential increasing demand for Mobile Electronic devices requires use of most power efficient, low area and high speed in VLSI Circuits. Addition operation plays a vital role in digital circuits and analog ICs and is the most arithmetic operation in processors, Filter designs and DSP Applications. In Arithmetic and Logic Units [1] adder circuits play an important role and so improving speed and minimizing power consumption mainly affect the speed, area and power consumption of DSPs, Filters and Processors. There are various methods on the subject of minimizing the power and speed of these units, which have been discussed in [2]-[9]. Sincerely, it is highly desirable to achieve higher speeds at low energy/power consumptions, which is a challenging case for the VLSI designers.

As there is Quadratic dependence of the switching energy on the voltage, the one of the main technique to lower the energy/power consumption of digital circuits is to reduce the Supply Voltage

$$Pd = C_l*(Vdd)^2*f$$

A Complex Digital Signal Processors contain many adders. The Designers are forced with more constraints are high speed, high throughput, small silicon area and low power consumption. Many design styles of adders available in VLSI. Although, Ripple carry adders (RCA) are the small in design structure but it's very slower. Recently, carry-skip Adders are used popularly due to their performance of high speed and smaller size. There are various adder families with different power consumptions, area and delays usages. The examples include RCA, CIA, CSKA, CSLA and PPAs may be found in [1] and [13].

The CSKA, which is an effective adder in terms of area usage, power consumption, was discussed in various papers. The critical path delay of the CSKA is much smaller than the RCA, but the Power Consumption and its area usage is similar to RCA. The power delay of the CSKA is smaller than that of the Parallel Prefix Adders and CSLAs. In addition to this, due to small number of transistors, the CSKA benefits from the wiring lengths. The CSKA structure, on reducing its delay by using static CMOS Logic. The proposing method improves the speed considerably by maintaining the low power consumption and area properties of CSKA. Hence, the contribution of this paper can be summarized as follows.

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Here the Proposing a customized CSKA structure by using HYBRID MUX instead of conventional multiplexer, compound gates and 4T XOR Gates instead of conventional XOR gates in the existing once. The rest of the paper is ordered as follows. Section 2 describes about the existing methods and section 3 describes about the proposed method. Section 4 shows the simulation Results. Finally, the Conclusion is drawn in section 5.

2. EXISTING METHODS

Conventional carry skip adder (existing method 1):

The block diagram of an N-bit Conv. CSKA mainly Contains the blocks of the Ripple Carry Adder, is as shown in the Figure 1. CS logic including the Chain of FULL ADDERs in each stage.

An RCA Contains N cascaded (Series connected) FULL ADDERS, the worst propagation delay of the addition of two N-bit numbers, A and B, belongs to where all the FULL ADDERS are in Propagation mode [1]. The CARRY SKIP operation can be performed by the multiplexers as shown in the above Figure 1.

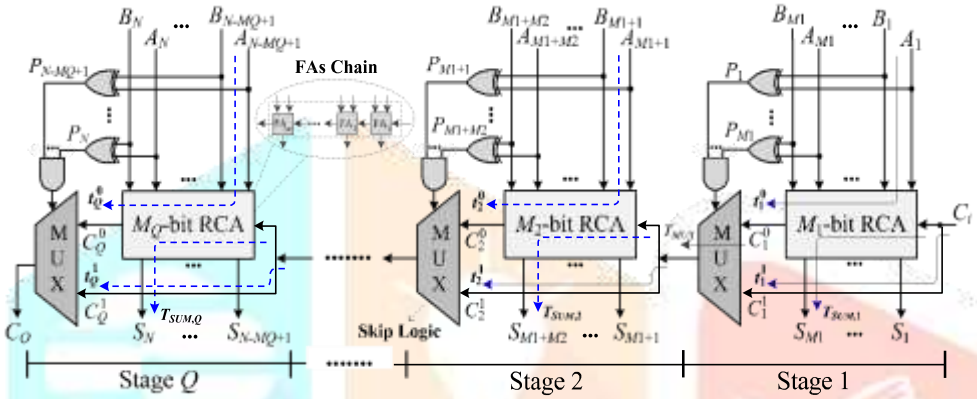

Figure 1. Conventional Carry Skip Adder

To design this Conventional Multiplexer 12 transistors are required. So the propagation delay and area of the design also increases. To diminish the propagation delay one may exercise the Compound gates for the SKIP Logic. The Power using up of the compound gates (AOI and OAI) less significant than that of multiplexer but the power consumption of the CI-CSKA (EXISTING METHOD 2) is more than that of CONVENTIONAL CSKA.

***CI-CSKA Existing Method 2*:**

The following figure.2 containing Concatenation and Incrementation methods with the conventional CSKA block diagram, and consequently it is denoted by CI-CSKA . In this compound gates were used for carry skip logic instead of using multiplexers and the sum can be produced from the incrementation blocks. The incrementation blocks contains XOR gates and AND gates (HALF ADDERS).The CI-CSKA as shown in the below Figure 2.

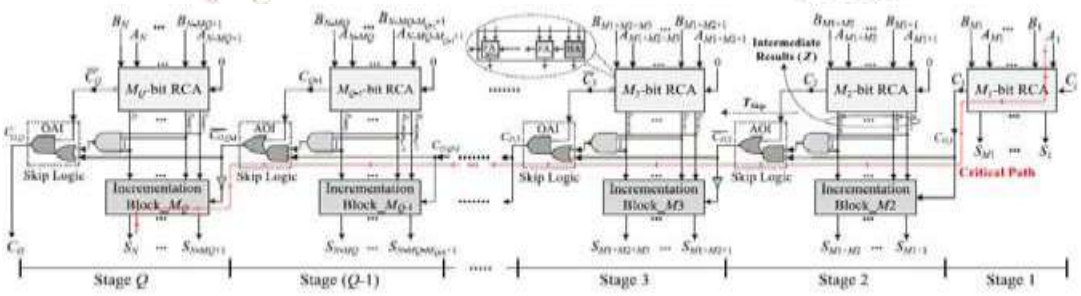

Figure 2. CI-CSKA

Due to this Incrementation blocks Area of the design increases and propagation delay also increases. In this adder the designer may give zero the carry input signal for the each RCA block as shown in above figure. On each consequent stage the generated carry is complemented and also one NOT gate is used to compliment the carry. It increases the delay area and power but speed of the operation is highest. But the CS Logic (AOI or OAI compound gates) is not able to avoid the zero carry input until the zero carry input propagates from the analogous RCA block. To work out this problem, in the proposed method the Carry Skip logic can be implemented by using —HYBRID MUX , and instead of using 12T XOR Gate , the 4T XOR gates are used to generate the Partial products which acts as an

inputs for the 8 input AND gate. The details of proposed method is discussed in the following section

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3. PROPOSED METHOD

3.1. HYBRID MUX:

Hybrid Mux is similar to the CMOS Inverter. The Hybrid Mux consists of One NMOS, One PMOS and two NOT gates. The structure of hybrid mux as shown in below Figure 4.It contains 2 Inputs and one Output and one Conditional signal. The Hybrid Mux having one NMOS, one PMOS followed by two NOT gates as shown in the Figure4. To design the hybrid mux 2 transistors are required. The conditional signal is generated by the partial products of the Input bits. All these partial products are applied to an 8 input AND Gate to generate the conditional signal. If the conditional signal is equal to one NMOS transistor is ON and PMOS transistor is OFF. The NMOS is connected to the Cin and PMOS is connected to the Cout of the RCA block. If NMOS is ON the input carry signal is directly connected to the next stage. If the conditional signal is equal to Zero, then PMOS transistor is ON and NMOS transistor is OFF. The Cout of the RCA block can acts as a Carry signal for next stage. It reduces the propagation delay of the carry, and also reduces the design area [1].

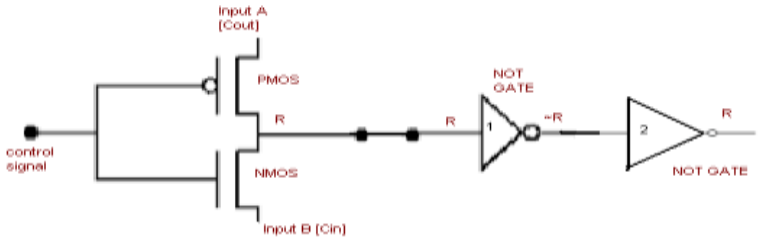

Figure 3. HYBRID MUX

3.2. 4T XOR Gate:

To design an XOR gate 12 transistors are required, so the area required to design XOR gate may increases and also propagation delay increases. Hence to reduce the no of transistors in proposed method a 4T XOR gate is designed It mainly consists of nmos and pmos transistors. It similar to the CMOS Inverters. Basically it is cascading of two CMOS Inverters as shown in below Figure 4.

Operation:

The first stage CMOS inverter, the PMOS drain is connected to the V_{dd} and source is connected to the NMOS drain and source of NMOS is connected to the ground. The gate terminals of both pmos and nmos are connected to the input1.the output of the first stage is connected to the source of second stage nmos and pmos drain is connected to the input1.the gate terminals of the second stage are connected to the input2 and the source of pmos and drain of the nmos tied together to get the XOR output.

When the V_{dd} is ON based on the input1 condition either pmos or nmos is ON and generate the complement. The following table shows the operation of 4T XOR GATE.

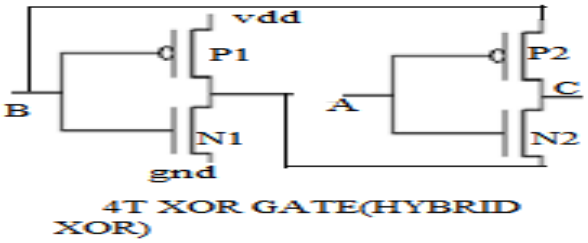

Figure 4: 4T XOR Gate

Table 1

INPUTS		PMOS	NMOS	PMOS	NMOS	OUTPUT
A	B	P1	N1	P2	N2	A xor B
0	0	ON	OFF	ON	OFF	0
0	1	OFF	ON	ON	OFF	1
1	0	ON	OFF	OFF	ON	1
1	1	OFF	ON	OFF	ON	0

3.3. Proposed Hybrid CSKA:

In the proposed method the Skip logic can be implemented by — HYBRID MUX instead of conventional Mux and also compound gates. And also to shrink the area of the design the partial product generator circuit can be implemented by 4T transistor XOR Gates instead of 12T transistor XOR Gates in existing methods. By using this hybrid mux and 4T XOR gates speed of the operation increases, power consumption decreases and also the design area reduces. The proposed method of CSKA as shown in below Figure 5.

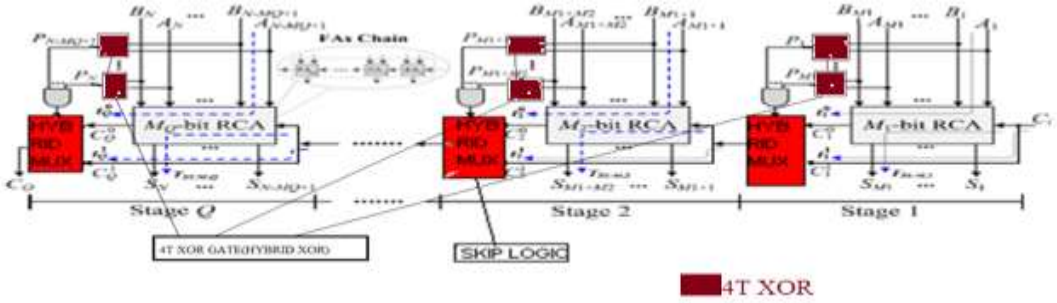

Figure 5. Proposed Hybrid CSKA

4. SIMULATION RESULTS

In this the simulation results are obtained by using the Xilinx tool. The coding of the design is written in Verilog HDL language and simulated. The Simulation is analysed in Xilinx 12.3 version. The simulation results as shown in the Figure 6. Here the Table 2 shows the comparison of number of LUTs, power consumption, delay and number of IOBs of the CONV CSKA, CI-CSKA, MODIFIDE CSKA and Proposed CSKA. And the remaining report shows synthesis analysis and proposed method results.

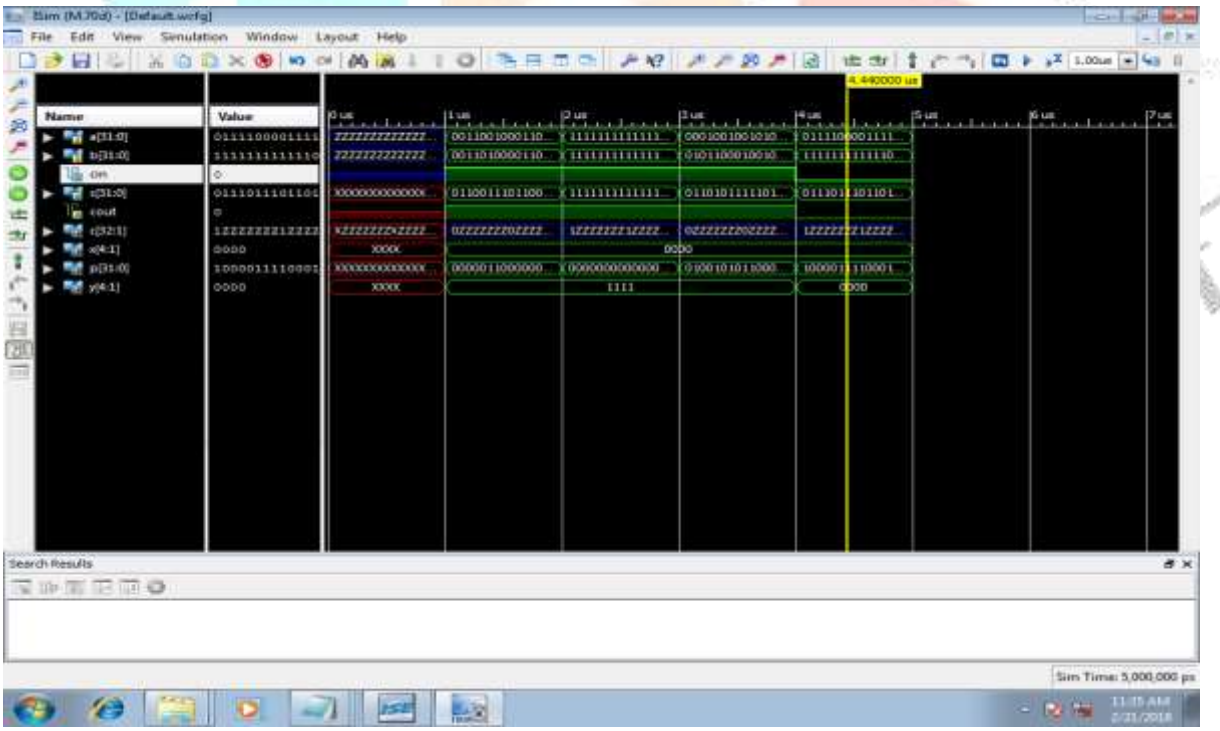

Figure 6. Simulation Results

***DESIGN SUMMARY*:**

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Partition Implementation Status
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  No Partitions were found in this design.

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Generating "PAR" statistics.

Timing Score: 0 (Setup: 0, Hold: 0)


Generating Pad Report.
```

cska32 Project Status			
Project File:	bhanuprakash.xise	**Parser Errors:**	No Errors
Module Name:	cska32	**Implementation State:**	Synthesized
Target Device:	xc3s500e-4fg320	• **Errors:**	X 4 Errors (0 new)
Product Version:	ISE 12.3	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Feb 21 12:45:40 2018	X 4 Errors (0 new)	0	0
Translation Report	Current	Wed Feb 21 12:46:06 2018	0	0	0
Map Report	Current	Wed Feb 21 12:46:09 2018	0	0	2 Infos (2 new)
Place and Route Report	Current	Wed Feb 21 12:46:17 2018	0	0	1 Info (1 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed Feb 21 12:46:20 2018	0	0	5 Infos (5 new)
Bitgen Report	Current	Wed Feb 21 12:46:30 2018	0	0	0

Device Utilization Summary:

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	54	9,312	1%	
Number of occupied Slices	48	4,656	1%	
Number of Slices containing only related logic	48	48	100%	
Number of Slices containing unrelated logic	0	48	0%	
Total Number of 4 input LUTs	64	9,312	1%	
Number of bonded IOBs	98	232	42%	
Average Fanout of Non-Clock Nets	1.74			

Comparison:

LOGIC Utilization	CONV CSKA	CI-CSKA	MODIFIDE CSKA	HYBRID CSKA
No. of LUTs	72 Out of 9312	75 Out of 9312	68 Out of 9312	57 Out of 9312
No. of bonded IOB s	98 Out of 242 (42%)	98 Out of 242 (42%)	98 Out of 242 (42%)	98 Out of 242 (42%)
Delay(ns)	15.386	10.731	10.112	7.714
Power consumption(%mw)	17	16	16	6

5. CONCLUSION

In this manuscript, a static cmos CSKA construction called HYBRID CSKA was proposed, which has a lower power consumption and reduction in the design area and higher speed/performance compared with the conventional one. The high speed/performance and low area and energy efficient can be achieved by using the Hybrid Mux for the skip logic and 4T XOR gate for the generation of partial products in the proposed method. The simulation results suggested that the CSKA structure is a useful adder for the applications where the speed, Power/Energy consumption and Area are critical.

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