IMPLEMENTATION OF FUZZY BASED DUAL-BUCK HALF-BRIDGE VOLTAGE BALANCER IN DC MICRO-GRID

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Abstract: Micro-dc grid is a novel power system focused on the development of renewable resources. Two-wire transmitting power mode is generally accepted in a micro-dc grid, which is usually not suitable for the requirements of the input voltage levels of different power converters and loads. A half-bridge voltage balancer was introduced in a micro-dc grid, which can convert a two-wire mode into a three-wire mode in a micro-dc grid via a neutral line. However, the shoot-through problem existing in bridge-type converters degrades the reliability of the voltage balancer. In this paper, a dual-buck half-bridge voltage balancer and a control strategy like Fuzzy is proposed, which can avoid the shoot-through problem. The small-signal model of the voltage balancer is derived for designing the control parameters and the current relationships of the inductors; the capacitors and the unbalanced loads are analyzed particularly. Finally, a prototype, which can deal with 2-kW unbalance ability, is built to verify that the proposed voltage balancer may have a good ability of balancing the voltage by building a neutral line.

IndexTerms **- Buck converter, DC distribution system, Half bridge, Micro-dc grid, Voltage Balancer, MATLAB/Simulink.**

I. INTRODUCTION

A Micro-Dc grid based on distributed generation system, which can supply super high-quality electric power, is widely focused on in recent years with the development of renewable resource generations [1]–[8]. The use of the direct current allows simplifying the insertion between the distribution generation and the network. It needs only one interface converter with alternating current grid to make the operation in islanding mode easier, without compromising the safety of the public network [9], and it has a distinct benefit—a line loss reduction [10]. A micro-dc grid is also dependent on all types of interfacing converter, such as bidirectional converter and dc converter [11], [12], grid- connected inverter [13]–[15], voltage balancer [1]–[7], and so on. However, a micro-dc grid usually has only one voltage level in two-wire dc distribution system, and it is impossible to supply some types of loads at half voltage such as dc/ac inverters needing a neutral line, converters with input voltage balancing like half-bridge converter and three-level half-bridge converter, and so on. In particular, when a micro-dc grid is used in domestic and office places, a neutral line connected to ground is favorable to the security of the persons. Obviously, in practice, a micro-dc grid with two-wire power system is impossible to meet the requirements of all electronic devices. Thus, a half-bridge voltage balancer was specially introduced to build a neutral line [1]–[7], which can easily convert a two-wire dc grid into a three-wire dc grid by a neutral line. In practice, the voltage balancer may be dispersedly used in any place where the voltage balance is needed, and of course, it can be placed at the output side of the power supply center for building a whole three-wire dc grid. It is thus evident that the voltage balancer improves the quality and flexibility of power supply in a micro dc grid.

Unfortunately, the topology of bridge-type converters maybe suffers from shoot-through risk, which is a major drawback to the reliability of this type of power converters. A dual-buck half-bridge converter can avoid the shoot-through problem, the freewheeling current goes through the independent freewheeling diodes instead of the body diode of the switches, and all the switches and diodes are operated at half of the line cycle; thus the efficiency may be improved [16]–[21]. In this paper, a dual-buck half-bridge voltage balancer is proposed. For meeting the characteristic of the proposed voltage balancer, a control strategy of respectively driving the two bridge legs of the proposed voltage balancer to work for a high efficiency is also presented. In order to select the parameters of filter inductors and capacitors and to design the control system parameters, the relationships of the currents of inductors, the capacitors, and the unbalanced loads are described in detail, and the small-signal model is derived. Finally, a prototype, which may deal with 2-kW power unbalance ability, is fabricated in the laboratory to verify that the dual-buck half-bridge voltage balancer may have a good ability of balancing the voltage by building a neutral line.

II. TOPOLOGY AND CONTROL STRATEGY OF THE PROPOSED VOLTAGE BALANCER

A. Typical Structure of a Micro-DC Grid

A typical structure of a micro-dc grid [1]–[7] with a voltage balancer is shown in Fig. 1, where the voltage balancer is used to construct a neutral line achieving two same voltage levels for requirements of different types of loads, such as unbalanced loads, half-bridge converter and inverter, and so on.

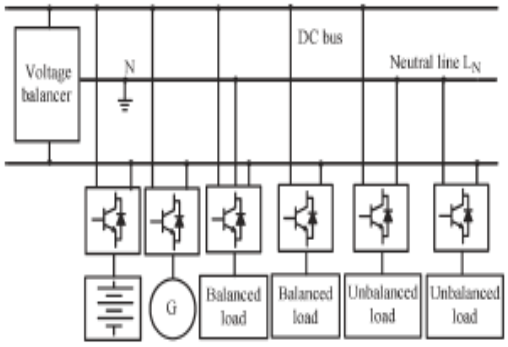

Fig. 1. Typical structure of micro-dc grid.

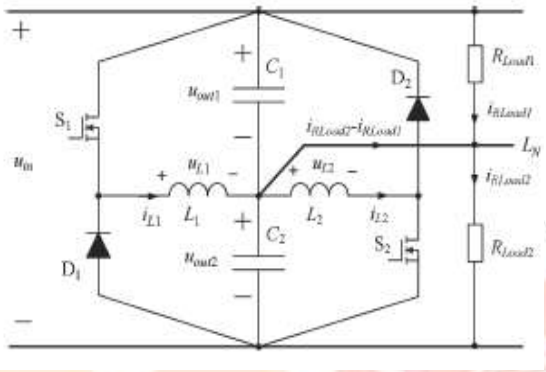

Fig. 2. Proposed dual bulk half-bridge voltage balancer.

B. Proposed Voltage Balancer

The proposed voltage balancer—a dual-buck half-bridge voltage balancer—is shown in Fig. 2, which is made up of a left bridge leg (S1,D1, *L*1), a right bridge leg (S2,D2, *L*2), and a neutral line *LN* usually connected to the earth ground. If the complementary driving technology is adopted between the switches S1 and S2, the two-inductor currents *iL*1 and *iL*2 will always exist during a switching period, and the unbalanced load current value (*iR*Load2 − *iR*Load1) is equal to the different value between the current average value *iL*1 and *iL*2. Thus, the two inductor currents will cause additional power losses. Obviously, the complementary operational technology does not use an advantage of the topology to improve the system efficiency. It is very expected to have a control strategy that can drive the left bridge leg and the right bridge leg, respectively, based on the different power quantity of the unbalanced loads.

C. Proposed Control Strategy

The proposed control strategy is presented in Fig. 3. The output signal *ue* of the voltage regulator is directly sent to control the switch S1, and its negative value (−*ue*) controls the switch S2. Combining Figs. 2 and 3, it may be concluded that, when *R*Load2 is lower than *R*Load1, the signal *ue* is positive and the left bridge leg will be driven while the right bridge leg will not work, and on the contrary, the signal *ue* is negative and the right bridge leg will be driven. It is thus clear that only one of the two bridge legs will work during every switching period and the loss of the other bridge leg will be avoided compared with the complementary driving technology.

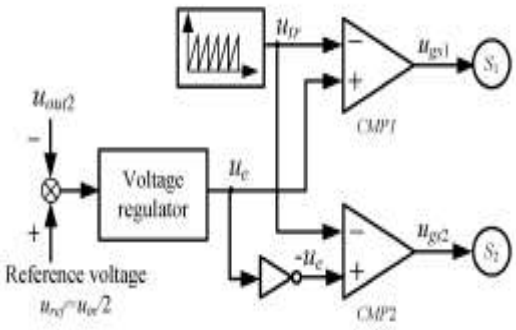

Fig. 3. Diagram of the proposed control strategy.

III. OPERATING PRINCIPLE BASED ON THE PROPOSED CONTROL STRATEGY

As similar to a buck converter, each bridge leg maybe operates in continuous conduction mode (CCM) and discontinuous mode operation (DCM). For simplifying the analysis of the operational principle, some assumptions are made: 1) All inductors and capacitors are ideal, $C1 = C2 = C$, and $L1 = L2 = L$; 2) the output voltages $u$out1 and $u$out2 are not changed during each switching process; and 3) all power switches and diodes are the ideal devices with ignored switching time and conduction voltage drop. As the operating procedures of the right bridge leg are the same as those of the left bridge leg, only the analyzing principle of the left bridge leg is given.

A. CCM of Left Bridge Leg

The driving signal $ugs1$, the current $iL1$, and the equivalent circuits are shown in Figs. 4 and 5, respectively, during CCM. From Fig. 4, there are only two main operating modes during each switching period. *1) Mode 1* [$t0$, $t1$] *[Refer to Figs. 4 and 5(a)]:* The switch S1 is turned on at the time $t0$, and the current $iL1$ increases linearly

$$L_1 \frac{di_{L1}}{dt} = u_{in} - u_{out2} = u_{out1}. \qquad (1)$$

During this mode, the input voltage u_{in} sends additional energy to the load R_{Load2} through the inductor L_1. The voltage stress of the freewheeling diode D1 is the input voltage u_{in}.

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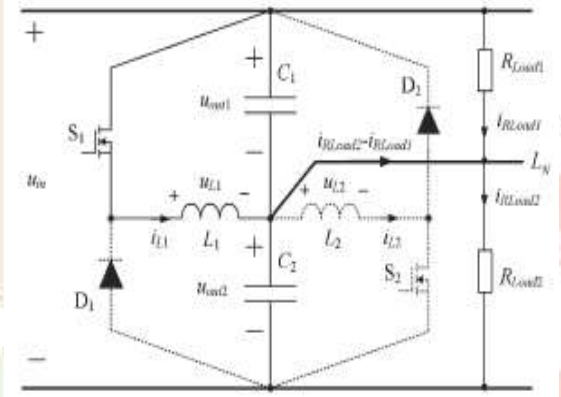
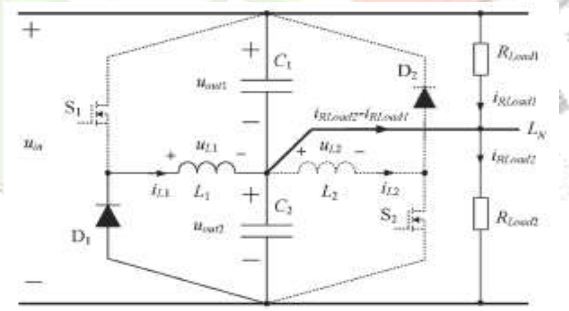


(a)



(b)

Fig. 5. Equivalent circuits under CCM. (a) Mode 1. (b) Mode 2.

2) Mode 2 [$t1$, $t2$] *[Refer to Figs. 4 and 5(b)]:* The switch S1 is turned off at the time $t1$, and the current $iL1$ will continue to run through the freewheeling diode D1. The current $iL1$ decreases linearly

$$L_1 \frac{di_{L1}}{dt} = -u_{out2}. \qquad (2)$$

The procedure will end when the S1 is turned on again at the time $t2$. During this mode, the voltage stress of the switch S1 is also the input voltage $u$in. From the time $t2$, a next operating period will start. As the voltage $u$out1 is the same as $u$out2 under the stabilization and a voltage-second product of an inductor is zero during ca period, it can be concluded

$$u_{out1}(t_1 - t_0) = u_{out2}(t_2 - t_1). \qquad (3)$$

Thus, the time ($t1 - t0$) is equal to the time ($t2 - t1$), i.e., the turn-on time is equal to the turnoff time.

B. DCM of Left Bridge Leg

There are three operating modes under DCM. The *ugs*1, *iL*1, and equal circuits are shown in Figs. 5–7, respectively. From Fig. 6, it can be concluded that the mode 1 [*t*0, *t*1] and the mode 2 [*t*1, *t*2] are in accordance with the two modes under CCM, respectively. Therefore, only the mode 3 [*t*2, *t*3] is given.

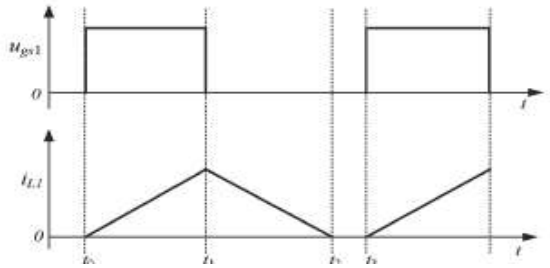


Fig. 6. Driving signal and inductor current waves under DCM.

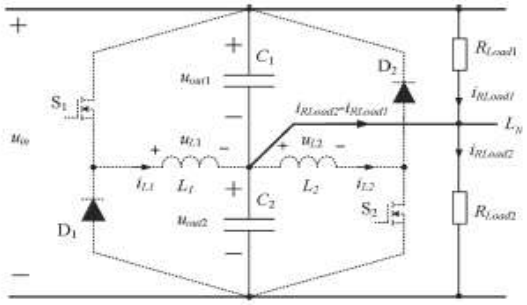


Fig. 7. Equivalent circuit of the mode 3 under DCM.

Mode 3 [*t*2, *t*3] *[Refer to Figs. 6 and 7]:* From the time *t*2, the loads *R*Load1 and *R*Load2 are supplied by the voltage sources *u*out1 and *u*out2 because the current *iL*1 decreases to zero. According to the voltage-second product of an inductor, it is got from Fig. 6

$$u_{\text{out1}}(t_1 - t_0) = u_{\text{out2}}(t_2 - t_1). \qquad (4)$$

Thus, the time (*t*1 − *t*0) is equal to the time (*t*2 − *t*1); this means that the turn-on time (*t*1 − *t*0) is smaller than the turnoff time (*t*3 − *t*1).

IV. MAIN CURRENT RELATIONSHIPS

As is known to all, the current relationship of filter inductors and capacitors is the important basis for selecting the value of filter inductors and capacitors and building an average small signal model in power converters. Therefore, the main current relationships of the voltage balancer will be analyzed in detail. For simplifying the analyses, the current relationships are defined in Fig. 8, and waveforms are shown in Fig. 9. Because of having the similar operating procedure, only the current relationships of the left bridge leg operation is analyzed. The analysis of the current relationships is divided into two parts according to the value of the inductor current *iL*1.

*A. Current iL*1 *Not Zero*

The current waveforms are shown in Fig. 9 during the time (*t*0 − *t*2). As the sum of *u*out1 and *u*out2 is equal to *u*in, the ripple voltage Δ*u*out1 of *u*out1 is also equal to the negative ripple voltage −Δ*u*out2 of *u*out2

$$\Delta u_{\text{out1}} = \frac{1}{C_1}\int_{t_0}^{T_S} i_{C1}\,dt = \frac{1}{C_2}\int_{t_0}^{T_S} i_{C2}\,dt = -\Delta u_{\text{out2}} \qquad (5)$$

where *TS* = *t*2 − *t*0 in Fig. 9(a) or *TS* = *t*3 − *t*0 in Fig. 9(b). As the average value of the current *i*1 is the load current *i*RLoad1, the ripple current Δ*i*1 is equal to the current *iC*1 of the capacitor *C*1. Thus, the ripple current Δ*i*2 is also equal to the current *iC*2 of the capacitor *C*2.

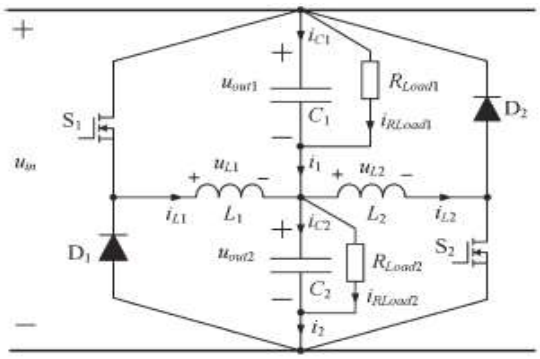


Fig. 8. Assigned diagram of the current relationships.

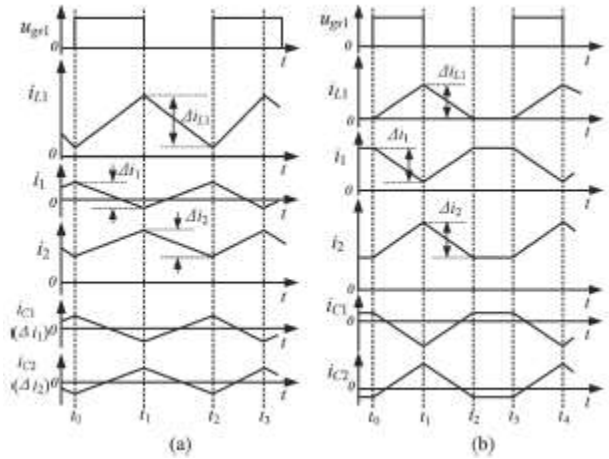


Fig. 9. Main current relationship waveforms of the left bridge leg. (a) CCM. (b) DCM.

$$\begin{cases} \Delta i_1 = i_{C1} \\ \Delta i_2 = i_{C2}. \end{cases} \quad (6)$$

According to (5) and (6), it yields under $C1 = C2$

$$\Delta i_1 = i_{C1} = -\Delta i_2 = -i_{C2}. \quad (7)$$

As $i2 = i1 + iL1$, it can be got

$$\Delta i_{L1} = \Delta i_2 - \Delta i_1 \quad (8)$$

where $\Delta iL1$ is the ripple current of the inductor $L1$. It is obtained by using (7) and (8)

$$\Delta i_{L1} = 2i_{C2} = -2i_{C1}. \quad (9)$$

Therefore, the $\Delta iL1$ is twice of the currents of $iC1$ and $iC2$.

B. Current iL1 Zero

The current relationships are shown in Fig. 9(b) between the time $t2$ and $t3$. As $iL1$ is zero, the current $i1$ and $i2$ will not be associated with the current $iL1$. That is to say, $i1 = i2$. The powers Pout1 and Pout2 of the loads RLoad1 and RLoad2 are $u2$ out1/RLoad1 and $u2$ out2/RLoad2, respectively. As the input power Pin(Pin = $u$in × $i$in) is the sum of Pout1 and Pout2 without power losses, the current $i$in is (Pout1 + Pout2)/$u$in, which is equal to $i1$ and $i2$. Due to $u$out1 = $u$out2 and RLoad2 < RLoad1 under stable condition, we can get $i2 < iR$Load2 and$i1 > iR$Load1. Thus, the capacitor $C2$ supplies a current ($iC2 = iR$Load2 − $i2$) to the load RLoad2 by discharging, which results in the $u$out2 linearly falling down, whereas the capacitor $C1$ is charged by the current ($iC1 = i1 − iR$Load1), and the $u$out1 linearly rises. Because of $u$out1 + $u$out2 = $u$in, the Δuout1 and $iC1$ are also equal to $-\Delta u$out2 and $-iC2$, respectively.

V. AVERAGE SMALL-SIGNAL MODEL

In order to select the control system parameters, the average small-signal model of the voltage balancer under CCM is derived. The duty cycles of S1 and S2 are defined as $d1$($d1 = D1 + \hat{} d1$) and $d2$($d2 = D2 + \hat{} d2$), respectively, where $D1$, $D2$, $\hat{} d1$, and $\hat{} d2$ are stable duty ratios and the perturbations of $d1$ and $d2$. Moreover, the voltage $u$in and $u$out2 are defined as $u$in = Uin + $u\hat{}$in and $u$out2 = Uout2 + uo$\hat{}$ut2, respectively, where Uin, Uout2, $u\hat{}$in, and uo$\hat{}$ut2 are the stable voltage values and the perturbations of $u$in and $u$out2.

A. Average Small-Signal Model of Left Bridge Leg

From Fig. 8, we can obtain (10) and (11) when the left bridge leg operates under CCM.

1)$S1$ turning on

$$\begin{cases} u_{L1} = L_1 \frac{di_{L1}}{dt} = u_{in} - u_{out2} \\ i_{C2} = C_2 \frac{du_{out2}}{dt} = i_{L1} + C_1 \frac{d(u_{in} - u_{out2})}{dt} + \frac{u_{in} - u_{out2}}{R_{load1}} - \frac{u_{out2}}{R_{Load2}}. \end{cases} \quad (10)$$

2) $S1$ turning off

$$\begin{cases} u_{L1} = L_1 \frac{di_{L1}}{dt} = u_{in} - u_{out2} \\ i_{C2} = C_2 \frac{du_{out22}}{dt} = i_{L1} + C_1 \frac{d(u_{in} - u_{out2})}{dt} + \frac{u_{in} - u_{out2}}{R_{load1}} - \frac{u_{out2}}{R_{Load2}}. \end{cases} \quad (11)$$

According to the methods of building average model, it can be derived from (10) and (11)

$$\begin{cases} L\frac{d\hat{i}_{L1}}{dt} = D_1\hat{u}_{in} + \hat{d}_1 U_{in} - \hat{u}_{out2} \\ 2C\frac{d\hat{u}_{out2}}{dt} = \hat{i}_{L1} + C\frac{d\hat{u}_{in}}{dt} + \frac{\hat{u}_{in}}{R_{Load1}} - \left(\frac{1}{R_{Load1}} + \frac{1}{R_{Load2}}\right)\hat{u}_{out2}. \end{cases} \quad (12)$$

Thus, the transfer function of the output voltage *u*out2 versus the duty cycle *d*1 is presented by

$$G_{out2d1}(s) = \left.\frac{\hat{u}_{out2}(s)}{\hat{d}_1(s)}\right|_{\hat{u}_{in}(s)=0} = \frac{U_{in}}{2LCS^2 + LS\left(\frac{1}{R_{Load1}} + \frac{1}{R_{Load2}}\right) + 1}. \quad (13)$$

It is obvious that the transfer function is similar to that of a buck converter.

B. Average Small-Signal Model of Right Bridge Leg

From Fig. 8, (14) and (15) may be got when the right bridge leg operates under CCM.

*1) S*2 turning on

$$\begin{cases} u_{L2} = L_2\frac{di_{L2}}{dt} = u_{out2} \\ i_{C2} = C_2\frac{du_{out2}}{dt} = C_1\frac{d(u_{in}-u_{out2})}{dt} + \frac{u_{in}-u_{out2}}{R_{load1}} - \frac{u_{out2}}{R_{Load2}} - i_{L2}. \end{cases} \quad (14)$$

2) S2turningoff

$$\begin{cases} u_{L2} = L_2\frac{di_{L2}}{dt} = (u_{in} - u_{out2}) \\ i_{C2} = C_2\frac{du_{out2}}{dt} = C_1\frac{d(u_{in}-u_{out2})}{dt} + \frac{u_{in}-u_{out2}}{R_{load1}} - \frac{u_{out2}}{R_{Load2}} - i_{L2}. \end{cases} \quad (15)$$

According to the methods of building average model, (14) and (15) are rewritten by

$$\begin{cases} L\frac{d\hat{i}_{L2}}{dt} = \hat{u}_{out2} - (1-D_2)\hat{u}_{in} + \hat{d}_2 U_{in} \\ 2C\frac{d\hat{u}_{out2}}{dt} = C\frac{d\hat{u}_{in}}{dt} + \frac{\hat{u}_{in}}{R_{Load1}} - \left(\frac{1}{R_{Load1}} + \frac{1}{R_{Load2}}\right)\hat{u}_{out2} - \hat{i}_{L2}. \end{cases} \quad (16)$$

The transfer function of the output voltage *u*out2 versus the duty cycle *d*2 is given by

$$G_{out2d2}(s) = \left.\frac{\hat{u}_{out2}(s)}{\hat{d}_2(s)}\right|_{\hat{u}_{in}(s)=0} = \frac{-U_{in}}{2LCS^2 + LS\left(\frac{1}{R_{Load1}} + \frac{1}{R_{Load2}}\right) + 1}. \quad (17)$$

Comparing (13) and (17), the right bridge leg is running backward buck converter. Moreover, combining Fig. 3, (13), and (17), the control system diagram of the voltage balancer can be illustrated by Fig. 10, where *Km* is the amplitude of the unipolar triangle carrying wave *utr*, *k* is the feedback coefficient, and

$$G_{out2d}(S) = \frac{U_{in}}{2LCS^2 + LS\left(\frac{1}{R_{Load1}} + \frac{1}{R_{Load2}}\right)}.$$

It is obvious that *G*out2*d*(*S*) is similar to the transfer function of a buck converter, and thus, the designing method of the control system parameters of the voltage balancer may be according to that of a buck converter.

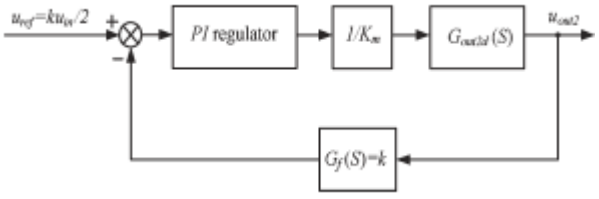


Fig. 10. Control system diagram.

VI. SIMULATION RESULTS

In order to confirm the aforementioned analysis, the computer simulations of the main current relationships and the loads transiently changing are carried out by using software Saber, and the other condition simulations are ignored. Considering single phase 110 V for a half-bridge inverter and single phase 220 V for a full-bridge inverter, the dc bus voltage (input voltage *u*in) is

selected to be 360 V. The other main simulation parameters are listed: switching frequency of 25 kHz, $L1 = L2 = 230\ \mu$H, and $C1 = C2 = 470\ \mu$F.

A. Simulations of the Current Relationships

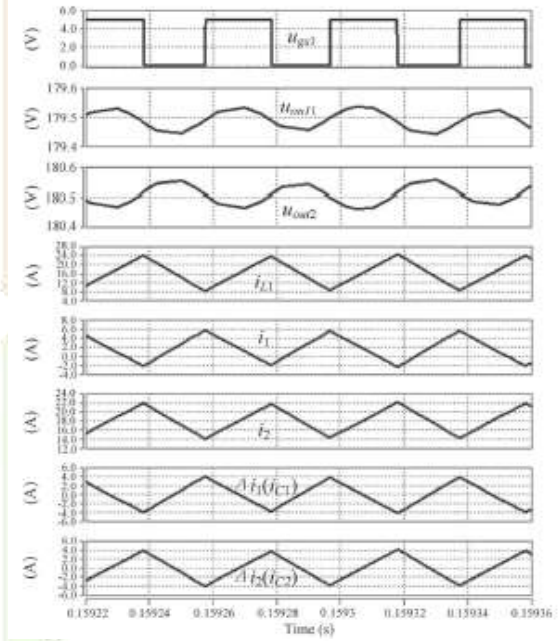
In this section, only the simulation results of the current relationships of the left bridge leg are given. The simulation results of the current relationships are given in Fig. 11. In Fig. 11, it includes CCM [RLoad1 = 100 Ω and RLoad2 = 10 Ω as shown in Fig. 11(a)] and DCM [RLoad1 = 40 Ω and RLoad2 = 30 Ω as shown in Fig. 11(b)]. As seen from Fig. 11, under nonzero $iL1$, it can be easily concluded that Δuout1 = $-\Delta u$out2, $iC1 = iC2$, and $\Delta iL1 = iC2 - iC1$.

When the inductor current $iL1$ is zero, we can get Pout1 = u2 out1/RLoad1 = 810 W, Pout2 = u2 out2/RLoad2 = 1080 W, $i$in = (Pout1 + Pout2)/$u$in = 5.25 A, $i2 = i1 = i$in = 5.25 A, iRLoad1 = $u$out1/RLoad1 = 4.5 A, and iRLoad2 = $u$out2/RLoad2 = 6 A under steady state.

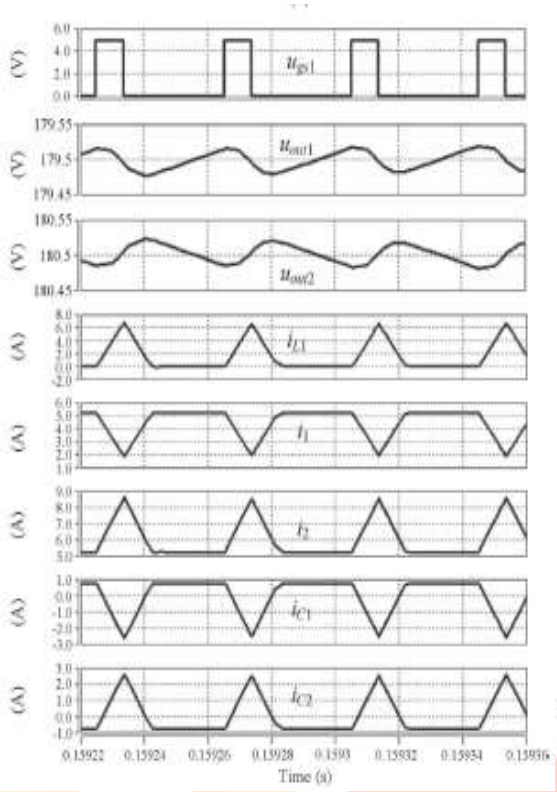
Because of $i2 < iR$Load2, the lacking current ($i2 - iR$Load2 = −0.75 A = $iC2$) is supplied by the capacitor $C2$ discharging, and the voltage $u$out2 linearly drops. Due to $i1 > iR$Load1, the capacitor $C1$ is charged by the surplus current ($i1 - iR$Load1 = 0.75 A = $iC1$), and the voltage $u$out1 linearly rises. These states are presented in Fig. 11(b).

B. Simulations of Loads Instantly Changing

Fig. 12 shows the simulation results of loads transiently changing, where Fig. 12(a) gives the results of the load current iRLoad2 = 2.3 A and the load current iRLoad1 changes from 0 to 6.7 A; Fig. 12(b) describes the results of iRLoad1 = 1.8 A, and the iRLoad2 changes from 0 to 5 A. As seen from Fig. 12, the left bridge leg will operate when iRLoad2 is larger than iRLoad1; otherwise, the right bridge leg will run. At the same time, the output voltages $u$out1 and $u$out2 are nearly equal, although they have obvious fluctuations when the loads are instantly changed. The fluctuations are mainly

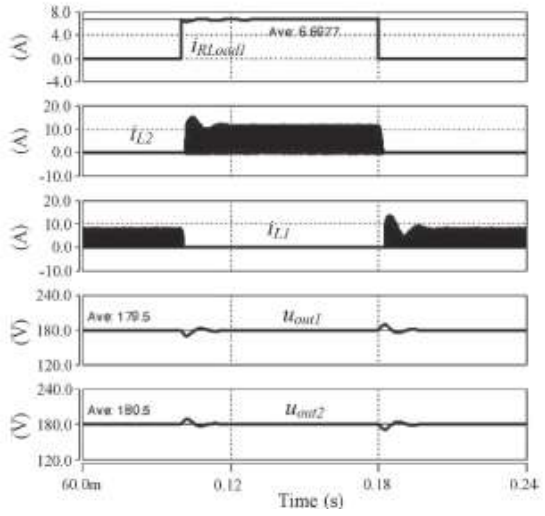


(a)

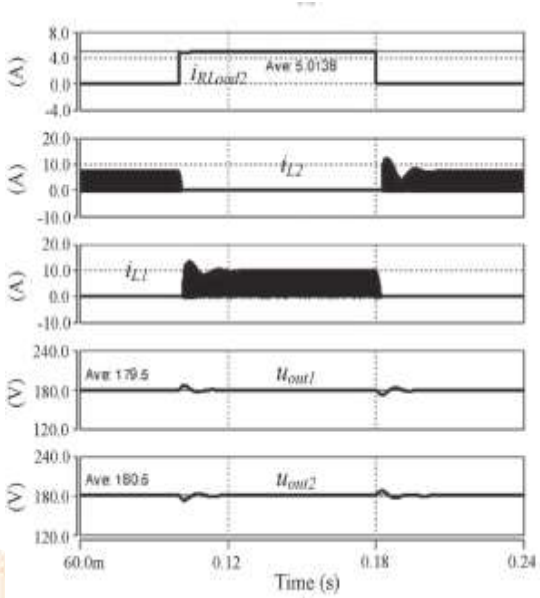


(b)

Fig.11(a) Simulation results under CCM. (b) Simulation results under DCM.



(a)



(b)

Fig.12. Simulation results under loads transiently changing. (a) *R*Load1 transiently changing. (b) *R*Load2 transiently changing.

MODELLING OF CASE STUDY

Control Strategy:

Fuzzy logic controller has been introduced in the tracking of the MPP in PV system. They have the advantage to be robust and relatively simple to design as they do not require the knowledge of the exact model. They do require in the other hand the complete knowledge of the operation of the PV system by the designer. The proposed system consist of two input variables: error (e) and change of error (CE), and one out variable, duty ratio or duty cycle (d).

The flc contains a fuzzy inference system (fis) whose structure is shown in above. The fis inputs, error (e) and change in error (ce), are obtained using the following equations

$$P(K) = V(K) * I(K)$$

$$E(K) = P(K) – P(K-1) / I(K) – I(K-1)$$

$$CE(K) = E(K) – E(K-1)$$

Where: P: The Power of the PV System
I: The Current of the PV System
E: Error
CE: Change in Error
K: Sampling Rate

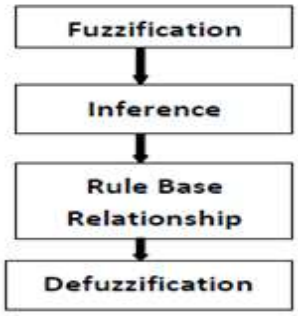


Fig 13. Step by Step Process of Fuzzy Logic Controller

Membership Function Plots:

- A membership function (MF) is a curve that defines how each point in the input space is mapped to a membership value (or degree of membership) between 0 and 1.
- Membership functions allow us to graphically represent a fuzzy set. the x axis represents the universe of discourse, whereas the y-axis represents the degrees of membership in the [0,1] interval.
- Membership functions plots, fig.a, fig.b, fig .c are the input 1, input2 and output of fuzzy controller respectively. these plots are obtained according to the rules written in the fuzzy tool box and the switching process depends upon these rules.

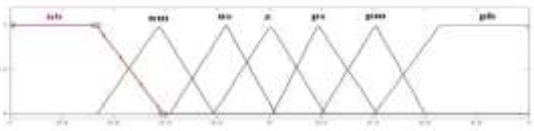


Fig.a. fuzzy membership function input 1

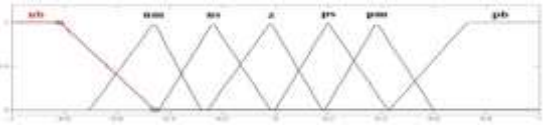


Fig.b. fuzzy membership function input 2

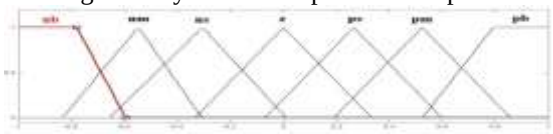


fig.c. fuzzy output membership function

SIMULATION RESULTS

➢ In order to confirm the aforementioned analysis, the computer simulations of the main current relationships and the loads transiently changing are carried out by using software MATLAB / Simulink.

➢ Considering single phase 110 V for a half-bridge inverter and single phase 220 V for a full-bridge inverter, the dc bus voltage (input voltage u_{in}) is selected to be 360 V.

The other main simulation parameters are listed:

Switching frequency of 25 kHz

$L_1 = L_2 = 230$ μH, and $C_1 = C_2 = 470$ μF

In CCM

$R_{Load1} = 100\ \Omega$ and $R_{Load2} = 10\ \Omega$

In DCM

$R_{Load1} = 40\ \Omega$ and $R_{Load2} = 30\ \Omega$

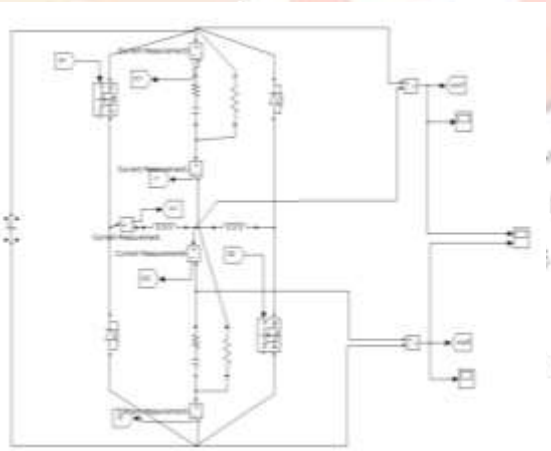


Fig.14. Simulink Model of Voltage Balancer

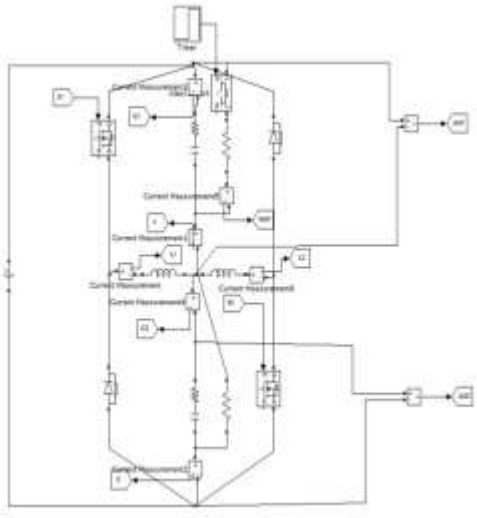


Fig.15. Simulink Model of Voltage Balancer under Transiently Changing R_{Load1}

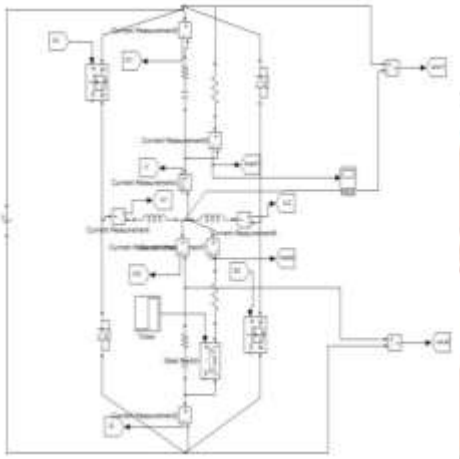


Fig16.Simulink Model of Voltage Balancer under Transiently Changing R_{Load2}

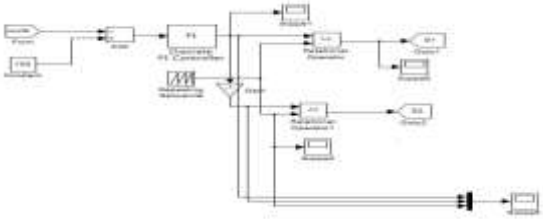


Fig17.Simulink Model of PI Control Strategy for CCM

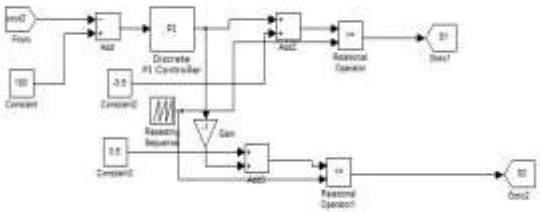


Fig18.Simulink Model of PI Control Strategy for DCM

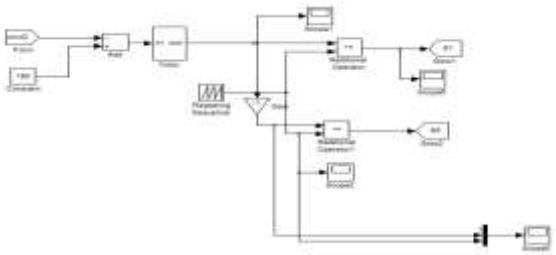


Fig19.Simulink Model of Fuzzy Control Strategy for CCM

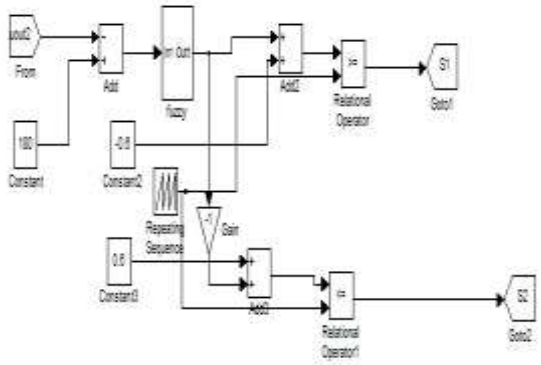


Fig20.Simulink Model of Fuzzy Control Strategy for DCM

SIMULATION RESULTS USING PI CONTROLLER

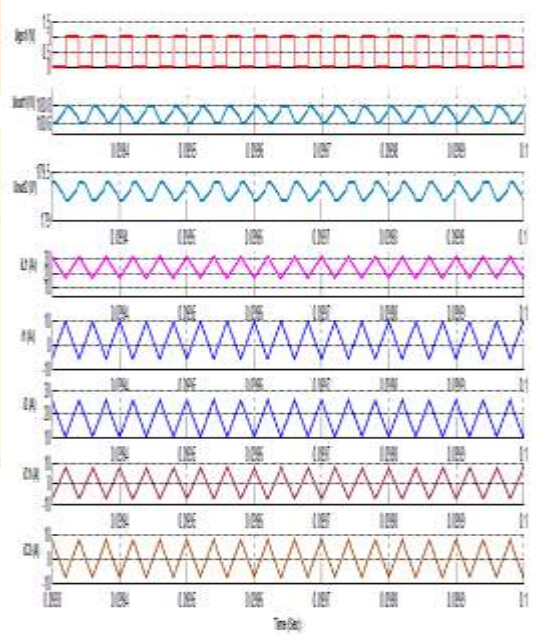


Fig21.Simulink Results of Voltage Balancer under CCM

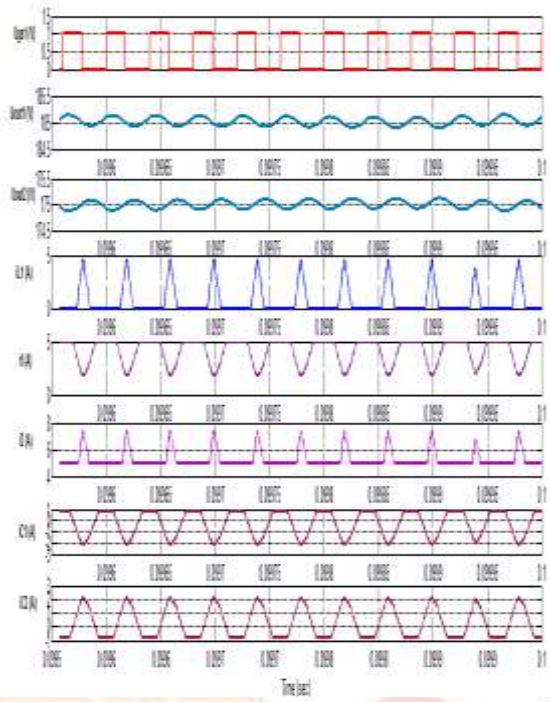


Fig22.Simulink Results of Voltage Balancer under DCM

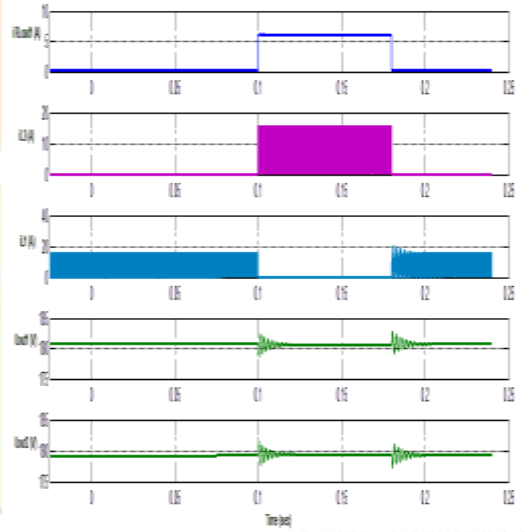


Fig23.Simulink Results of Voltage Balancer under Transiently Changing R_{Load1}

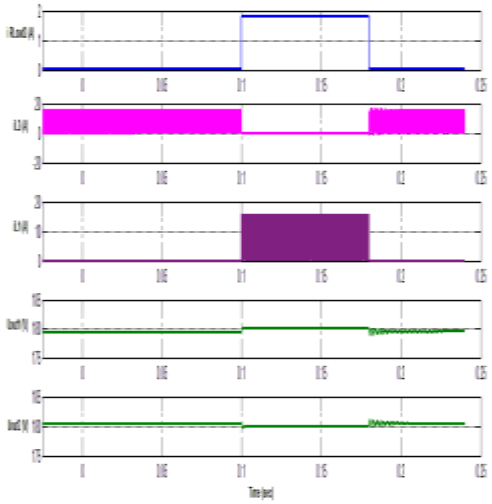


Fig24.Simulink Results of Voltage Balancer under Transiently Changing R_{Load2}

SIMULATION RESULTS USING FUZZY CONTROLLER

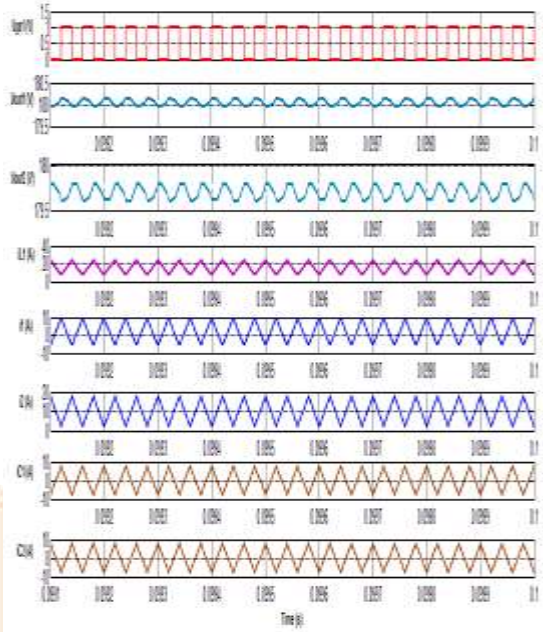


Fig25.Simulink Results of Voltage Balancer under CCM using Fuzzy

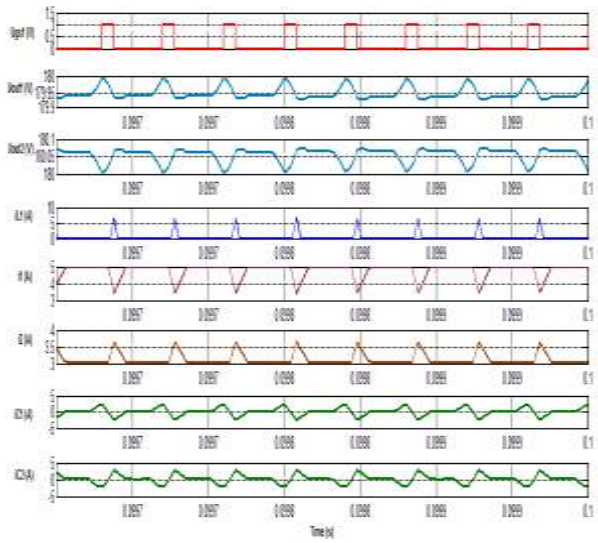


Fig26.Simulink Results of Voltage Balancer under DCM using Fuzzy

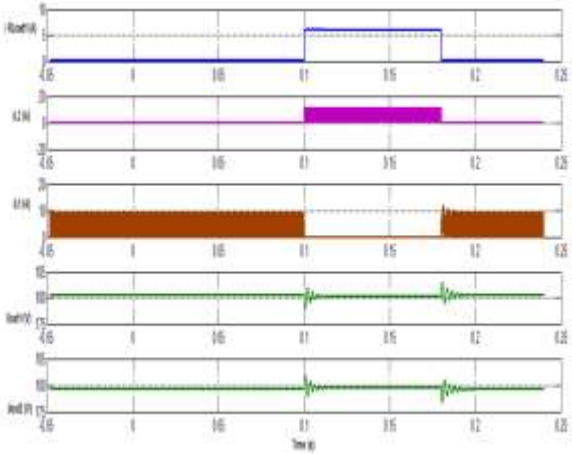


Fig27.Simulink Results of Voltage Balancer under Transiently Changing R_{Load1} using Fuzzy

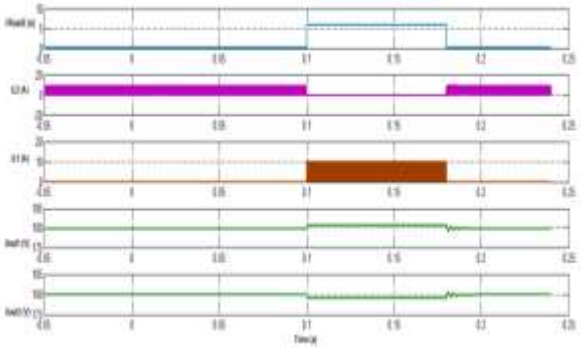


Fig28.Simulink Results of Voltage Balancer under Transiently Changing R_{Load2} using Fuzzy

RESULTS COMPARISON

Parameter	PI Controller (Simulated in Saber) (Results from the Reference Paper-I)	PI Controller (Simulated in Simulink)	Fuzzy Controller (Simulated in Simulink)
U_{out1} (V)	179.5	180.7	180.2
U_{out2} (V)	180.5	179.3	179.8
i_{L1} (A)	24	30	20
I_1 (A)	6	10	10
I_2 (A)	22	22	15
i_{C1} (A)	4	8	8
i_{C2} (A)	4	8	8

DISCONTINUOUS CONDUCTION MODE

Parameter	PI Controller (Simulated in Saber) (Results from the Reference Paper-I)	PI Controller (Simulated in Simulink)	Fuzzy Controller (Simulated in Simulink)
U_{out1} (V)	179.5	185	180
U_{out2} (V)	180.5	175	180
i_{L1} (A)	6	4	5
I_1 (A)	2	2	3.5
I_2 (A)	8	7	3.5
i_{C1} (A)	-2	-2	-2
i_{C2} (A)	2	2	2

TRANSIENTLY CHANGING $R_{LOAD\,1}$

Parameter	PI Controller (Simulated in Saber) (Results from the Reference Paper-I)	PI Controller (Simulated in Simulink)	Fuzzy Controller (Simulated in Simulink)
$I_{R\,Load1}$ (A)	6.6	6	6.2
i_{L2} (A)	10	15	10
i_{L1} (A)	10	15	10
$U_{out\,1}$ (V)	179.5	180.5	180
$U_{out\,2}$ (V)	180.5	179.5	180
Settling time for U_{out1}(s)	0.02	0.02	0.01
Settling time for U_{out2}(s)	0.02	0.015	0.007

TRANSIENTLY CHANGING R LOAD 2

Parameter	PI Controller (Simulated in Saber) (Results from the Reference Paper-I)	PI Controller (Simulated in Simulink)	Fuzzy Controller (Simulated in Simulink)
$I_{R\,Load1}$ (A)	5.01	1.8	6
i_{L2} (A)	10	15	10
i_{L1} (A)	10	15	10
$U_{out\,1}$ (V)	179.5	180.5	180
$U_{out\,2}$ (V)	180.5	179.5	180
Settling time for U_{out1}(s)	0.02	0.02	0.007
Settling time for U_{out2}(s)	0.02	0.015	0.005

CONCLUSION

In this paper, a dual-buck half-bridge voltage balancer and its control strategies (both PI and fuzzy) were implemented. This type of voltage balancer can well resolve the shoot-through problem. It can build a neutral line to balance two output voltages for different loads in a micro-dc grid. The simulation results are done to illustrate the proposed voltage balancer having a good ability of balancing output voltage even if under the different input voltage, unbalanced loads, and transiently changing loads. Fuzzy control strategy gives approximately balancing output voltage and settling time reduces in the case of transiently varying loads.

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