DESIGN OF LOW POWER ALU USING GDI TECHNIQUE

N.Srinu, M.Kedhar, O.Ajay

Abstract— the purpose of this paper is to design low power and area efficient ALU using GDI technique. Main sub modules of ALU are adder, logical unit, Subtractor, multiplexer, divider. This work evaluates and compares the performance & optimized area of ALU with conventional CMOS style &GDI technique the simulations are performed by using Micro wind tool. At first by using Micro Wind tool the circuits are designed &simulated with CMOS technique and then with GDI technique. By comparing two designs GDI&CMOS style then GDI is an advantage of less power and less area.

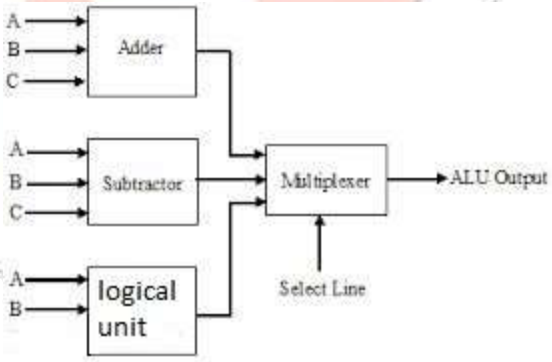
Index Terms—Adder, ALU, Comparator, GDI, Logical unit, Low power, one's complement, multiplexer, divider.

1. INTRODUCTION

Recently, the industries are in demand for low power, less area and high speed for designing the circuits. With improvement in technology and the enlargement of embedded system used electronic devices such as mobile, laptops, TV applications, power consumption, which is one of the limits in both high & low performance system, has become a primary focus in VLSI digital design.

In this paper the adder was based on regular CMOS structure .Disadvantage of this paper uses a number of transistors results in high input loads, more power consumption and larger silicon area. Morgenshtein has proposed basic GDI cell .By using this GDI cell we design ALU. In digital system design processor is main part of the system. And an ALU is one of the main components of a micro-processor. CPU works as a brain to any system & and ALU works as a brain to CPU. So it's a brain of computer's brain. They consists of fast dynamic logic circuits and have carefully optimized structures. Of total power consumption in any processor, CPU accounts a significant portion of it. Therefore, this motivate us strongly for an energy-efficient ALU designs that satisfy the high-performance requirements, while reducing power dissipation. ALU is a combinational circuit that performs arithmetic and logical operations .Arithmetic operations are basic functions and necessary for any low power, high speed application digital signal processing, image processing, and microprocessor. The internal structure of an ALU is shown in Fig.1.

Fig. 1: Internal structure of ALU



Logic Unit:

ALU can perform various logic operations like NOT, AND, OR, NAND, NOR, XOR, XNOR etc. For these operations a special unit is made called as Logical Unit. This Logic Unit performs all logic operations asked to perform. A MUX operated by select lines, for which particular logic operation to perform, is used inside this logic block.

Low Power ALU using 4:1 MUX

There is a substantial increase in the standby mode leakage power, where technology is used here is 90nm. Reducing the power consumption of the ALU is important not only because they consume a

considerable percentage of processor energy, but also because they are one of the most active and busiest component of the processor. As a result of they dissipate a lot of dynamic energy. This is aggravated by the exponential dependence of leakage on the temperature, & ALU also become a site of high leakage. The total leakage of the ALU can be given as IS, T=N.IS, i Where, N= number of transistors in the ALU IS, i= sub threshold leakage of gate i which is a function of gate length L. Similarly, the dynamic power of the ALU is given as ID=α.Ceff.Vdd2.f where α is the switching factor, Ceff. Is the total effective capacitance, Vdd is the supply voltage & f is the frequency of operation.

RELATED WORKS

• There are different types and designs of full adder which is discussed in various papers at state of the art level and process and circuit level. Twelve state of the art full adder cells are: conventional CMOS, CPL, TFA, TG CMOS, C2MOS, Hybrid, Bridge, FA24T, N-Cell, DPL and Mod2f.

• R. Shalem, E. John, and L.K. John, proposed a conventional CMOS full adder consisting of 28 transistors. Later, the number of transistor count is reduced to have less area and power consumption.

• A. Sharma, R Singh and R. Mehra, Member, IEEE, have improved performance with Transmission Gate Full adder using CMOS Nano technology where 24 transistors are used.

• The Complementary Pass-transistor Logic (CPL) full Adder contains the 18 transistors. The power consumption of this structure is 2.5µw.

• A Transmission Function Full Adder (TFA) based on the transmission function theory has 16 transistors. The power consumption of this structure is 12µw.

• N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. The power consumption of this structure is 1.62µw.

• Mod2f Full Adder contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. The power consumption of this structure is 2.23µw. • Saradindu Panda, N. Mohan Kumar, C.K. Sarkar, optimized the full adder circuit to 18 Transistor using Dual Threshold Node Design with Submicron Channel Length.

• T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy, designed 14 transistor high speed CMOS full adder and significantly improved threshold problem to 50%. Gate Diffusion Input Technique is a new method of reducing power dissipation, propagation delay with less area. We have designed ALU in different way by using GDI cells to implement multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexers and ALU is implemented by using full adder.Ex: T. Esther Rani, M. Asha Rani, Dr. Ramesh war Rao, designed an area optimized low power arithmetic and logic unit in which Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique.

EXISTING SYSTEM STRUCTURE

An arithmetic logic unit (ALU) is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. It is responsible for performing arithmetic and logic operations such as addition, subtraction, increment, decrement, logical AND, logical OR, logical XOR and logical XNOR.ALU consists of eight 4x1 multiplexers, four 2x1 multiplexers and four full adders. The 4-bit ALU is designed in 250nm, n-well CMOS technology. When logic '1'and logic '0' are applied as an input INCREMENT and DECREMENT operations takes place respectively. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation.

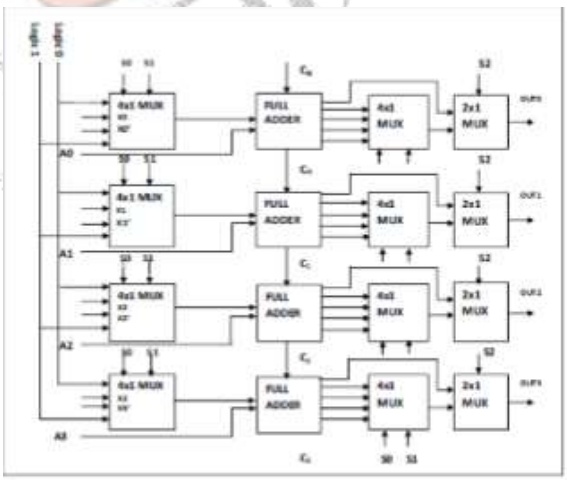


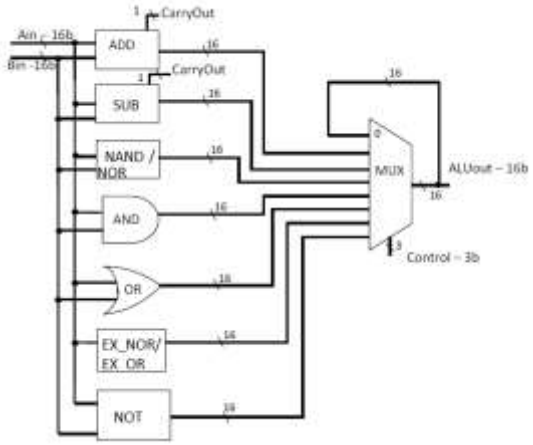
Fig 2: 4-bit Arithmetic and Logic Unit

Two's complement method is used for SUBTRACTION in which complement of B is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR.

Fig:2 shows the block diagram of 4-bit ALU where the first stage to fourth stage is cascaded with the CARRY bit. Symbolic representation of 4-bit ALU has been visualized in it. The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results. The multiplexer at the output stage selects the appropriate output and route it to output port. The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design. Shows multiplexer logic at input port. Shows multiplexer logic at output port. The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results. The multiplexer at the output stage selects the appropriate output and route it to output port. T shows the truth table for the operations performed by the ALU based on the status of the select signal.

Transistor that can be modified along with the design. Fig 2 represents the complete schematic view of ALU. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits. This paper presents a new approach using concept of Gate Diffusion Input Technique to design an arithmetic and logic unit. In an ALU, for appropriate selection of input to perform particular operation and for obtaining output accordingly multiplexer is the most applicable device. In earlier designs of ALU, the multiplexer unit is either implemented by conventional CMOS logic or by pass transistor logic which proven to have high power consumption. The approach gives better result than previous designs in terms of power consumption, propagation delay as well as area.

PROPOSED WORK:



Where we are using 8: 1 mux here.for ever select line we are having different functions like and, or, nand, nor, not, xor, xnor, adder & subtractor. Where the each logical unit is designed by using GDI technique by using the gates we are design it.

RESULT:

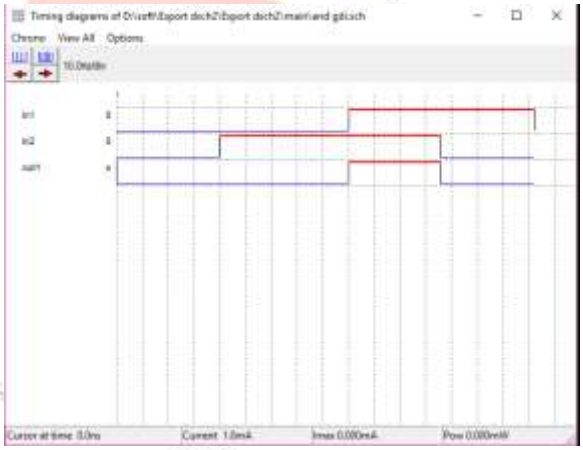


FIG: AND output

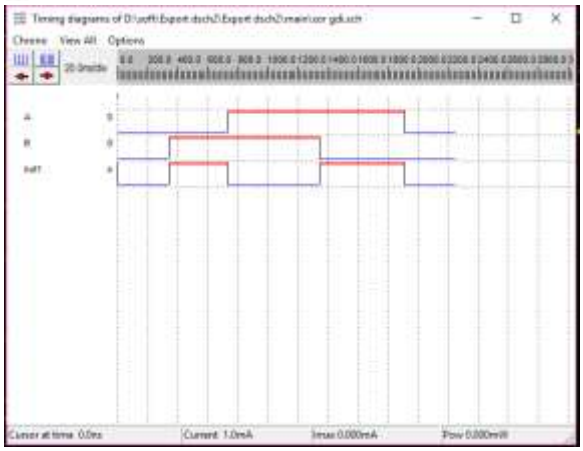


FIG: XOR output

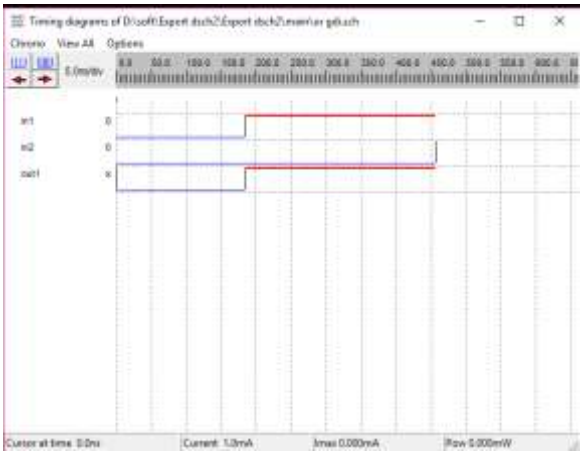


FIG :OR gate output

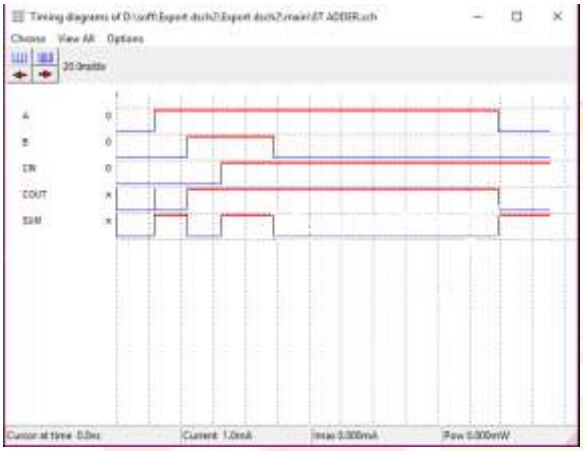


FIG: Full adder output

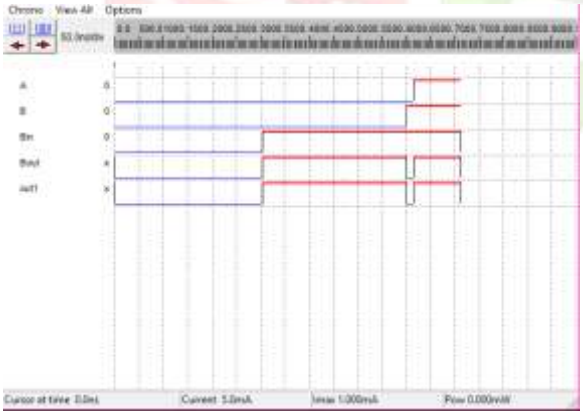


FIG: Full subtractor output

FIG: FINAL OUTPUT OF ALU

NO OF TRANSISTORS ARE USED IN ALU

	CMOS	GDI
AND GATE	4	2
OR GATE	4	2
NAND GATE	4	4
NOR GATE	4	4
XOR GATE	8	4
XNOR GATE	8	4
NOT GATE	2	2
ADDER	10	6

CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly related to dynamic power. The numbers of power supply to ground connections are reduced in GDI implementation which reduces the dynamic power consumption. This work presents a 4-bit ALU designed in 250nm technology for low power and minimum area with GDI technique. Various topologies of multiplexer and full adder implementation is studied and compared. The 2x1 multiplexer, 4x1 multiplexer, 1-bit full adder with 10- transistors designed using GDI technique is chosen for lowering power consumption and minimum possible area. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS, nMOS PTL and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques.

REFERENCES:

1) Serial Divider Using Modified GDI Technique

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2) LOW POWER AND LOW AREA ALU DESIGN USING GDI TECHNIQUE

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