FULL-SWING FAULT TOLARENCE SRAM ARCHITECTURE BASED ON MARCH TEST

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*Abstract:*In system on chips, both fault diagnosis and semiconductor random access memories are used to increase the density and dominant portion of embedded memories. In order to improve the product quality, reliability and yield the manufacturing defects should be detected, diagnosed and located. The Memory defects of system of chip can be modelled as stuck-at, coupling, transition, address decoder, and pattern-sensitive faults. Basically, in industries memory fault models and March test algorithms are used to simulate and test the chip. At last in this paper we discuss about the March test algorithm to increase speed of memory.

Index Terms - **Random Access Memory (RAM), System-on-Chip (SOC), Stuck-at Faults, Coupling Faults, Transition Faults, Address Decoder Faults, Pattern-Sensitive Faults, March Test Algorithm.**

I. INTRODUCTION

In recent years, with the widespread use of battery powered applications, such as handheld smart devices and implantable medical devices, low-power operation has become a critical issue associated with the system-on-chip (SoC) design. A low-power SoC can be effectively realized with a low-power static random access memory (SRAM) because the SRAM critically affects the total power of the SoC, owing to the fact that it occupies a large portion of the area of the SoC. Further, power reduction can be effectively achieved by decreasing the operating voltage because of the quadratic dependence of power on the operating voltage. However, at a low operating voltage, the adverse effect of the variation in threshold voltage (*V*th) becomes more significant. It should be noted that an SRAM cell is highly susceptible to variations in *V*th, given that it is designed with small transistors for high density integration. Furthermore, in the case of a conventional 6T SRAM cell, a trade-off exists between the read stability and the write ability, owing to which, it is very challenging to simultaneously achieve sufficient read stability and write ability in a low-voltage region.

Several SRAM cell alternatives with a decoupled read port have been proposed for a low-voltage operation. The advantage of adding a decoupled read port is that it eliminates the trade-off between the read stability and the write ability in the SRAM array to which the bit-interleaving is not applied; thus, the read stability and write ability can be optimized separately, facilitating a low-voltage operation. An SRAM cell is likely obtained soft errors from α-particles to address these errors. To exhibit bit-interleaving it is very necessary to use the SRAM.

In a bit-interleaved SRAM array, the selected cells are the SRAM cells targeted for the read or write operation. The row half selected cells are the SRAM cells located on the selected row and the unselected column, whereas the column half-selected cells are the SRAM cells located on the unselected row and the selected column. During the write operation, the row half-selected cells are disturbed because of the selection of the word line (WL) of the row half-selected cells. The stability of the rowhalf-selected cells will be in the SRAM design. This consideration of the stability of row half-selected cells is referred to as a half-select issue. Unfortunately, the aforementioned alternatives do not address the half-select issue without a write-back scheme. The write back scheme, in particular, ensures the stability of the row half-selected cells by reading the stored data in one cell and then writing back the same data into the same cell; however, this scheme requires additional power, delay, and area. To address the half-select issue without the write-back scheme, a 10T SRAM cell exhibiting a cross-point structure was proposed. This 10T SRAM cell includes vertical and horizontal WLs, both of which need to be selected to access the storage nodes.

During the write operation, both the WLs are selected only in the selected cell, owing to which the half-select issue is eliminated. On the other hand, a disadvantage of the 10T SRAM is that it suffers from a large area overhead to accommodate the additional transistors in its architecture. To address this disadvantage, an average-8T SRAM architecture based on a 130-nm technology was proposed; this SRAM architecture is a good alternative to the previously proposed SRAMs in that it addresses the half-select Issue with no write-back scheme, and it exhibits a competitive area. However, a drawback of this 8T SRAM is that it's read delay increases considerably when it is fabricated using a more advanced technology.

II. EXISTED SYSTEM

The below figure (1) shows the architecture of eisted system. The proposed SRAM that stores *I*bits in one block. The minimum operating voltage and area per bit of the existed SRAM depend on the number of bits in one block. A configuration that stores four bits in one block is selected as the basic configuration by considering the balance between the minimum operating voltage and the area per bit. The basic configuration of the existed SRAM includes four cross-coupled inverter pairs, pass gate transistors

(PGL1~4 and PGR1~4), block mask transistors (MASK1 and MASK2), write access transistors (WR1 and WR2), read buffers (RD1 and RD2), A head switch (P1), and cross-coupled pMOSs (P2 and P3).

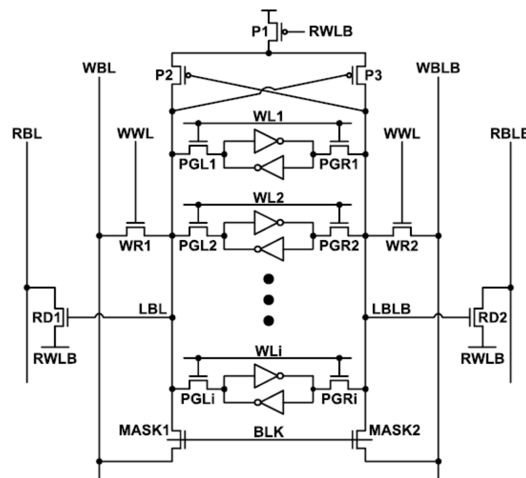

FIG. 1. EXISTED SYSTEM

The head switch and cross-coupled pMOS of the proposed SRAM are notable differences from the average-8T SRAM. This operation is performed in two phases. During the first phase, BLK of the selected block is forced to remain at 0 V, and the selected WL is enabled. The read operation in the first phase is similar to that of the average-8T SRAM, except that the RBL is not discharged because the RWLB is high in the first phase. The second phase starts with the falling of the RWLB. The assertion of the RWLB enables not only the discharge of the RBL but also the feedback of cross-coupled pMOSs.

III. PROPOSED SYSTEM

The functional model of an SRAM chip, which can often be found in the manufacturer's data sheets, consists of many blocks. Though each of the blocks of the sample model shown in Figure (2) represents a particular function and may become defective, faults in certain blocks show the same fault behavior. This model includes the address decoder and the memory cell array, and the read/write logic. Address decoder faults (AFs) are faults in the address decoder .We, assume that AFs do not change the decoder into sequential logic and will be the same during read and write operations many different faults can occur in a memory cell array these can be classified as faults which involve only a single cell.

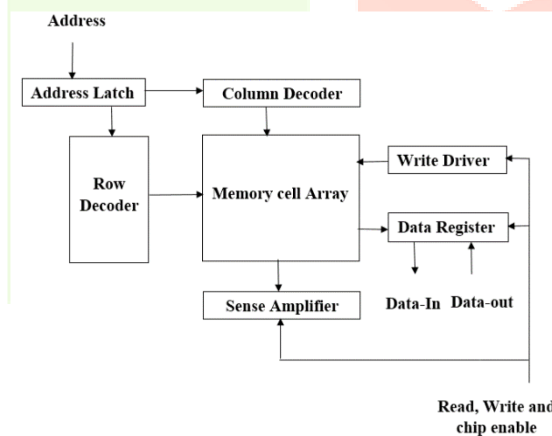

FIG. 2. PROPOSED SYSTEM

The latter class is called coupling faults (CFs). Coupling faults are divided into three types they are inversion, idempotent, and state coupling faults. Also, CFs may be linked. In a stuckst fault (SAF), the logic value of a stuck-at cell or line is always 0 or always 1. A stuck-open fault (SOF) means that a cell cannot be accessed. The differential sense amplifier has to sense a voltage difference between the bit lines of that cell. In case of an SOF, both bit lines will have the same voltage level consequently the output value produced by the sense amplifier (SA) de pends on the way it is implemented.

Operation of the SA is transparent to SOFs. When the SA has only a single input, an SOF will produce a fixed output value. Operation of the SA is non-transparent to SOFs. To broaden the read window, the SA may contain a latch. Then a SOF may have the effect that the latch is not updated because the voltage difference between the bit lines is too small. The Previous output value is produced as the output value for the SOF. So at last an efficient and reliable output is obtained from proposed system compared to exist one.

IV. RESULTS

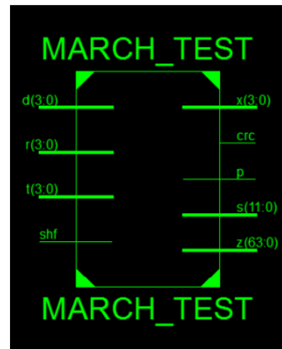

FIG. 3. RTL SCHEMATIC

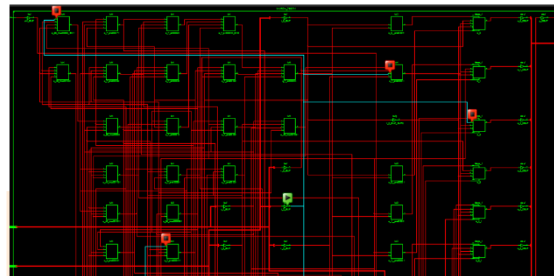

FIG. 4. TECHNOLOGY SCHEMATIC

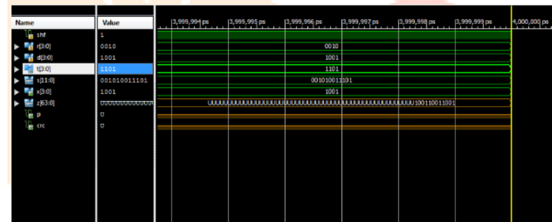

FIG. 5. OUTPUT

V. CONCLUSION

The proposed algorithm is very fast and it provides excellent solutions compared to exist one. From experimental results it can observe that this flow can save the designer many days of work by offering good BIST architectures which are complete in terms of logical and physical attributes. By using March algorithm the entire proposed system is designed. Because of this it produces better results compared to previous system. It is strongly believed that the proposed system can be widely used for the embedded memory testing especially under the SoC design environment due to the superior flexibility and extendibility in applying different combination of memory test algorithms.

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