A PERFECT REVERSE CONVERTER DESIGN FOR FIVE MODULI SET RESIDUE NUMBER SYSTEM

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***Abstract*- For designing high speed digital systems, it consider so many factors, among those the Number System, what it uses plays a crucial role. The selected number system must provide inherent properties such as Carry-free operations, Parallelism and Fault Tolerance. All these can be achieved with the use of Residue Number System (RNS). The RNS is an unconventional number system i.e., defined in terms of relatively Prime Moduli Set $\{m_1, m_2,.....,m_n\}$ that GCD $(m_i,m_j) =1$ for $i \neq j$. The RNS based system contains three major blocks, such as Forward Converter, RNS Processor and Reverse Converter. For Reverse conversion two algorithms are used i.e. Chinese Remainder Theorem (CRT) and Mixed Radix Conversion (MRC). The CRT is desirable; because of the data conversion can be parallelized, while MRC is a sequential process by its nature.**

While designing RNS, the selection of choice of moduli set plays a key role. The 3n-bit dynamic range RNS moduli set $\{2^{n-1}, 2^n, 2^{n+1}\}$ is the most famous RNS moduli set because of its simple and well formed balanced moduli. However, the arithmetic operations with respect to the modulus 2^{n+1} are complex and dynamic range is not sufficient for applications that require larger dynamic range. The 4n-bit dynamic range four moduli set minimize the dynamic range, and have long conversion delay and asymmetric moduli channel length.

In this paper, a special five moduli set $(2^n-1, 2^n, 2^n+1, 2^{n+1}-1, 2^{n-1}-1)$ for even n is proposed. It has high dynamic range $(m_1*m_2*m_3*m_4*m_5)$, while keeping the moduli small enough and converter efficient. In this paper reverse converter design is done with the CRT and the results are compared with the MRC and also with the three and four moduli sets. The required language is Verilog HDL, and the required Software tool is Xilinx ISE Design Suite 14.7. The simulator is ISim (VHDL/Verilog) and the synthesis tool is XST (VHDL/Verilog).

I. INTRODUCTION

Since the last five decades, RNS's features have been rediscovered and thus the interest in this system has been renewed. The researchers have used the RNS in order to benefit from its features in designing high-speed and fault-tolerance applications. The fundamental idea of the RNS is based on uniquely representing large binary numbers using a set of smaller residues, which results in carry-free, high-speed and parallel arithmetic. This system is based on modulus operation, where the divider is called modulo and the remainder of the division operation is called residue. This fact encourages the implementation of RNS in some applications where intensive processing is inevitable.

The principal aspect that distinguishes the RNS from other number systems is that the standard arithmetic operations; addition, subtraction and multiplication are easily implemented, whereas operations such as division, root, comparison, scaling and overflow and sign detection are much more difficult. Therefore, the RNS is extremely useful in applications that require a large number of addition and multiplication, and a minimum number of comparisons, divisions and scaling. In other words, the RNS is preferable in applications in which additions and multiplications are critical. Such applications are cryptography, Digital Signal Processing, image processing, speech processing and transforms. In the last decades, we have witnessed an ongoing increase in integrated circuit performance mainly due to advances in fabrication technology and improvements in computational paradigms.

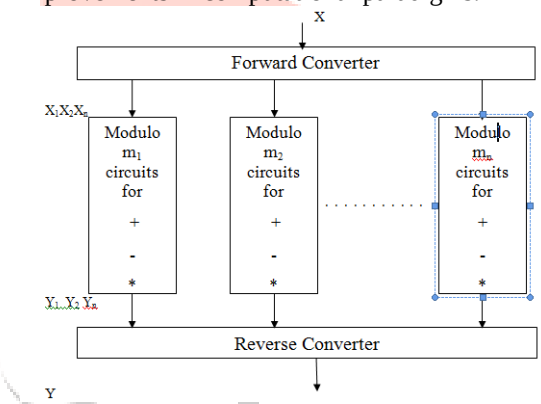

Figure 1: Block diagram of a typical RNS system

The major challenge in improving performance from the computational paradigm point of view is the reduction/elimination of the carry propagation chains inherent to Weighted Number Systems (WNS), e.g., binary number systems, decimal number systems. While this is an intrinsic performance limiter for arithmetic units and processors built based on WNS, several attempts have been made to overcome the speed limitations by following two main research avenues as follows: The carry propagation through the conventional ripple-carry adders, which is the main contributor to the addition delay, can be accelerated by using fast addition techniques. Those make use of specialized circuitry able to desterilize the carries calculation via methods like carry look ahead, carry-skip, prefix calculation, anticipated calculation, etc. These fast addition techniques are very important in improving arithmetic units performance because other arithmetic operations such as multiplication and division are based on addition, thus their delay heavily depends on the addition delay.

For non redundant number systems, e.g., traditional binary and decimal number systems, the delay of such fast

adders is logarithmically bounded by the number of operand digits. Thus far, most of the RNS related research has been done in the utilization of RNS in Digital Signal Processing (DSP) applications, e.g., Digital Filtering, Convolutions, Correlations, Discrete Cosine Transform (DCT), Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT). Additionally, RNS has also been applied in low power design, number theory, and digital communications. Despite all these desirable RNS features, it has not found a widespread usage in general purpose processors as the following RNS challenges must be properly addressed in order to be able to design RNS based general purpose architectures: sign detection, magnitude comparison, overflow detection, moduli selection, residue to binary/decimal conversion and vice-versa, division, and other complex arithmetic operations. Effective data converters are required in order to efficiently implement the difficult RNS operations, e.g., magnitude comparison, sign detection, and division, and also to build fault tolerant RNS architectures.

Thus, for general purpose RNS processors to become a reality, high-speed data converters are required. Due to these reasons, in this thesis, we propose efficient conversion techniques stemming from either the Mixed Radix Conversion (MRC) or the Chinese Remainder Theorem (CRT).

II. LITERATURE SURVEY

There have been a growing number of applications demanding high through put to execute billions of repetitive arithmetic operations per second. The most notable examples are inner products computations typical for various digital signal processing (DSP) algorithms like digital convolution, filtering, discrete Fourier transform (DFT), discrete cosine transform (DCT), and discrete wavelet transform (DWT).

The throughput of a digital system can be increased by using various approaches which can be used simultaneously, like: increasing clock frequency, implementation of less complex algorithms, parallelization of computations through the use of multiple processors or low level pipelining, adaptation of data representation to a computational problem, etc. In the latter case, selecting a suitable number system can directly decrease:

- The number of operations,
- The length of operands,
- The activity of data, and
- The number and/or length of global connections,

This can result in reduced area, delay, latency, and power dissipation. One of the most promising and still largely underestimated examples of the latter case is a non-positional residue number system (RNS).

III. PROPOSED SYSTEM

The RNS based system contains three major blocks such as Forward converter, RNS processer and Reverse converter. Forward converter is used to convert weighted – binary number to Residue number. It is done with simple circuitry and look-up tables (LUT) or ROMs. This process is simple and fast. RNS processer performs the required operations such as addition, subtraction and multiplication on the given residue numbers and it gives it to the reverse converter, it is also simple and fast. Reverse converter is used to convert Residue number to weighted-binary conversion. The Residue Number System performance mainly depends on the reverse conversion process and the selection of proper moduli set.

The reverse converter has more complexity. If the reverse converter design is efficient then the RNS is efficient and increase the speed. For reverse conversion two algorithms are available namely Chinese Remainder Theorem (CRT) and Mixed Radix Conversion (MRC). The CRT is desirable because the data conversion can be parallelized and it requires large modulus adders operation in parallel manner. The MRC is sequential process by its nature and it has less complex circuitry and slow modulo-M-operation, for different radixes. The dynamic range, the speed and the hardware implementation of the RNS systems depend on the form and the number of moduli chosen. There are three, four and five moduli sets, each moduli sets have their own advantage and disadvantage.

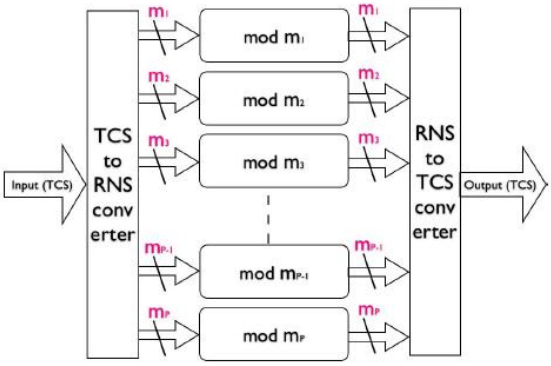

Figure 2: Structure of RNS processor

The figure 2 shows the basic RNS processor. Due to the absence of any carry propagation among the different modular processors, the architecture implementation is very efficient. The propagation on the whole word length is only present in the input and output converters.

The modulo M adder can be realized using ROMs, pure combinational logic, or a combination of both. When the dynamic range is large, the speed and the complexity of the multi-operand modulo M adder becomes the bottleneck of the design of the of the R/B converter. Most of the available CRT based R/B converters have the general high-level block diagram shown in Figure 3.

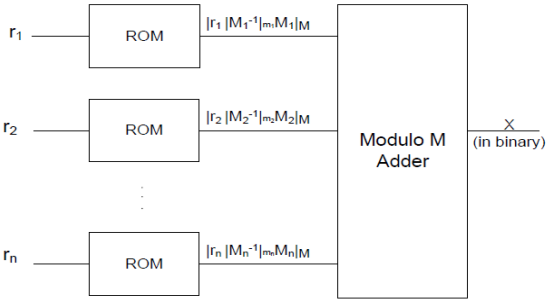

Figure 3: CRT based R/B converter

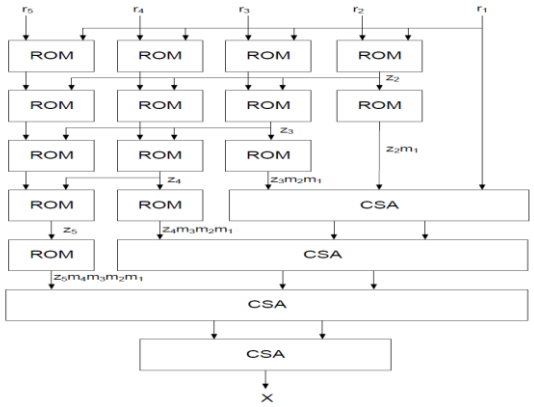

Figure 4: MRC based R/B converter

The possible implementation of MRC based reverse converter block diagram as shown in figure 4. Here two types of ROMS are used. The sum addressable ROMs are used to generate the product of differences and the inverses. The ordinary ROMs are used to generate the product of the moduli. The summation equation is implemented using carry save adders(CSA).

1) Three Moduli Set

Most of the available high performance reverse converter architectures are based on the three moduli set $\{2^n\text{-}1,2^n, 2^n\text{+}1\}$. It is the most famous and well known moduli set because of its simple arithmetic calculations. However, this set has modulo $(2^n\text{+}1)$ channel that represents the bottleneck of the system. Its arithmetic circuits suffer from the longest delay among all three channels. In general arithmetic circuits modulo $(2^n\text{-}1)$ are more efficient than those modulo $(2^n\text{+}1)$, it is better to reduce the number of moduli of the form $(2^n\text{+}1)$. The complexity caused by modulo $(2^n\text{+}1)$ in the set $\{2^n\text{-}1,2^n, 2^n\text{+}1\}$, can be simplified by replacing the new modulo $(2^{n\pm1}\text{-}1)$ of the form $(2^n\text{-}1)$ in new moduli sets $\{2^{n\text{-}1}\text{-}1,2^n\text{-}1,2^n\}$ and $\{2^n\text{-}1,2^n,2^{n+1}\text{-}1\}$. If we add one or two more modulus to the three moduli set, then the closed form multiplicative inverses become difficult and cannot be implemented with simple hardware as in the case of three moduli set.

These three moduli sets have a 3n-bit dynamic range(DR), which is sufficient for applications that require medium dynamic ranges. This RNS offers the (3n-1) bit dynamic range (DR) with 3-bit resolution. For example the maximal dynamic ranges available for n=6,7, and 8 are respectively 17,20, and 23 bits. Clearly, its drawback is that should the 18-bit range be needed, a designer must use a moduli set with the closest sufficiently large n, i.e., n=7, although its 20-bit dynamic range is unnecessarily large, thus requiring the use of too large residue data paths. Not less important selection criterion than efficiency of separate arithmetic blocks for individual moduli is that they should guaranteeing exactly a given dynamic range, the most advantageous sets of moduli are those for which the delays and areas of all residue data paths are as much close as possible. It is well known that the arithmetic operations mod 2n are significantly less complex and slightly faster than their mod $2^n\text{-}1$ (mod $2^n\text{+}1$) counterparts: the carry out signal mod 2^n is simply ignored, whereas the carry out signal mod 2^n is simply ignored, whereas the carry out signal mod $2^n\text{-}1$(mod $2^n\text{+}1$) appears as the end-around carry (EAC). Clearly, a more balanced performance could be achieved by using a larger even modulus 2k with k>n. The need for balancing of the residue data paths and 1-bit dynamic range resolution were at the origin of introduction of the special 3-moduli set $\{2^n\text{-}1, 2^k, 2^n\text{+}1\}$ with flexible even modulus 2^k whose size is independent on n, proposed in along with the reverse converter for $n\leq k\leq 2n$.However, it is not suitable for applications (DSP) which require larger dynamic range and more parallelism. Therefore, new moduli sets $\{2^n\text{–}\ 1,\ 2^n,\ 2^{2n+1}\text{–}\ 1\}$ and $\{2^n\text{–}\ 1,\ 2^n\text{+}\ 1,\ 2^{2n}\text{+}\ 1\}$ that provide 4n-bit DR and $\{2^n,\ 2^{2n}\text{–}\ 1,\ 2^{2n}\text{+}\ 1\}$that provides 5n-bit DR, were suggested. Although the dynamic range is larger, the delay of the residue arithmetic units based on these sets has considerably increased, due to utilizing moduli with greater magnitudes. In order to eliminate this drawback and maintain the large dynamic range, four and five moduli sets have been suggested.

2) Four Moduli Set

The four moduli set has high dynamic range than the three moduli set and eliminates the drawback present in the three moduli set. Such four moduli sets are $\{2^n\text{–}1,\ 2^n,\ 2^n\text{+}\ 1,\ 2^{n+1}\text{–}1\}$, $\{2^n\text{–}\ 1,\ 2^n,\ 2^n\text{+}\ 1,\ 2^{n+1}\text{+}\ 1\}$, $\{2^n\text{–}\ 1,\ 2^n,\ 2^n\text{+}\ 1,\ 2^{2n}\text{+}\ 1\}$, $\{2^n\text{–}\ 1,\ 2^n,\ 2^n\text{+}\ 1,\ 2^{2n+1}\text{–}1\}$, $\{2^n\text{–}\ 1,\ 2^n,\ 2^n\ \text{+}\ 1,\ 2^n\text{–}\ 2^{(n+1)/2}\ \text{+}\ 1,\ 2^n\text{+}\ 2^{(n+1)/2}\ \text{+}\ 1\}$, $\{2^n\text{–}\ 1,\ 2^n\text{+}\ 1,\ 2^{2n}\text{–}2,\ 2^{2n+1}\text{–}3\}$, $\{2^n\text{–}1,\ 2^{2n},\ 2^n\text{+}\ 1,2^{2n}\text{+}\ 1\}$, $\{2^n\text{–}\ 1,\ 2^n,\ 2^n\text{+}\ 1,\ 2^{n-1}\text{–}\ 1,\ 2^{n+1}\ \text{+}\ 1\}$ and$\{2^n,\ 2^{n/2}\ \text{–}1,\ 2^{n/2}\ \text{+}1,\ 2^n\text{+}1,\ 2^{2n-1}\text{–}\ 1\}$. Each of these sets has its own advantages and disadvantages. Some of them offer higher dynamic range than others, while others have more parallelism. Some can result in more efficient RCs, while others in more efficient RAUs. The 4n-bit dynamic range four moduli set minimizes the dynamic range, and has asymmetric moduli channel length and long conversion delay.

3) Five Moduli Set

To increase the dynamic range the five moduli set were introduced. The five moduli set have high dynamic range than the three and four moduli sets and eliminates the drawbacks. A five moduli set $\{2^n\text{-}1,2^n,2^n\text{+}1,2^n\text{+}2^{(n+1)/2}\text{+}1,2^n\text{-}2^{(n+1)/2}\text{+}1\}$ and $\{2^{3n},\ 2^{3n}\text{-}1,\ 2^{3n}\text{+}1,\ 2^{3n}\text{-}2^{(3n+1)/2}\text{+}1,\ 2^{3n}\text{+}2^{(3n+1)/2}\text{+}1\}$is proposed, but here the new two moduli are not in the form of 2^n or $2^n\pm1$. This makes it hard to design efficient architectures of VLSI. Another five moduli set which is $\{2^{n+1},\ 2^n\text{-}1,\ 2^n\text{+}1,\ 2^{n+1}\text{-}1,\ 2^{n+1}\text{+}1\}$, where all the moduli are in the form of 2^n or $2^n\pm1$. Therefore, it has more efficient residue arithmetic unit , but the disadvantage is that the moduli set is not co-prime for any value of n, which reduces the dynamic range and also makes the residue – to-binary conversion algorithm more difficult.

The operations modulo $2^n\text{-}1$ are more efficient than those for modulo $2^n\text{+}1$, therefore it is better to minimize the number of moduli having the form of $2^n\text{+}1$. In this project, we propose a new five moduli superset $\{2^n\text{-}1,\ 2^n,\ 2^n\text{+}1,\ 2^{n+1}\text{-}1,\ 2^{n-1}\text{-}1\}$, for evenvalues of n. The forward and reverse converter and the modular operations for this moduli set is more efficient, as the moduli are in the form of 2^n or $2^n\pm1$. There is only one modulus in the form of $2^n\text{+}1$.It has high dynamic range that can represent up to 5n-1 bits while keeping the moduli small enough and converter efficient.

IV. SIMULATION RESULTS

Simulation is the process of verifying the functionality of the design at any level of abstraction. We use Xilinx ISE simulator to simulate the Hardware models. To test ifthe RTL codemeets the functional requirements of the specification and the RTL blocks are functionally correct, we need to write test bench, which generates test vectors. Here we use the Verilog HDL as the hardware description language

A. MRC-Simulation Results

For the design of 3 moduli set reverse converter using Mixed Radix Conversion Theorem, the Verilog HDL code is written, compiled and simulated. In this design for the moduli set $\{2^{n-1},2^n, 2^{n+1}\}$inputs n and residue set-$\{x_1,x_2,x_3\}$ are applied and the reverse converted result isobtained as shown in Figure 5.

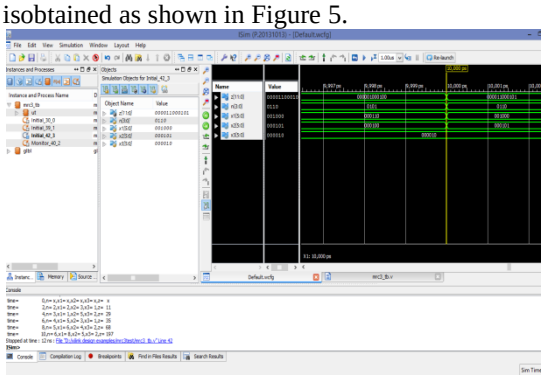

Figure 5: Simulation results for 3 moduli set RNS reverse converter using MRC

For 3 moduli set reverse converter using MRC the inputs n and residue set are taken as
n=2 moduli set = $\{2^{n-1},2^n,2^{n+1}\}$ = {3, 4, 5}
residue set $\{x_1, x_2, x_3\}$={2, 3, 1}
The obtained result is Z=11.

For the design of 4 moduli set reverse converter using Mixed Radix Conversion Theorem, the Verilog HDL code is written,compiled and simulated. In this design for the moduli set $\{2^{n-1}+1,2^{n-1},2^n,2^{n+1}\}$inputs n and residue set-$\{x_1, x_2, x_3,x_4\}$ are applied and the reverse converted result is obtained as shown in Figure 6.

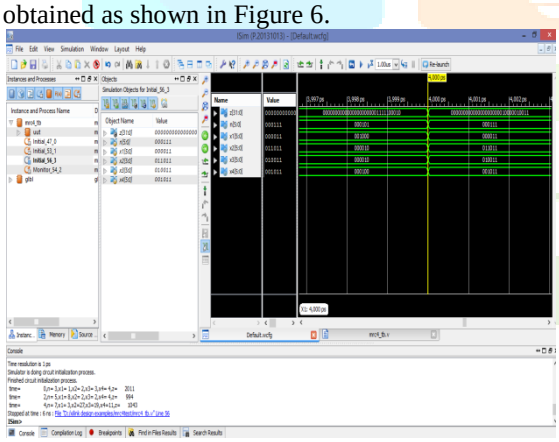

Figure 6: Simulation results for 4 moduli set RNS reverse converter using MRC

For 4 moduli set reverse converter using MRC the inputs N and residue set are taken as
n=3 moduli set = $\{2^{n-1}+1, 2^{n-1},2^n,2^{n+1}\}$ = {5, 7, 8, 9}
residue set$\{x_1, x_2, x_3,x_4\}$= {1, 2, 3, 4}
The obtained result is Z=2011.

For the design of 5 moduli set reverse converter using Mixed Radix Conversion Theorem, the Verilog HDL code is written,compiled and simulated. In this design for the moduli set $\{2^n\text{-}1, 2^n, 2^n\text{+}1, 2^{n+1}\text{-}1, 2^{n-1}\text{-}1\}$ inputs n and residue set-$\{x_1, x_2, x_3,x_4, x_5\}$ are applied and the reverse converted result is obtained as shown in Figure 7.

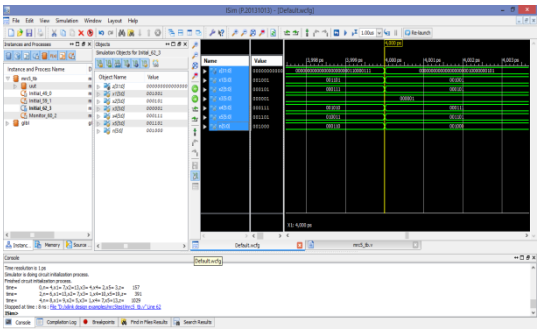

Figure 7: Simulation results for 5 moduli set RNS reverse converter using MRC

For 5 moduli set reverse converter using MRC the inputs N and residue set are taken as
n=4 moduli set = $\{2^n\text{-}1, 2^n, 2^n\text{+}1, 2^{n+1}\text{-}1, 2^{n-1}\text{-}1\}$ = {15, 16, 17, 31, 7}
residue set $\{x_1, x_2, x_3,x_4, x_5\}$= {7, 13, 4, 2, 3}
The obtained result is Z=157.

B. CRT-Simulation Results

For the design of 3 moduli set reverse converter using Chinese Remainder Theorem, the Verilog HDL code is written,compiled and simulated. In this design for the moduli set $\{2^{n-1},2^n,2^{n+1}\}$inputs n and residue set-$\{x_1, x_2, x_3\}$ are applied and the reverse converted result isobtained as shown in Figure 8.
For 3 moduli set reverse converter using CRT the inputs n and residue set are taken as
n=2 moduli set = $\{2^{n-1},2^n,2^{n+1}\}$ = {3, 4, 5}
residue set $\{x_1, x_2, x_3\}$= {2, 3, 1}
The obtained result is Z=11.

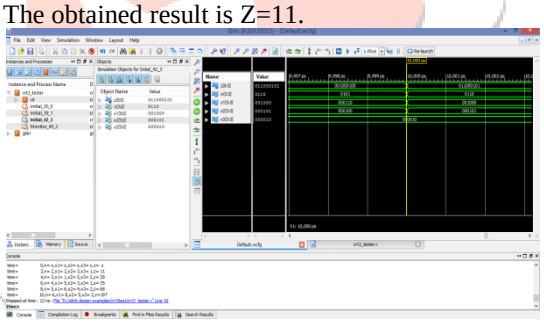

Figure 8: Simulation results for 3 moduli set RNS reverse converter using CRT

For the design of 4 moduli set reverse converter using Chinese remainder Theorem, the Verilog HDL code is written,compiled and simulated. In this design for the moduli set $\{2^{n-1}+1,2^{n-1},2^n,2^{n+1}\}$inputs n and residue set-$\{x_1, x_2, x_3,x_4\}$ are applied and the reverse converted result is obtained as shown in Figure 9.

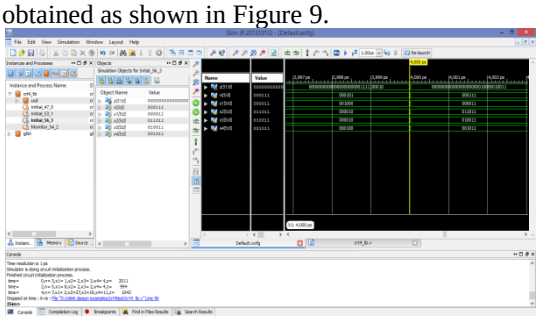

Figure 9: Simulation results for 4 moduli set RNS reverse converter using CRT

For 4 moduli set reverse converter using CRT the inputs N and residue set are taken as

n=3 moduli set = $\{2^{n-1}+1, 2^{n-1}, 2^n, 2^{n+1}\}$ = {5, 7, 8, 9}
residue set $\{x_1, x_2, x_3, x_4\}$= {1, 2, 3, 4}
The obtained result is Z=2011.

For the design of 5 moduli set reverse converter using Chinese Remainder Theorem, the Verilog HDL code is written,compiled and simulated. In this design for the moduli set $\{2^n-1, 2^n, 2^n+1, 2^{n+1}-1, 2^{n-1}-1\}$ inputs n and residue set-$\{x_1, x_2, x_3, x_4, x_5\}$ are applied and the reverse converted result is obtained as shown in Figure 10.

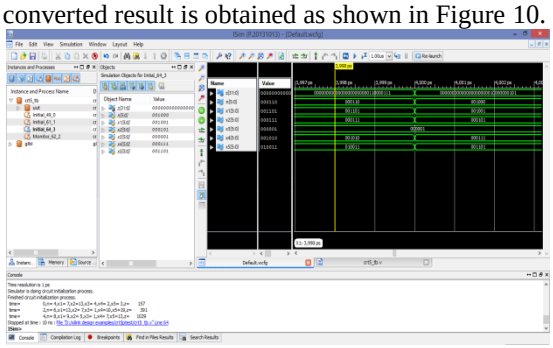

Figure 10: Simulation results for 5 moduli set RNS reverse converter using CRT

For 5 moduli set reverse converter using CRT the inputs N and residue set are taken as

n=4 moduli set = $\{2^n-1, 2^n, 2^n+1, 2^{n+1}-1, 2^{n-1}-1\}$ = {15, 16, 17, 31, 7}
residue set $\{x_1, x_2, x_3, x_4, x_5\}$= {7, 13, 4, 2, 3}
The obtained result is Z=157.

C. RTL Schematics:

RTL means Register Transfer Level.RTL is a graphical representation of our design. The RTL schematic gives gate level architecture of a digital network. Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic. This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, counters, multipliers, OR gates and AND gates that are independent of the targeted Xilinx device.

The figure 11 shows the RTL schematic of the 3 moduli set reverse converter using Mixed Radix Conversion Theorem. The RTL schematic consists of adders, subtractors, multipliers, comparators, and gates.

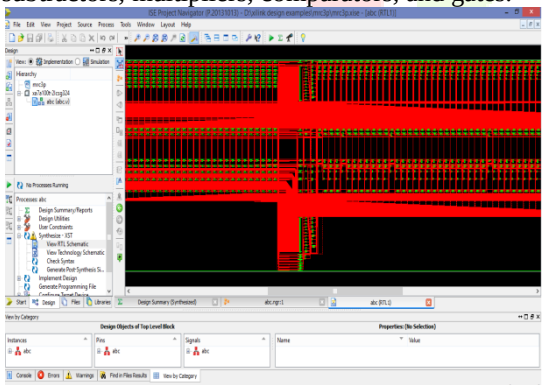

Figure 11: RTL Schematic for 3 moduli set RNS reverse converter using MRC

The figure 12 shows the RTL schematic of the 4 moduli set reverse converter using Mixed Radix Conversion Theorem. The RTL schematic consists of adders, subtractors, multipliers, comparators, and gates.

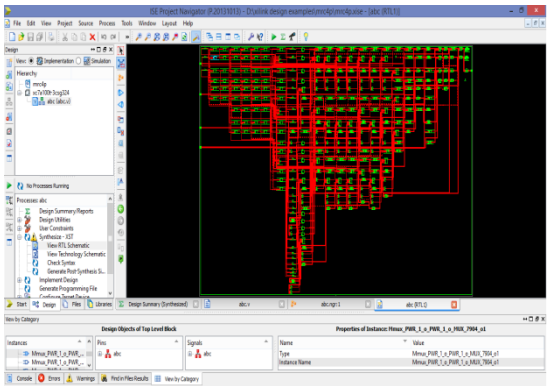

Figure 12: RTL Schematic for 4 moduli set RNS reverse converter using MRC

The figure 13 shows the RTL schematic of the 5 moduli set reverse converter using Mixed Radix Conversion Theorem. The RTL schematic consists of adders, subtractors, multipliers, comparators, and gates.

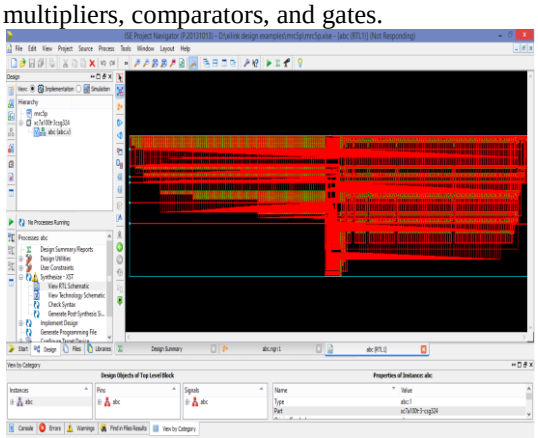

Figure 13: RTL Schematic for 5 moduli set RNS reverse converter using MRC

The figure 14 shows the RTL schematic of the 3 moduli set reverse converter using Chinese Remainder Theorem.The RTL schematic consists of adders, subtractors, multipliers, comparators, and gates.

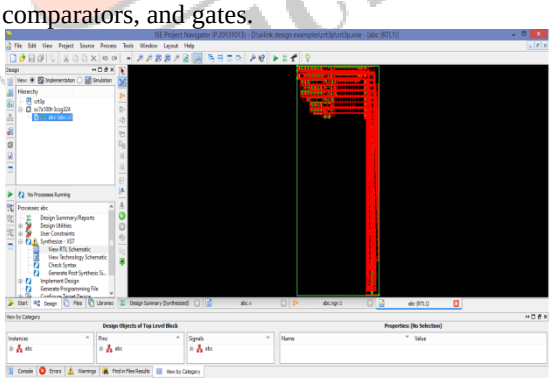

Figure 14: RTL Schematic for 3 moduli set RNS reverse converter using CRT

The figure 15 shows the RTL schematic of the 4 moduli set reverse converter using Chinese Remainder Theorem.The RTL schematic consists of adders, subtractors, multipliers, comparators, and gates.

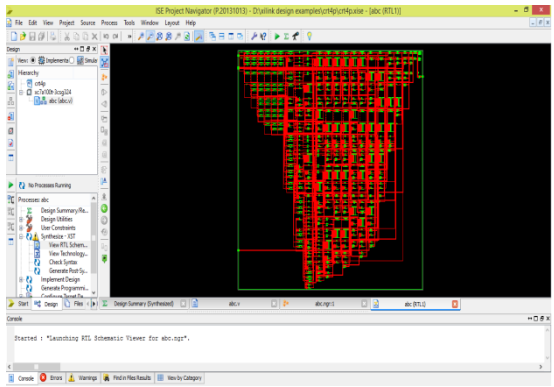

Figure 15: RTL Schematic for 4 moduli set RNS reverse converter using CRT

The figure 16 shows the RTL schematic of the 5 moduli set reverse converter using Chinese Remainder Theorem.The RTL schematic consists of adders, subtractors, multipliers, comparators, and gates.

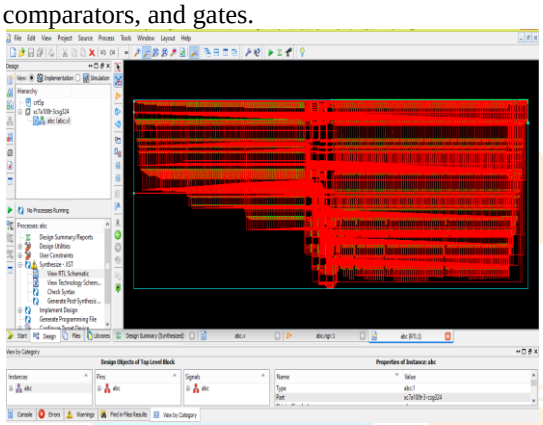

Figure 16: RTL Schematic for 5 moduli set RNS reverse converter using CRT

D. Synthesis Reports:

Synthesis report gives the design summary of the project in terms of device utilization summary (number of LUTs, number of slice registers, and number of IOBs), primitive and black box usage, HDL and advanced HDL synthesis report, the memory usage, and timing summary. The device utilization summary gives the details about number of registers, LUTs and IOBs used and percentage of device utilization. The timing summary gives maximum combination path delay, XST computation time etc. The HDL and advanced HDL synthesis report gives number of adders, subtractors, multipliers, comparators and shift registers, flip-flops used in the design.

The figure 17 shows the synthesis report of the 3 moduli set reverse converter using Mixed Radix Conversion Theorem. Here the inputs are n and x_1, x_2, x_3 and the output is z. Here the number slice registers is 14 and the number of bonded IOBs is 36 and the maximum combination path delay is 185.65ns.

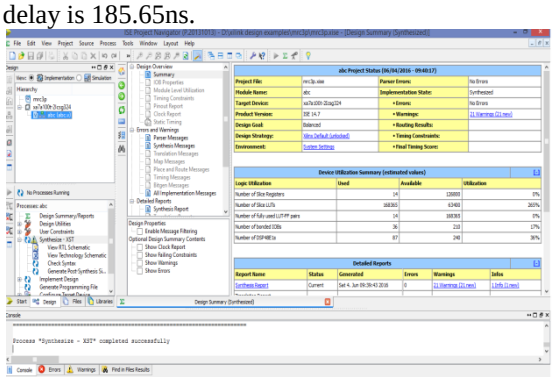

Figure 17: Synthesis report of 3 moduli set RNS reverse converter using MRC

The figure 18 shows the synthesis report of the 4 moduli set reverse converter using Mixed Radix Conversion Theorem. Here the inputs are n and x_1, x_2, x_3, x_4 and the output is z. Here the number slice registers is 12 and the number of bonded IOBs is 42 and the maximum combination path delay is 223.21ns.

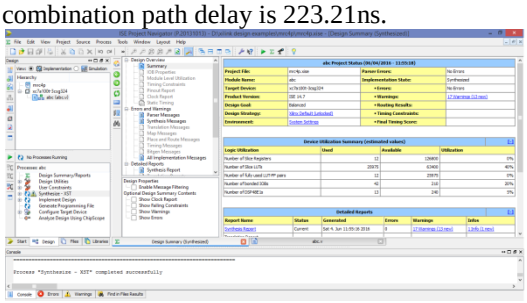

Figure 18: Synthesis report of 4 moduli set RNS reverse converter using MRC

The figure 19 shows the synthesis report of the 5 moduli set reverse converter using Mixed Radix Conversion Theorem. Here the inputs are n and x_1, x_2, x_3, x_4, x_5 and the output is z. Here the number slice registers is 28 and the number of bonded IOBs is 92 and the maximum combination path delay is 638.60ns.

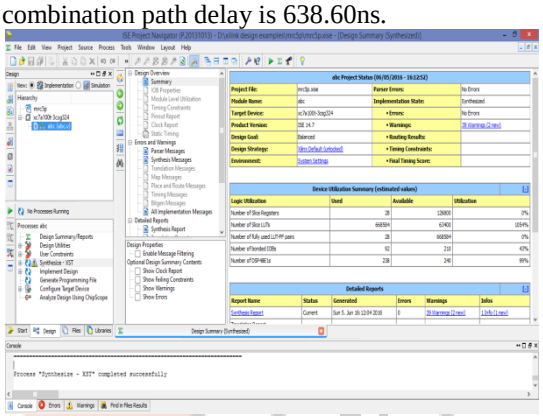

Figure 19: Synthesis report of 5 moduli set RNS reverse converter using MRC

The figure 20 shows the synthesis report of the 3 moduli set reverse converter using Chinese Remainder Theorem. Here the inputs are n and x_1, x_2, x_3 and the output is z. Here the number slice registers is 12 and the number of bonded IOBs is 54 and the maximum combination path delay is 171.12ns.

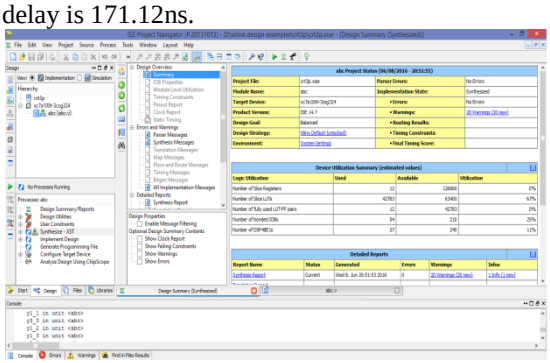

Figure 20: Synthesis report of 3 moduli set RNS reverse converter using CRT

The figure 21 shows the synthesis report of the 4 moduli set reverse converter using Chinese Remainder Theorem. Here the inputs are n and x_1, x_2, x_3, x_4 and the output is z. Here the number slice registers is 16 and the number of bonded IOBs is 67 and the maximum combination path delay is 175.59ns.

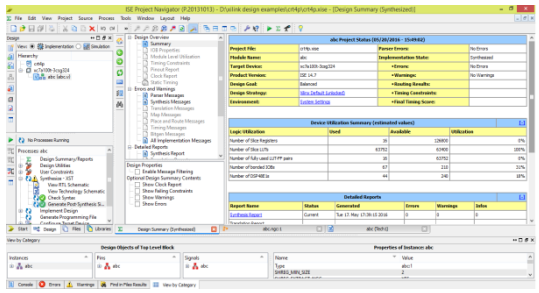

Figure 21: Synthesis report of 4 moduli set RNS reverse converter using CRT

The figure 22 shows the synthesis report of the 5 moduli set reverse converter using Chinese Remainder Theorem. Here the inputs are n and x_1, x_2, x_3, x_4, x_5 and the output is z. Here the number slice registers is 35 and the number of bonded IOBs is 92 and the maximum combination path delay is 186.71ns.

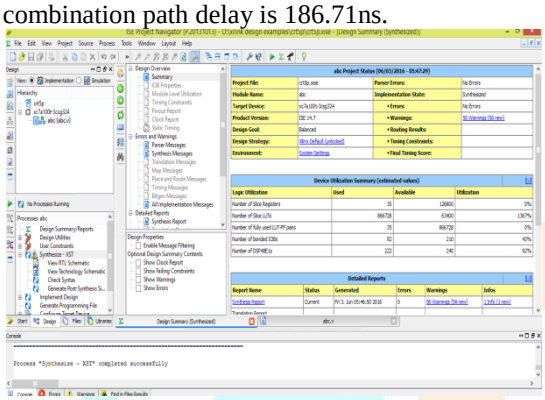

Figure 22: Synthesis report of 5 moduli set RNS reverse converter using CRT

V. CONCLUSION

This work aims to build an efficient Reverse converter for residue number system, with high dynamic range to increases speed and more parallelism .In this project we proposed a five moduli set{2^n-1, 2^n, 2^n+1, 2^{n+1}-1, 2^{n-1}-1} for even values of n. The reverse converter designed using Chinese remainder theorem. It has higher dynamic range (up to 5n-1 bits), higher parallelism and the forward and reverse conversion and residue arithmetic units simple. As compared to other existing converter designs the reverse converter design for five moduli set using Chinese remainder theorem has high dynamic range, high speed, and more parallelism and reduces the complexity.

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