Comparison of Static and Dynamic Carry Look Ahead Adders

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Abstract: Power consumption and delay are the two most important parameters that has to be considered in the design of today's VLSI based electronic devices. In this paper the performance of 4-bit static carry look ahead adder is compared with 4-bit dynamic carry look ahead adder. The speed performance of the ripple carry 4-bit adder is significantly improved by using static and dynamic carry look ahead adders. The circuit is simulated in TSPICE in the high performance 2 µm CMOS technology with a supply voltage of VDD=5V.

IndexTerms - **Pass transistor, Carry look ahead adders, Inverter, PUN, PDN.**
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I. INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

Although adders can be constructed for many number representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor.

II. RIPPLE CARRY ADDER

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that Cin = 0).

The layout of a ripple-carry adder is simple, which allows fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 32-bit ripple-carry adder, there are 32 full adders, so the critical path (worst case) delay is 3 (from input to carry in first adder) + 31*2 (for carry propagation in latter adders) = 65 gate delays.
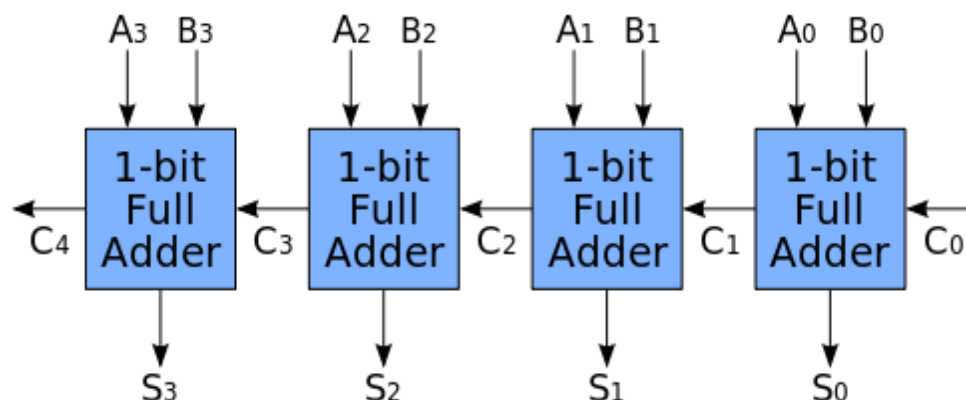

Fig.1 Ripple Carry Adder

III. CARRY LOOK AHEAD ADDER

A carry-look ahead adder (CLA) or fast adder is a type of adder used in digital logic. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits.

It can be contrasted with the simpler, but usually slower, ripple carry adder, for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry bit have been calculated to begin calculating its own result and carry bits (see adder for detail on ripple carry adders). The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger-value bits of the adder. It examines all the input bits simultaneously and also generates the carry in bits for all the stages simultaneously.
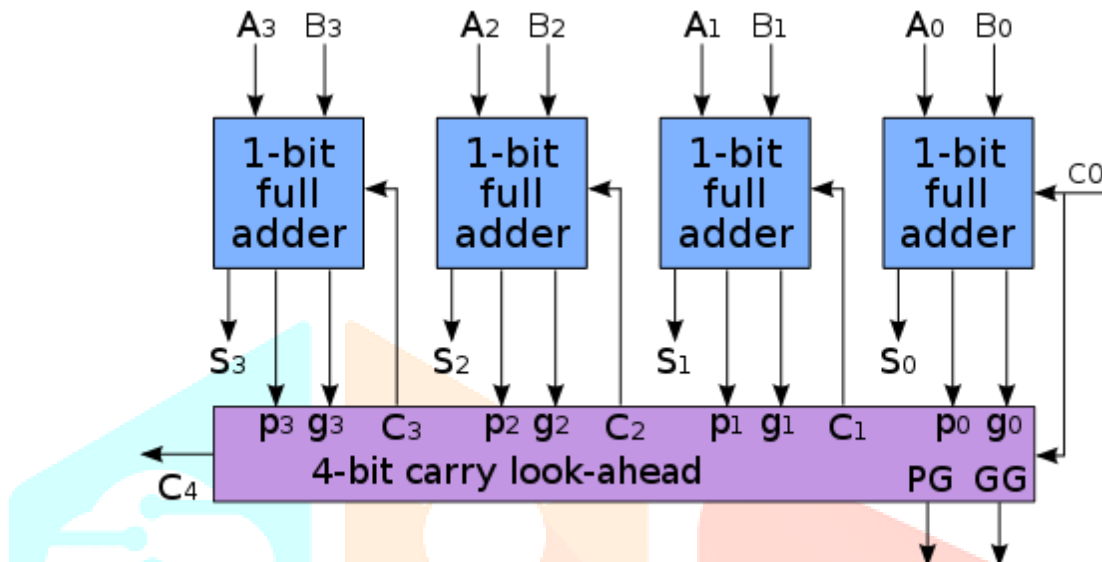
Fig.2 Carry Look-Ahead Adder

In the case of binary addition, ${\displaystyle A\cdot B}$A.B generates if and only if both A and B are 1. If we write ${\displaystyle G(A,B)}$G(A,B) to represent the binary predicate that is true if and only if ${\displaystyle A\cdot B}$A.B generates, we have

$$G(A, B) = A . B$$

In the case of binary addition, $A+B{\displaystyle A+B}$ propagates if and only if at least one of A or B is 1. If we write P(A,B) ${\displaystyle P(A,B)}$ to represent the binary predicate that is true if and only if ${\displaystyle A+B}$A+B propagates, we have

$$P(A, B) = A + B$$

A + B is said to propagate if the addition will carry whenever there is an input carry, but will not carry if there is no input carry. Fortunately, due to the way generate and propagate bits are used by the carry look ahead logic, it doesn't matter which definition is used. In the case of binary addition, this definition is expressed by

$$P(A, B) = A \oplus B$$

In boolean algebra, with ${\displaystyle C_{i}}$Ci the carry bit of digit i, and ${\displaystyle P_{i}}$Pi and ${\displaystyle G_{i}}$Gi the propagate and generate bits of digit i respectively, and is expressed by

$$C_{i+1} = G_i + (P_i . C_i)$$

IV. STATIC CARRY LOOK AHEAD ADDER

The most widely used logic is complementary CMOS logic due to advantages associated with it like Low sensitivity to noise, Low power consumption with no static power dissipation, Good performance and Robustness. These properties lead to implementation of large fan in logic circuits using same devices. Static MOS circuits design includes complementary CMOS, ratioed logic (pseudo NMOS and DCVSL) and pass transistor logic.

Static CMOS gates are implemented by using combination of two networks, the pull up network (PUN) and pull down network (PDN).Static CMOS is characterized by very good current driving capabilities and high noise margins. In Static CMOS design, at every point in time, each gate output is connected to either Vdd or Vss via a low-resistance path. Also, the outputs of

the gate assume at all times the value of the Boolean function implemented by the circuit. A Static CMOS gate is a combination of two networks, the pull up network (PUN) and the pull down network (PDN). The function of the PDN is to provide a connection between the output and Vdd.

When the output of the logic gate is supposed to be 1. Similarly, the PDN connects the output to Vss when the output is expected to be 0. The PUN and PDN networks are constructed in a mutually exclusive manner such that one and only one of the networks are conducting in steady state. The Static CMOS gates have rail-to-rail swing, no static power dissipation. The speed of the static CMOS circuit depends on the transistor sizing and the various parasitic that are involved with it. The problem with this type of implementation is that for N fan-in gate 2N number of transistors are required, i.e., more area required to implement logic. This has an impact on the capacitance and thus the speed of the gate.
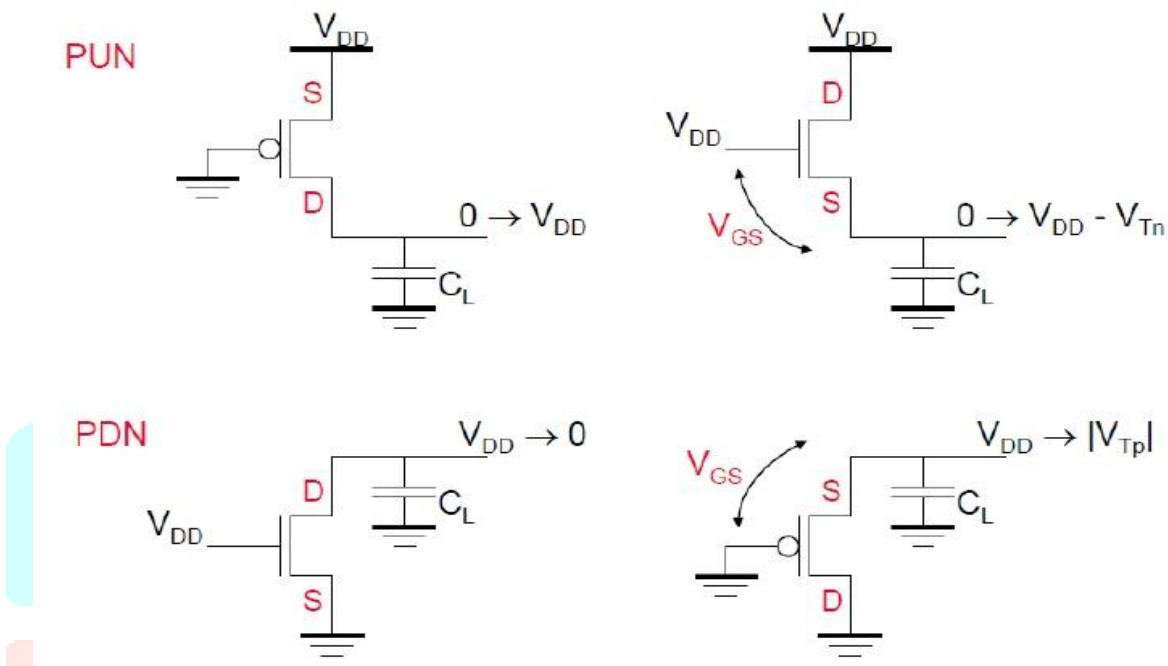
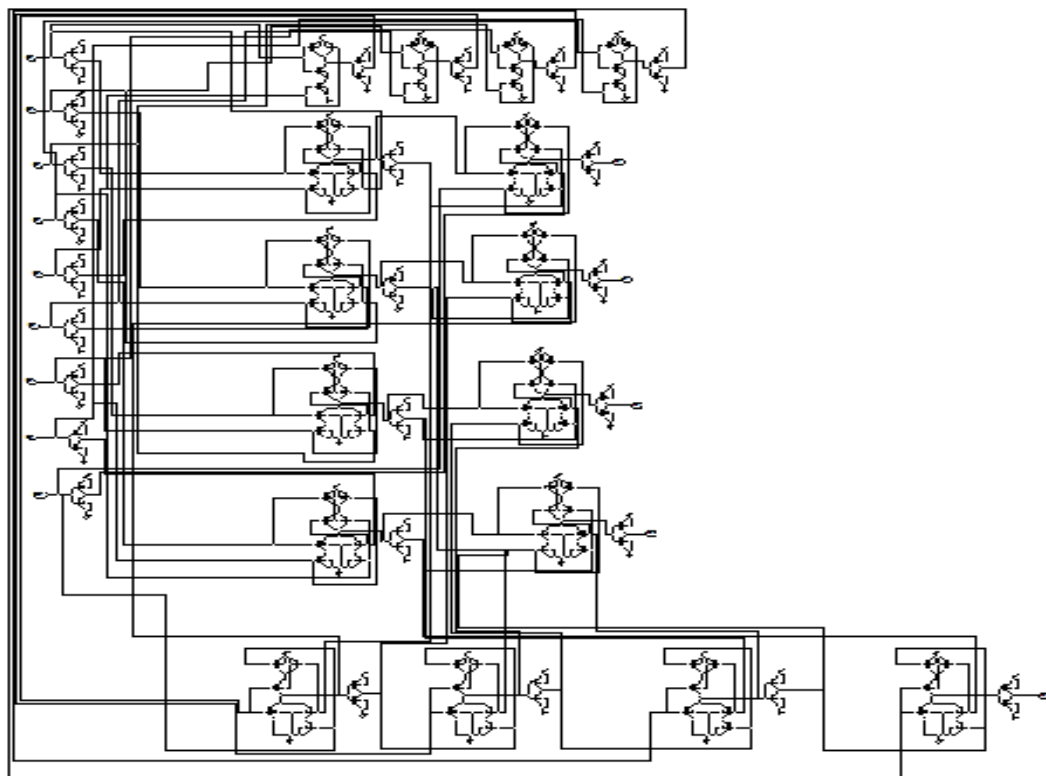Fig.3 Circuit diagram for PUN and PDN of static CMOS

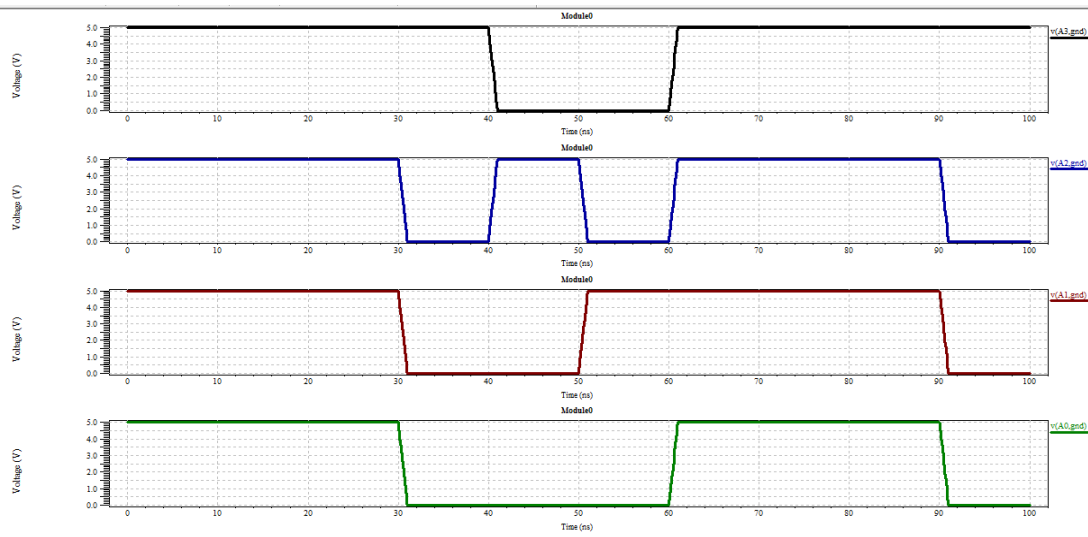Fig. 4 Circuit diagram for static carry look ahead adder

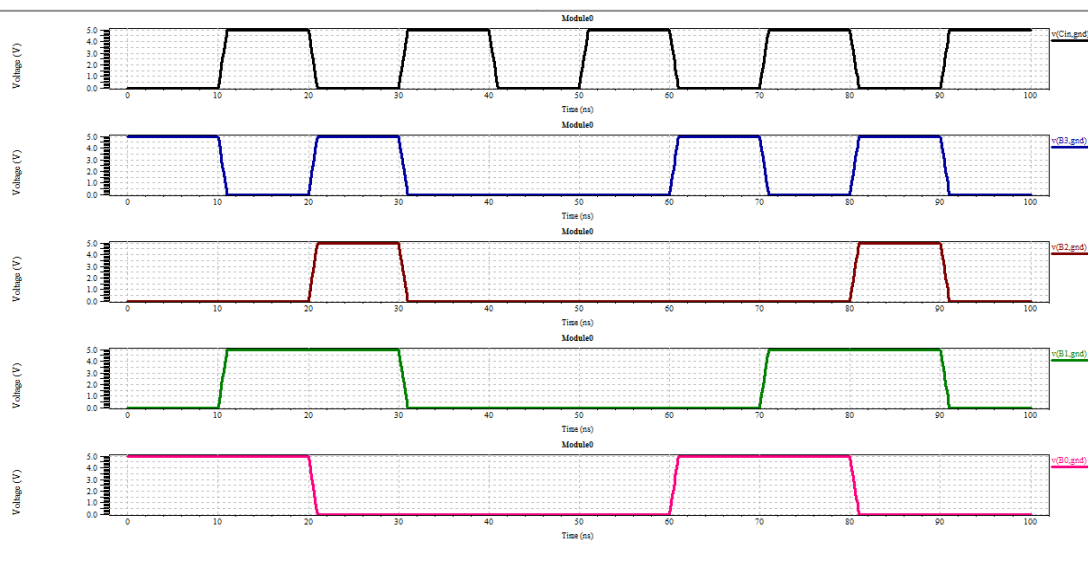Fig. 5 Input waveform for static carry look ahead adder

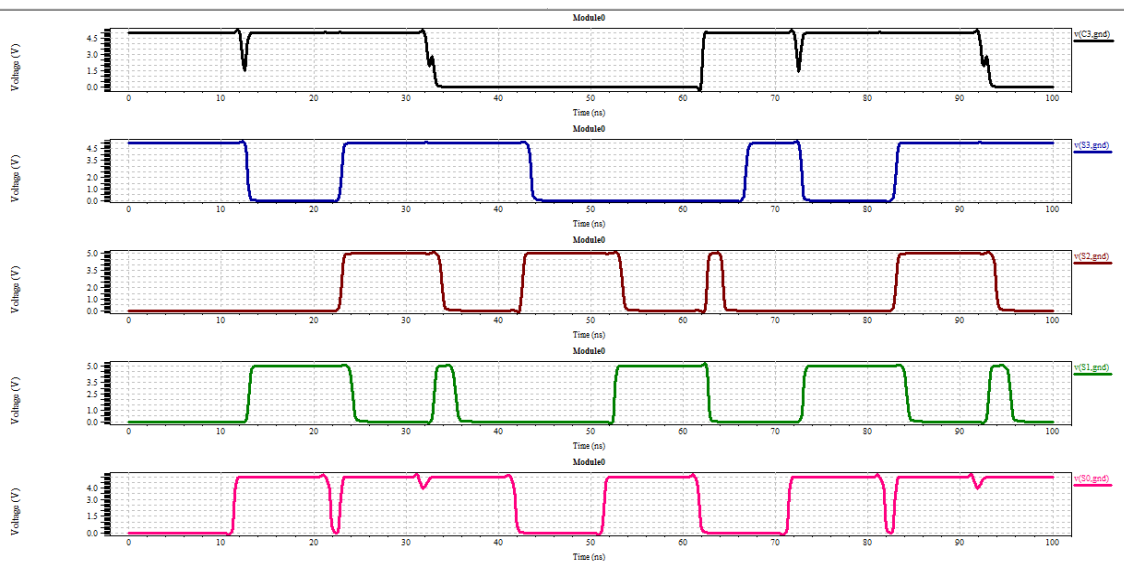Fig. 6 Input waveform for static carry look ahead adder

Fig. 7 Output waveform for static carry look ahead adder

V. DYNAMIC CARRY LOOK AHEAD ADDER

Dynamic logic on the other hand uses a sequence of precharge and conditional evaluation phases governed by the clock to realize complex logic functions. Both forms can be used. The operation of the pull-down network (PDN) can be divided into two major phases. The precharge and the evaluation phase. In what mode the circuit is operating is determined by the signal φ, the "clock " signal. PUN and PDN are shown in fig
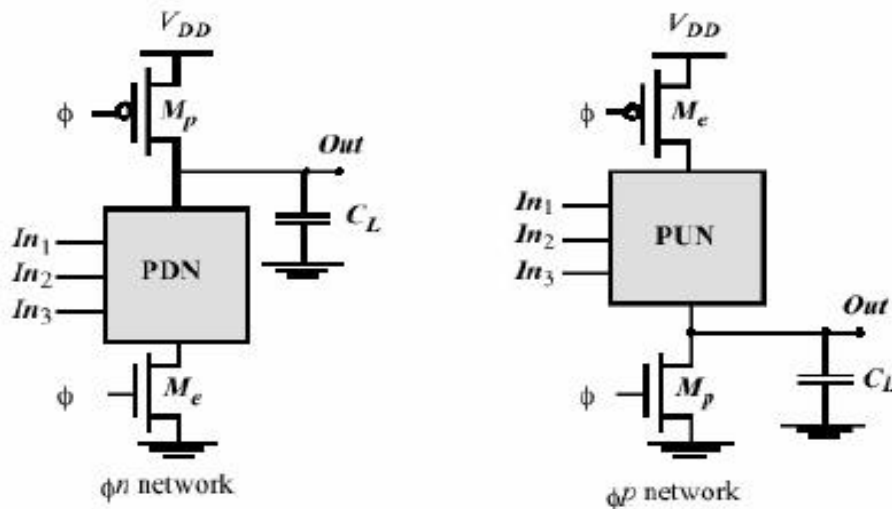

Fig. 8 Circuit diagram for PUN and PDN of dynamic CMOS

Precharge

When φ =0, the output node "OUT" is precharged to VDD by the PMOS transistor. During that time, the nmos evaluation transistor is off, so the nmos logic network is isolated from ground by a series of nmos transistors and hence no dc current flows regardless of the values of the input signal. Input signals can change with no effect to the output It is also difficult to control the change of variables during precharge.

Evaluation

When φ =1, the precharge pull up transistor is off, and the evaluation transistor is turned on. Depending on the values of the input and the composition of the PDN, a   conditional path between OUT and (through the nmos transistors) GND is created. If such a pathexits, OUT is discharged and a low output signal is obtained. If not, the precharge value remains stored on the output capacitor CL and a high output value is obtained during the evaluation phase.

Only path between the output node and a supply rail is to GND, consequently, once "OUT" is   discharged, it cannot be charged again. This is in contrast with the static circuit, where the output node is low-impedance under all possible circumstances. The inputs to the circuit can therefore make at most one transition during evaluation.
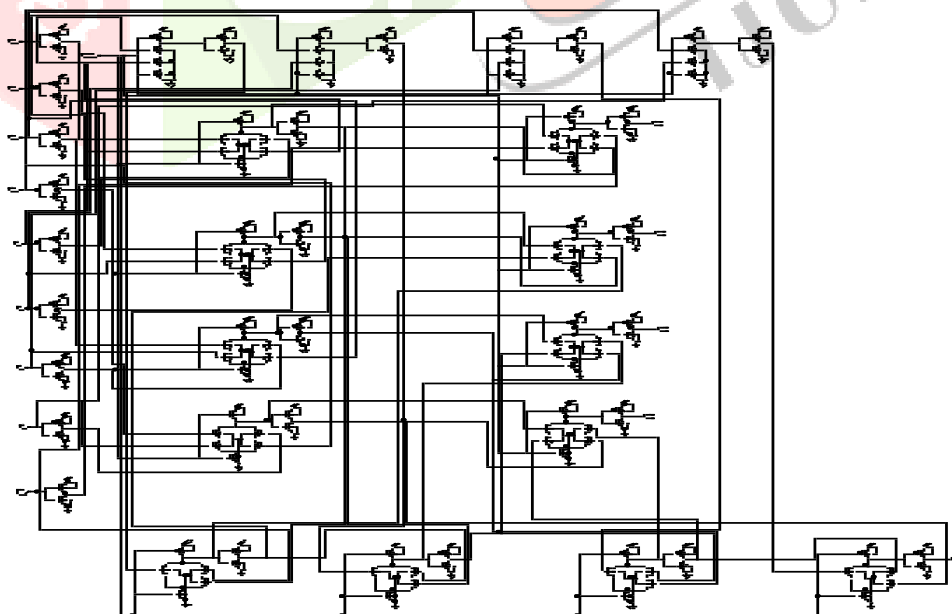

Fig. 9 Circuit diagram for dynamic carry look ahead adder
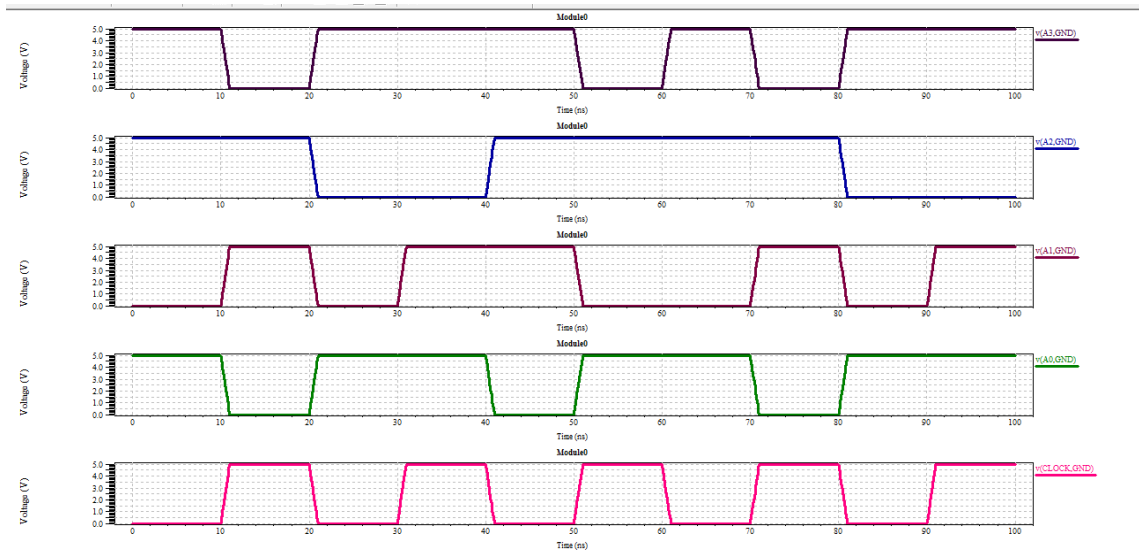
VI. RESULT AND OUTPUT

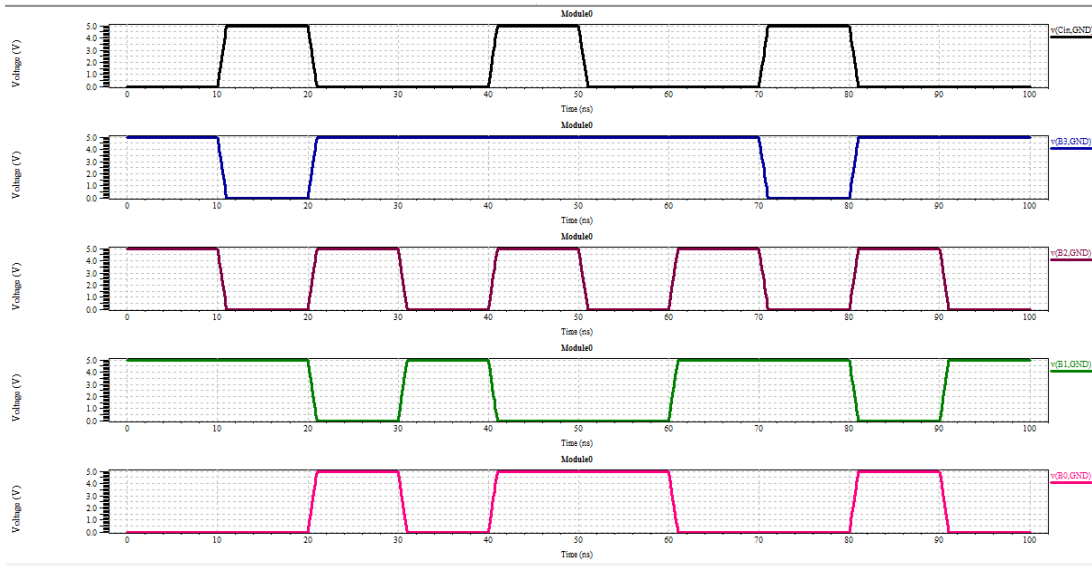Fig. 10 Input waveform for dynamic carry look ahead adder

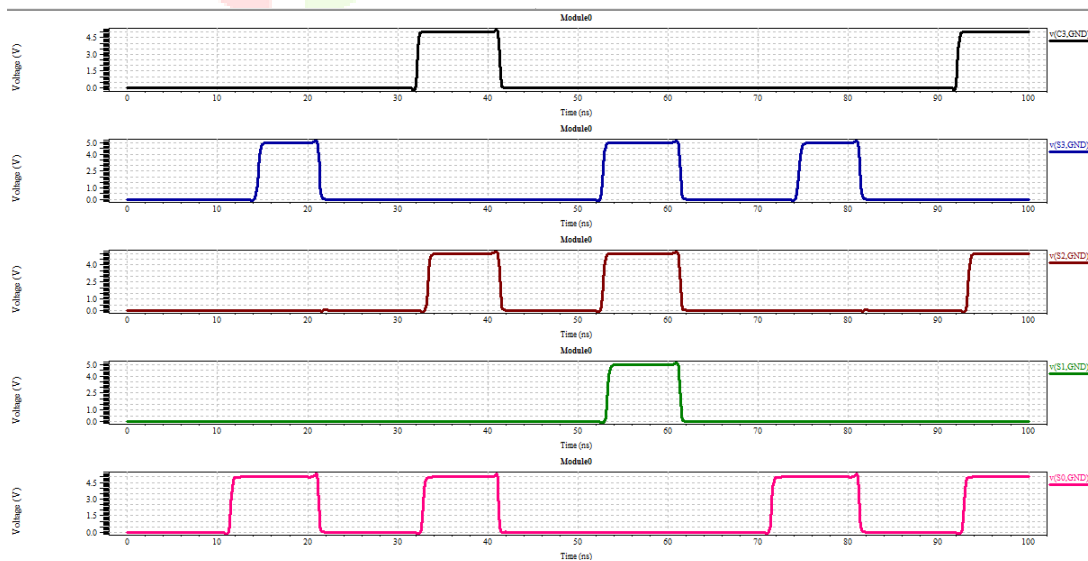Fig. 11 Input waveform for dynamic carry look ahead adder

Fig. 12 Output waveform for dynamic carry look ahead adder

Data Analysis

The largest difference between static and dynamic logic is that in dynamic logic, a clock signal is used to evaluate combinational logic.Dynamic logic, when properly designed, can be over twice as fast as static logic. It uses only the faster N transistors, which improve transistor sizing optimizations. Static logic is slower because it has twice the capacitive loading, higher thresholds, and uses slow P transistors for logic.

Dynamic logic can be harder to work with, but it may be the only choice when increased processing speed is needed. Most electronics running at over 2 GHz these days, require the use of dynamic, although some manufacturers such as Intel have completely switched to static logic to reduce power consumption. Note that reducing power use not only extends the running time with limited power sources such as batteries or solar arrays (as in spacecraft), but it also reduces the thermal design requirements, reducing the size of needed heat sinks, fans, etc., which in turn reduces system weight and cost.

Since the delay in dynamic logic is less so the speed of transistors are more. According to the data analysis the delay in static is 2.5 ns and in dynamic is around 1.8 ns so the dynamic logic is 0.7 times more efficient when compared to static logic.

Description	Delay (ns)	Transistors	Max power(W)	Min power(W)	Average power(W)
Static	2.5	154	$1.089e^{-1}$	$9.654e^{-7}$	$>4.992e^{+1}$
Dynamic	1.8	134	$1.027e^{-1}$	$6.116e^{-6}$	$>3.058e^{+1}$

Table 1:Comparative study on Static and Dynamic logic

VII. CONCLUSION

Thus the Carry Look Ahead Adder is done using model file ML125 and its output waveform and the transient analysis of static and dynamic logic are performed .The power analysis for static and dynamic logics are taken .These techniques were performed on various transistor logics. The proposed dynamic adders provides 28% better efficiency than static adders. dynamic logic greatly increases the number of transistors that are switching at any given time, which increases power consumption over static CMOS. There are several power saving techniques. that can be implemented in a dynamic logic based system. In addition, each rail can convey an arbitrary number of bits, and there are no power-wasting glitches. Power-saving clock gating and asynchronous techniques are much more natural in dynamic logic.

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