MODELLING OF HALF SUBTRACTOR USING 2X1 MULTIPLEXER

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***Abstract*:** In this current paper I have try to reduce the complexity of the electronic circuit using multiplexer. Multiplexer is a kind of digital circuit which can use as universal logic, so here we use the property of multiplexer to implement the half sub-tractor. For electronics processing, opto-electronic conversion of data takes place at the receiving end high data rate signal processing result in increased consumption of power and heat generation from electronic integrated circuit. More numbers of elements used in any electronic circuit dissipate the more heat, so here we use multiplexer to reduce the number of elements in any integrated circuit. It gives finally the solution of heat dissipation in any integrated circuit.

***Index Terms*—Multiplexers (mux); Optical logic gate; AND, OR, NOT.**

I. INTRODUCTION

In the present society where we live is full of digital equipments wherever we see, as we are living and experiencing the information era. In today's world huge amount of data is being generated, transported and processed. Optical fiber is the medium used for transportation of data at very high rate. For electronics processing, opto-electronic conversion of data takes place at the receiving end high data rate signal processing result in increased consumption of power and heat generation from electronic integrated circuit. It is stated in few papers (notomi et al.2011)[1]; Shancham et al.(2008)[2] that even the electronic transportation of high speed data among the processing nodes consumes major chunk of energy. These are the limiting factors in expanding high speed data networking and processing. If data is being transported in optical domain it should also be processed in optical domain and hence the elimination of opto electronic conversion and development of all optical processing is need of the hour. The main advantage of all optical data processing is its high data rate, low power consumption and fast dynamics. Optical logic gates are building blocks of the photonic processing circuits. In recent years extensive research has been done in designing of all optical logic gates like AND (Li et. Al. 2009)[3] OR(Singh et al. 2014)[4], NOT (Singh et al. 2013)[5], NAND (Mohammadnejad et. Al. 2009) [6] and NOR (Hamie et. Al. 2002) [7]. In this current paper the implementation of half sub-tractor have been designed using 2x2 multiplexer which is single level implementation of circuit, while the symbolic block diagram shown in Fig.1 is a kind of 2 level implementation of the circuit which is ultimately enhance the performance of any circuit and reduces the complexity of integrated circuit.

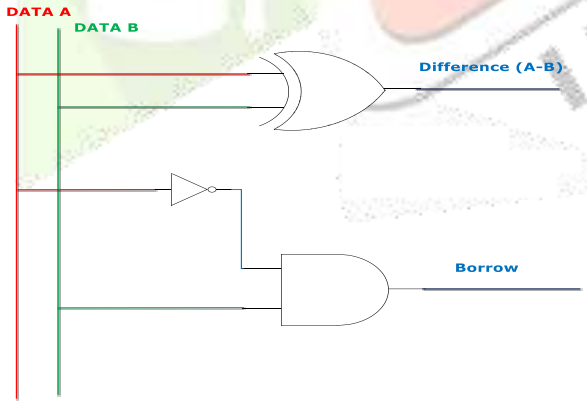

Fig. 1 Symbolic diagram of half subtractor

II. PRINCIPLE OF OPERATION AND MODEL FORMULATION

In the proposed model the logical operation of half sub-tractor i.e borrow and difference are achieved with the help of Multiplexer. The red line shows the input data A while the representation of data B is by green colour other than these two input A ,B data all zero and All one are shows by Input data 0 and input data 1 respectively. In fig 2 the block diagram of proposed model is designed here data A is given in select line in the mux 1, and input1 is given as first input of multiplexer and input 0 given to second input of multiplexer output comes from here gives $\bar{A}$ which is further used as input of second arm of mux 3 while in first arm of multiplexer data A as input . After the data process by mux3 we get the output difference (A-B). At Mux 2 the output comes from mux1 works as

input of second arm in mux2 and data 0 is input for first arm of mux2 which processed by mux 2 and gives the result that is nothing but only borrow of 2 data A and B.

TABLE I FUNCTIONAL TABLE FOR HALF SUBTRACTOR

Serial no.	DATA A	DATA B	DIFFERENCE P	BORROW Q
1.	0	0	0	0
2.	0	1	1	1
3.	1	0	1	0
4.	1	1	0	0

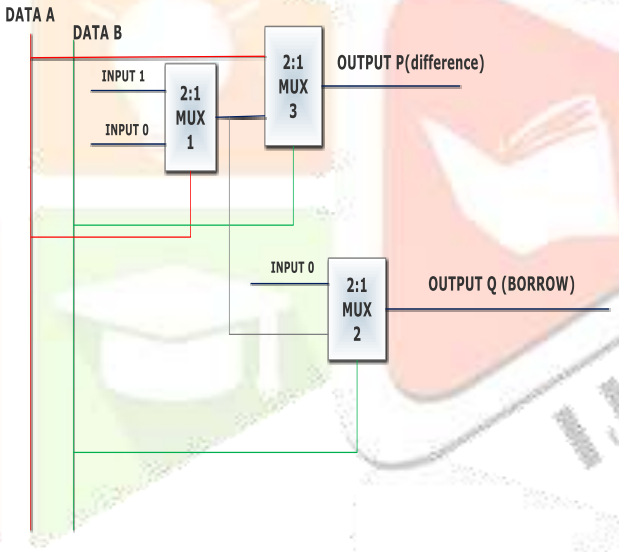

Fig .2 Design of half sub-tractor using 2x1 Mux.

FORMULATION:-

Here A and B are inputs having data values (0011) and (0101) repectively

When data A is given as select lines of MUX 1. The mux process is described as follow.

INTERMIDIATE RESULT FROM MUX 1 = 1x$\bar{A}$+ 0xA

= $\bar{A}$

This result given as input for mux 3 and data B works here as select line. MUX 3 processed as follow and gives the result X as output.

P = Ax$\bar{B}$+$\bar{A}$xB

P = $A\bar{B}$+$\bar{A}$B

P = A$\oplus B$

Above output P verified by standard result that is the difference of half Subtractor.

SIMILARLY,

For mux 2 one arm is inputed by data input zero while in second arm the input is $\bar{A}$ which comes from Mux 1 and data B as select lines. The process of mux 2 is described as follow

Q = 0x$\bar{B}$+$\bar{A}$xB

Q = $\bar{A}$B

Above output **Q** verified By standard result of Borrow.

III. RESULT AND DISCUSSION

The proposed design of photonic circuit works at 10 Gbps data rate. All three Mux's used in this design have similar values Fig. 3a-b represents the input signals, and the output signals represented by fig. 3c and 3d. P is the OUTPUT of half subtractor, and it is verified by truth table Table1. Fig 3d shows the output Q which is Borrow of half subtractor verified by the truth table which is presented by table 1. The output signals shown here are actually the low power probe signals which are the inverted copy of their high power pump signals after passing through SOA. Therefore these overshoots occur for the rising edge of the high power pump signal which corresponds to falling edge of probe signal for the same instance of time. Both rising edge of the pump signal as well as the falling edge of the probe signal experiences high gain due to the presence of high population of carriers for that period of time. One of the reasons for high population of carrier for that particular time period is the absence of high power pump signal just before the overshoot. The overshoot is actually instigated by the high power signal.

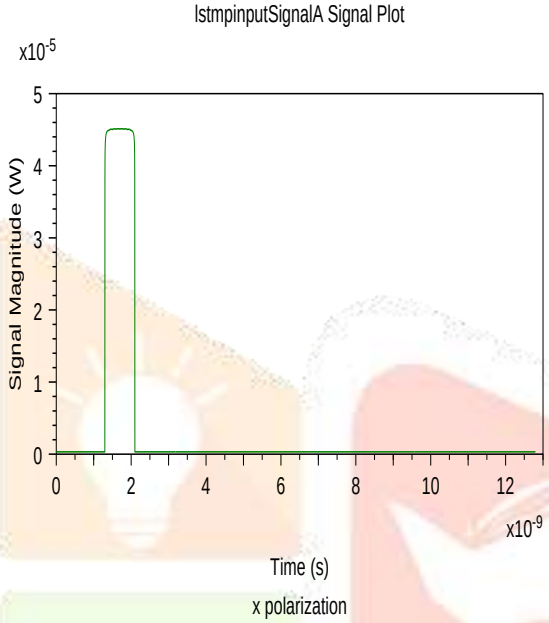

Fig.3(a) INPUT SIGNAL A

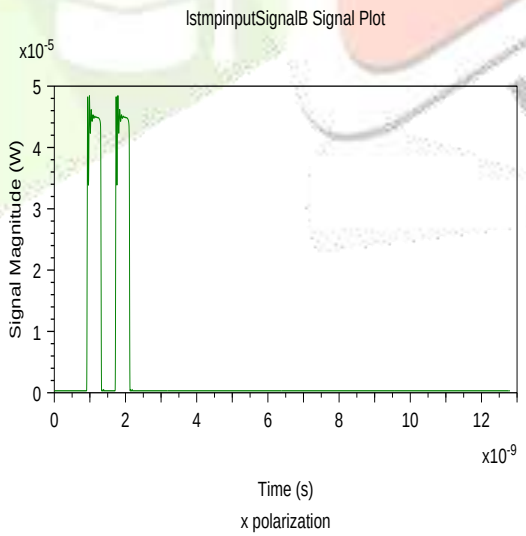

Fig.3(b) INPUT SIGNAL B

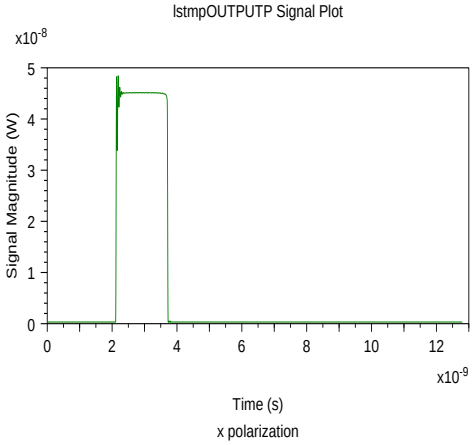

Fig.3(c) DIFFERENCE OF HALF SUBTRACTOR

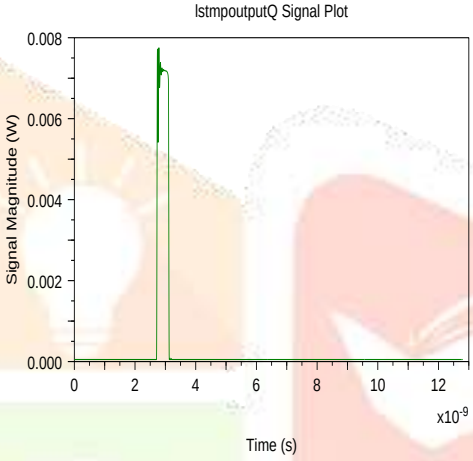

Fig.3(d) BORROW OF HALF ADDER

IV. CONCLUSION

An implementation of DIFFERENCE and BORROW in a single photonic circuit is done success-fully in this manuscript. Multiple optical gates onto a single chip will lead to optical signal processing in the future and electronic circuitry will be replaced by the optical circuitry. With the development of photonic circuitry it is now possible to get any digital result in optical domain. The very basic two input one output optical line selector can be integrated to form a part of more bigger and complex photonic circuit. Development of photonic circuits like these are leading towards all optical signal processing which is the ultimate goal.

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