Design & Implementation of ATC Using Widrow-Hoff LMS Algorithm on FPGA

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Abstract: This paper intends implementation of Widrow-Hoff LMS algorithm to cancel out the noise added to the desired signal. We have taken mixture of sinusoidal signals as input signal and desired signal is also a sinusoidal signal from the input signal. We implement an Adaptive Tone Canceller(ATC) on an FPGA and use the LMS algorithm as the adaptive filtering algorithm of the Adaptive Tone Canceller. Adaptive Tone Canceller is a real-time system that requires high sampling rate, thus FPGA is a good choice,also for its low cost,high speed and reprogram ability.A 5 tap adaptive filter is considered as a system which can adapt the the coefficients after 80 samples.

Keywords-Widrow-Hoff LMS algorithm, FPGA

I. INTRODUCTION

Digital signal processing, which spans a wide variety of application areas including speech and image processing, communications, networks, and so on, is becoming increasingly important in our daily life. Digital signal processing applications impose considerable constraints on area, power dissipation, speed and cost, thus the design tools should be carefully chosen. The most commonly used tools for the design of signal processing systems are: Application Specific Integrated Circuit (ASIC), Digital Signal Processors (DSP) and FPGA. DSP is well suited to extremely complex math-intensive tasks, but cannot process high sampling rate applications due to its serial architecture. ASIC can meet all the constraints of digital signal processing, however, it lacks flexibility and requires long design cycle. FPGA can make up the disadvantages of ASIC and DSP. With flexibility, time-to-market, risk-mitigation and lower system costs advantages, FPGA has become the first choice for many digital circuits' designers.

In this paper, in order to show the performance of FPGA in digital signal processing applications, we implement an Adaptive Tone Canceller on an FPGA and use the Widrow-Hoff LMS algorithm as the adaptive filtering algorithm of the Adaptive Tone Canceller. Adaptive Tone Canceller is a real-time system that requires high sampling rate, thus FPGA is a good choice. LMS algorithm, originally proposed by Widrow and others, is widely used for adaptive filter [1], [12]. After that, delayed LMS (DLMS) algorithm [2] has been derived to achieve low latency. The previous works of Very Large Scale Integrated Circuit (VLSI) implementations of LMS and DLMS are shown in [3]-[5]. However, they are mainly concerned with the convergence behavior of LMS or DLMS, the detailed implemental process of VLSI and the advantage of VLSI implementation are not mentioned clearly. This paper is based on the performance of FPGA implementation of an Adaptive Tone Canceller.

II. ATC SYSTEM

As the name implies, ATC is a technique used to remove an unwanted tone from a received signal, the operation is controlled in an adaptive way. As shown in Fig.1.1, an ATC is typically a dual-input, closed-loop adaptive feedback system. The two inputs are: the primary input signal d(n) (the desired tone signal tone extracted) and the reference signal x(n) (an interfering noise supposed to be uncorrelated with the desired signal plus multi tone signal). The adaptive filtering operation achieved the best results when the system output is noise plus unwanted tone free, which means that the output SNR is infinitely large.

ATC technique has been successfully applied to many applications, such as acoustic noise reduction, adaptive speech enhancement and channel equalization. In these cases and other related high speed required applications, pure software implementation would bring about long processing time, thus cannot meet the requirement. An effective way can be represented hardware implementation on FPGA.

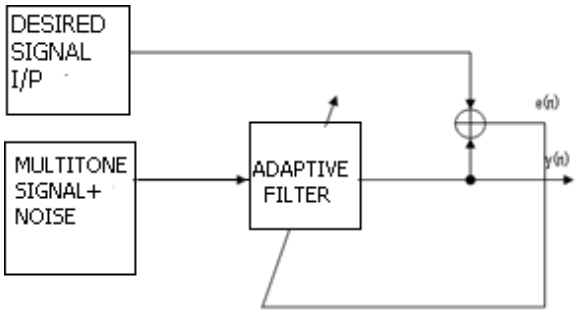

Fig-1-ATC System Block diagram

III. LMS ALGORITHM

Due to computational simplicity, unbiased convergence in the mean to the wiener solution and existence of proof of convergence in a stationary environment[7], Least Mean square(LMS) algorithm is widely used in application to adaptive filtering. Also its behavior is quite simple to understand and algorithm appears to be very robust[12].

The Widrow–Hoff least mean square (LMS) adaptive algorithm is a practical method for finding a close approximation in real time. The algorithm does not require explicit measurement of the correlation functions, nor does it involve matrix inversion. Accuracy is limited by statistical sample size, since the filter coefficient values are based on the real-time measurements of the input signals.

The LMS algorithm is an implementation of the method of the steepest descent. According to this method, the next filter coefficient vector h[n + 1] is equal to the present filter coefficient vector **h[**n] plus a change proportional to the negative gradient:

$$h[n+1] = h[n] - \frac{\mu}{2}\nabla[n]$$

The parameter μ is the learning factor or step size that controls stability and the rate of convergence of the algorithm. During each iteration the true gradient is represented by $\nabla[n]$.
The LMS algorithm estimates an instantaneous gradient in a crude but efficient manner by assuming that the gradient of $J = e[n]^2$ is an estimate of the gradient of the mean-square error $E\{e[n]^2\}$.

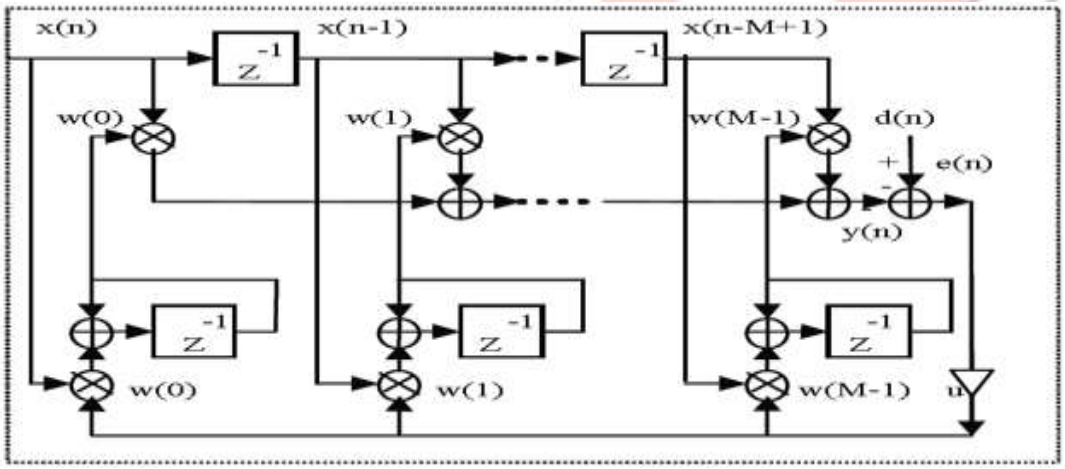

Fig-2-Structure of LMS algorithm

The Widrow–Hoff LMS algorithm to adjust the N filter coefficients of an adaptive uses the following steps:

1)Initialize the (N × 1) vector $\boldsymbol{h} = \boldsymbol{x} = \boldsymbol{0} = [0, 0, \ldots, 0]^T$.
2) Accept a new pair of input samples $\{x[n], d[n]\}$ and shift $x[n]$ in the reference signal vector $\boldsymbol{x}[n]$.

3) Compute the output signal of the FIR filter, via $y[n] = \boldsymbol{h}^T[n]\boldsymbol{x}$[n]
4) Compute the error function with $e[n] = d[n] - y[n]$.
5) Update the filter coefficients according to
h[n + 1] = h[n] + 2$\mu e[n]\boldsymbol{x}[n]$.
Now continue with step 2.
Design problem specification for 5 tap Adaptive Filter:

- Application type: Tone Cancellation
- Algorithm used: Widrow Hoff LMS algorithm

- Filter Length or no. of taps: 5
- Hardware architecture: Direct form
- No. input Signal samples :80
- Sampling frequency: 5 times of signal samples
- Signal to Noise Ratio(SNR_{dB}): 30
- Input data and Co-efficient length: 8bits
- Output data length: 16 bits

IV. SIMULATION RESULT

Main part in the ATC is to implement the LMS algorithm. The design is simulated both in MATLAB and XILINX by taking a learning factor of 0.25. In this problem a 5 tap adaptive filter is considered as a system which can adapt the the coefficients after 80 samples. In MATLAB ,a sinusoidal mixture is given as input to the system. Also the desired signal is given. First the system is trained for 80 samples.The error squre is minimized which has been shown in convergence curve fig 4. From fig. comparing the output of the system and the desired signal,it can be clearly observed that initially there is some difference but later as number of samples increase it lies on the desired signal and the co-efficients of filter can be found out form fig 6.

The filter weights atfter computing 80th sample

W=[0.1 ,-0.4 ,-0.76 ,-0.7, -0.43]

fig.

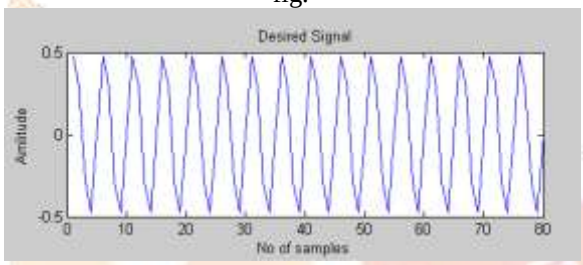

Fig 3-Desired signal

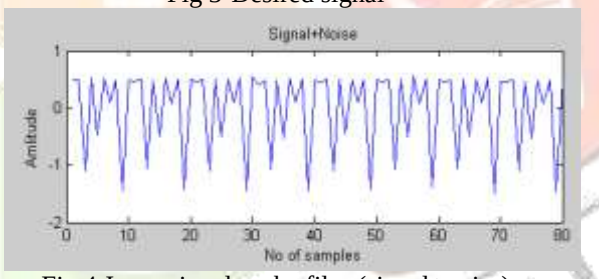

Fig 4-Input signal to the filter(signal+noise)

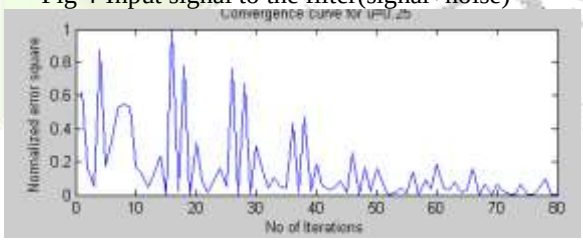

Fig 4-Convergence curve for u=0.25

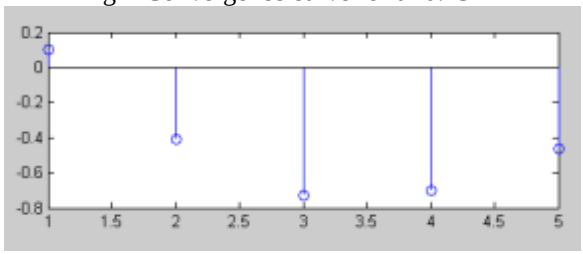

Fig 5-filter coefficients after 80th sample

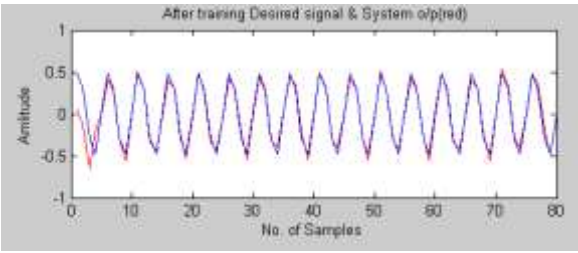

Fig 6:comparing system o/p and desired signal

Simulating the problem with same data taken for MATLAB in Xilinx with VHDL it has the same filter coefficients after 80th sample.The RTL view of the ATC and its internal views shown in fig 7 & 8 respectively.Also the logic utilization data shown in table 1.

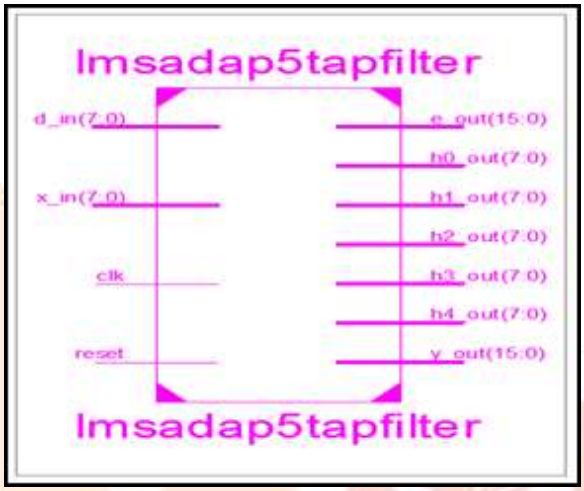

Fig 7-RTL View

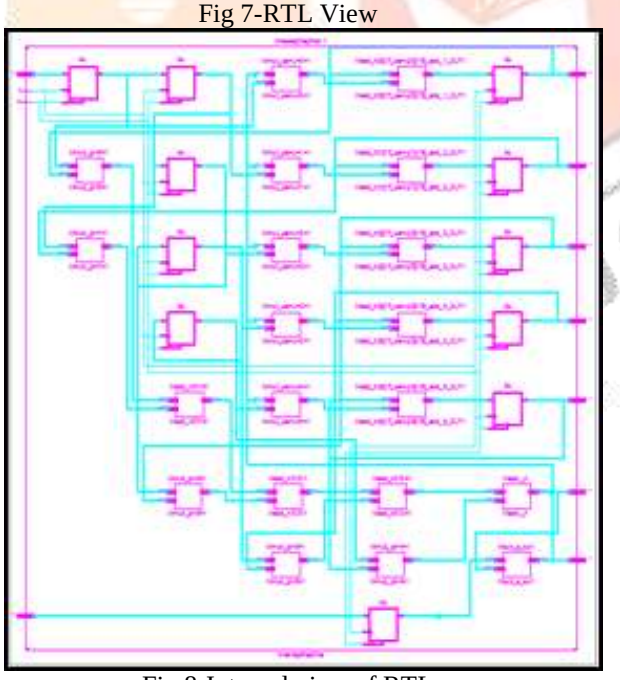

Fig 8-Internal view of RTL

Logic Utilization	Used
Number of Slice Registers	88
Number of Slice LUTs	50
Number of fully used LUT-FF pairs	40
Number of bonded IOBs	90
Number of BUFG/BUFGCTRLs	1
Number of DSP48E1s	10

Table.1-Logic Utilization

The samples of x(n) and d(n) are quantized with 8bit signed format. The quantized values are entered in test bench i/p and then simulated. The o/p y_out ,e_out and w vector are obtained at 80th sample almost same to the MATLAB simulation**.**After that downloading the design ito the FPGA board we implemented the ATC.Here we implement it on VIRTEX II PRO –PROTOBOARD (MODEL – MXV2P4/7FP-000-RKPC-001). Virtex-II Pro devices are user-programmable gate arrays with various configurable elements and embedded blocks optimized for high density and high-performance system designs.Virtex-II Pro devices implement the following functionality: Embedded high-speed serial transceivers enable data bit rate up to 1.25 Gb /s per channel (Gigabit Ethernet).Embedded IBM PowerPC 405 RISC processor blocks provide performance of 300+ MHz

V.CONCLUSION:

For today's life adaptive filter is very important for the communication purpose and also for military purpose as it adapts its environment very quickly(using LMS algorithm).In terms of high speed architecture the direct form approach is preferred for design ,The architecture is successfully implemented in FPGA.FPGA devices an ideal solution for military and university research for its low cost,high speed and reprogram ability. The high speed capability and register rich architecture of FPGA an ideal implementation of LMS algorithm. The design implementation entailed the employment of Xilinx ISE14.7 & MATLAB 2011a software tool. Implementing the design on a virtex-II chip and hardware testing and verification of the Adaptive FIR filter could be done successfully . Finally simulation and synthesis with Xilinx xst tool and RTL schematic of Adaptive filter chip obtained .

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