Survey of Content Addressable Memory

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Abstract : Content-addressable memory (CAM) is a type computer memory for search applications that operates like a hardware search engine. It is used in certain very-high-speed searching applications. It is also known as associative memory, associative storage, or associative array. It compares input search data against a table of stored data, and returns the address of matching data. It is capable of searching its whole contents in a single clock cycle. It does that by pairing the SRAM-based memory with additional logic comparison circuitry that is active on every clock cycle. The time required to find an item stored in memory for access can be reduced by identifying its content rather than by its address. The CAM has a parallel active circuitry which consumes more power and the main challenge in designing the CAM is to reduce the power consumption without reducing the speed and memory density. It provides a performance advantage over other memory search algorithms, such as binary or tree-based searches or look-aside tag buffers, by comparing the desired information against the entire list of pre-stored entries simultaneously, often resulting in an order-of-magnitude reduction in the search time. Here review of low power match line sensing techniques is concentrated. There are different types of CAM architectures available today, each of them having its own advantages as well as disadvantages. Here a comparative study on different Content Addressable Memory architecture is done.

Index Terms **- Content-addressable memory (CAM), Associate memory, Match line sensing, Search line power**

I. INTRODUCTION

A Content Addressable Memory is a type of ordinary memory that can be accessed using its contents rather than address. In order to access a particular entry, a search data word is compared against previously stored word in parallel to find a match. Each stored word is associated with a tag that is used in the comparison process. Once a search data word is applied to the input of CAM, the matching data word is retrieved within a single clock cycle. This prominent feature makes CAM a promising candidate for applications where frequent and fast look-up operations are required, such as in translation look-aside buffers (TLBs), database accelerators, image processing, parametric curve extraction, Hough transformation, Huffman coding/decoding and image coding. Although dynamic CMOS circuit techniques can result in low-power and low-cost CAM's, these designs can suffer from low noise margins, charge sharing, and other problems not to be energy efficient when scaled.

CAM is used in applications where search time is very critical and very short. It is well suited for several functions like Ethernet address lookup, data compression, and security or encryption information on a packet-by packet basis for high performance data switches. It can also be operated as a data parallel or Single Instruction/Multiple Data (SIMD) processor. Since CAM is an extension of RAM first, we have to know the RAM features to understand CAM. In general RAM has two operations read and write i.e. the data stored in RAM can be read or written but CAM has three operations read, write and compare [1]. The compare operation of CAM makes it useful in variety of applications like network routers. The network router is that which forwards the incoming packets from the sender port to the proper destination port by looking in to its routing table. Basically CAMs are used to design network routers for fast transfer or forwarding of packets.

The next section II the Literature Review includes the details on various content addressable memories and the architectural effects on energy consumption and performance. The section III contains the comparative analysis on the various algorithms included in former section. The next section IV concludes the survey and a better choice among the previous algorithm and its performance results is also included.

II. BASICS OF CONTENT ADDRESSABLE MEMORY

CAM comprises memory element, usually built with 6T SRAM cell and a circuit to compare search bit against the stored bit. NOR- and NAND-type MLs are the two basic comparison circuits presented as follows.

2.1 CAM fundamentals

A detailed model of CAM is shown in Figure 2.1. The figure shows the CAM cell for 3 words and each word having 3 bits. That corresponds to 3 CAM cells. There is a match line is connected to each words and cell is connected with search line pairs. These are connected to match line sense amplifiers. Each CAM cell is stored with some data and the search operation starts with loading the register with search data. And also these are recharged to high value. The high value is in the match line. Next the search data from the register is given to these arch lines. The CAM cell compares the stored data against the search data bits on the search lines. If the comparison result is a mismatched condition then the match lines are discharged otherwise these remain in the precharged high state.

The match line sense amplifier finds the matched or mismatched condition. And the encoder encodes the matching location to its encoded address

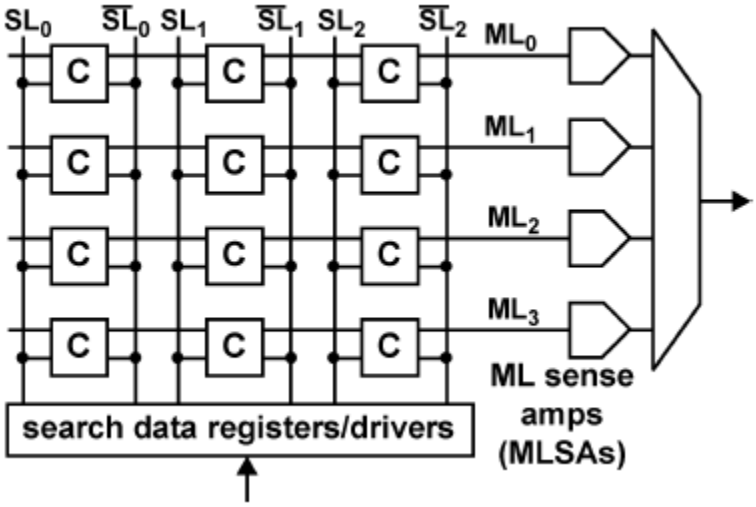


Fig. 2.1 CAM fundamentals

2.2Basic operation of CAM cell

The basic CAM cell is based on the static memory cell. Data is stored in the two cross coupled inverters. The two NMOS transistors controlled by the word line which allow the CAM to be written. The four additional transistors used for matching. The bit storage portion is a standard 6T static RAM (SRAM) cell. Hence, this cell performs READ and WRITES operations similar to an SRAM cell. Third operation is MATCH operation. For matching a data bit with stored bit, first leave the word line low then Precharge match line. Place key on bit line. Match line is evaluated.

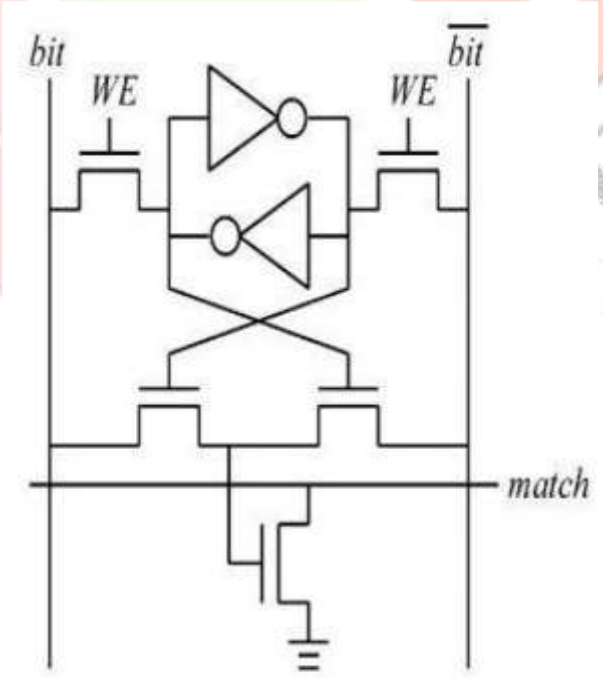


Fig. 2.2 block diagram of CAM cell

2.3 NAND- type CAM cell

The NAND cell implements the comparison between the stored bit, D, and corresponding search data using the three comparison transistors M1,MD, and MDB , which are all typically minimum-size to maintain high cell density. Consider the case of a match, when SL =1 and D=1 Pass transistor MD is ON and passes the logic 1 on the SL to node B. If there is a match in the cell when the node B is the bit-match node which is logic 1. The logic 1 on node B turns ON transistor M1. Note that M1 is also turned ON in the other match case when SL =0 and D=0. In this case, the transistor MDB passes logic high to raise node B. For the remaining cases, where SL not equal to D result in a mismatch condition, and accordingly node B is logic is 0 and the transistor M1 is OFF. Node B is a pass-transistor implementation of the XNOR function SL XNOR D. The NAND nature of this cell becomes clear when multiple NAND cells are serially connected. In this case, the MLn and MLn+1 and nodes are joined to form a word. A serial NMOS chain of all the transistors resembles the pull down path of a CMOS NAND logic gate.

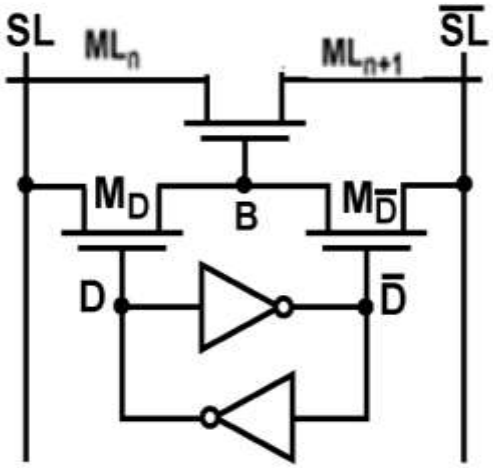


Fig. 2.3 block diagram of CAM cell

2.4 NOR-type CAM cell

The NOR cell implements the comparison between the complementary stored bit, D (and ~D), and the complementary search data on the complementary search line, SL (and ~SL), using four comparison transistors, M1 through M4, which are all typically minimum-size to maintain high cell density.These transistors implement the pull down path of a dynamic XNOR logic gate with inputs SL and D. Each pair of transistors, M1/M3 and M2/M4, forms a pull down path from the match line, ML, such that a mismatch of SL and D activates least one of the pull down paths, connecting ML to ground.

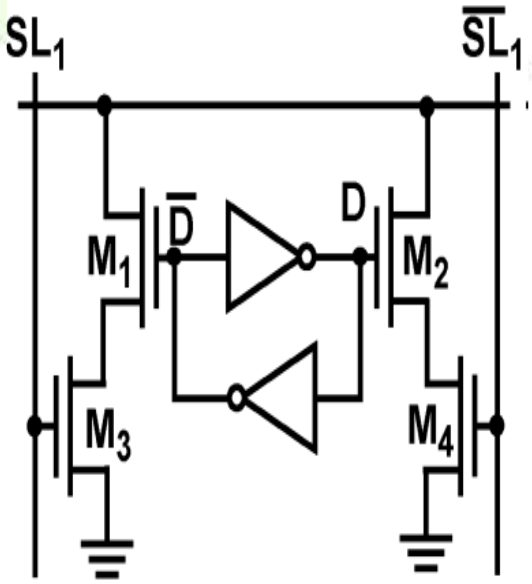


Fig.2.4 NOR-type CAM cell

A match of SL and D disables both pull down paths, disconnecting ML from ground. The NOR nature of this cell becomes clear when multiple cells are connected in parallel to form a CAM word by shorting the ML of each cell to the ML of adjacent cells. The pull down paths connect in parallel resembling the pulldown path of a CMOS NOR logic gate. There is a match condition given ML only if every individual cell in the word has a match.

2.5 Match line structures

Basically, match line is one of the key structures in CAMs. The NOR cell and NAND cell are used to construct a CAM match line.

2.5.1 NOR match line

The schematic form of NOR match line is shown in Fig 5. The NOR cells are connected in parallel to form a NOR match line. A typical NOR search cycle operates in three phases: search line precharge, match line precharge, and match line evaluation. First, the search lines are precharged low to disconnect the match lines from ground by disabling the pull down paths in each CAM cell. Second, with the pull down paths disconnected, the Mpre transistor precharges the match lines high. Finally, the search lines are driven to the search word values, triggering the match line evaluation phase. In the case of a match, the ML voltage, VML, stays high as there is no discharge path to ground. In the case of a miss, there is at least one path to ground that discharges the match line. The match line sense amplifier (MLSA) senses the voltage on ML, and generates a corresponding full-rail output match result. The main feature of the NOR match line is its high speed of operation. In the slowest case of a one-bit miss in a word, the critical evaluation path is through the two series transistors in the cell that form the pull down path. Even in this worst case, NOR-cell evaluation is faster than the NAND case, where between 8 and 16 transistors form the evaluation path [1].

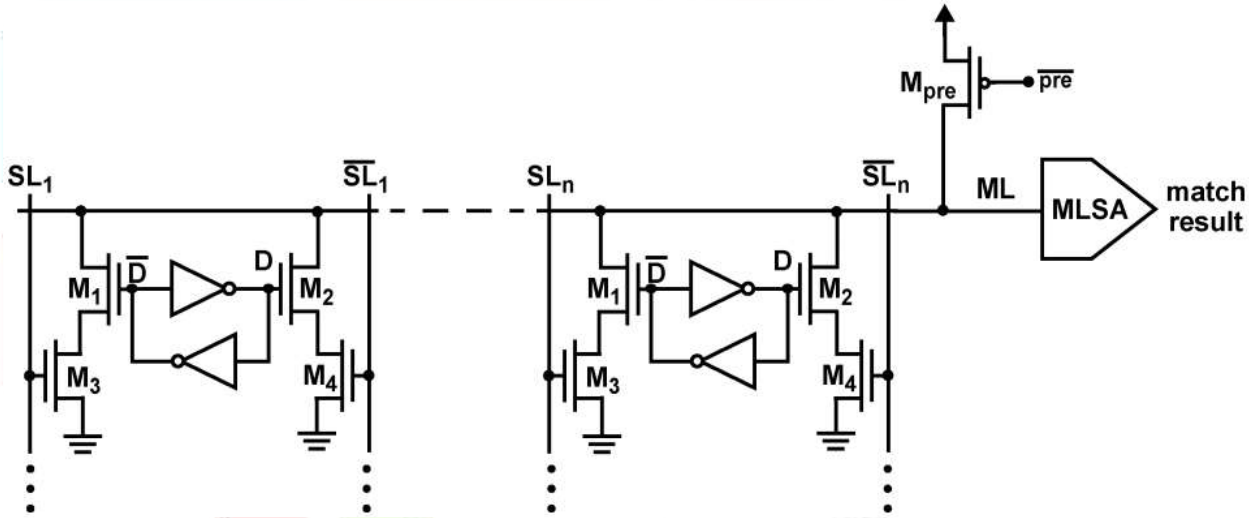


Fig.2.5 Structure of a NOR matchline with n cells

2.5.2 NAND match line

A number of n cells are cascaded to form the NOR match line. The prechargepMOS transistor, Mpre, sets the initial voltage of the match line, ML, to the supply voltage, VDD. Next, the evaluation nMOS transistor, Meval, turns ON. In the case of a match, all nMOS transistors, M1through Mn are ON, effectively creating a path to ground from the ML node, hence discharging ML to ground. In the case of a miss, at least one of the series nMOS transistors, M1through Mn, is OFF, leaving the ML voltage high. A sense amplifier, MLSA, detects the difference between the match (low) voltage and the miss (high) voltage. The NAND match line has an explicit evaluation transistor, Meval, unlike the NOR match line, where the CAM cells themselves perform the evaluation. There is a potential charge sharing problem in the NAND matchline. Charge sharing can occur between the ML node and the intermediate MLi nodes. This charge sharing may cause the ML node voltage to drop sufficiently low such that the MLSA detects a false match. A technique that eliminates charge sharing is to precharge high, in addition toML, the intermediate match nodes ML1 through MLn-1.

This procedure eliminates charge sharing, since the intermediate match nodes and the ML node are initially shorted. However, there is an increase in the power consumption due to the search line precharge. A feature of the NAND match line is that a miss stops signal propagation such that there is no consumption of power past the final matching transistor in the serial nMOS chain. Typically, only one match line is in the match state, consequently most matchlines have only a small number of transistors in the

chain that are ON and thus only a small amount of power is consumed. Two drawbacks of the NAND match line are a quadratic delaydependence on the number of cells, and a low noise margin. The quadratic delay-dependence comes from thefact that adding a NAND cell to a NAND matchline adds both a series resistance due to the series nMOS transistor and a capacitance to ground due to the nMOS diffusion capacitance. These elements form an RC ladder structure whose overall time constant has a quadratic dependence on the number of NAND cells. The low noise margin iscaused by the use of nMOS pass transistors for the comparison circuitry. NOR cells avoid this problem by applying maximum gate voltage to all CAM cell transistors when conducting [1].

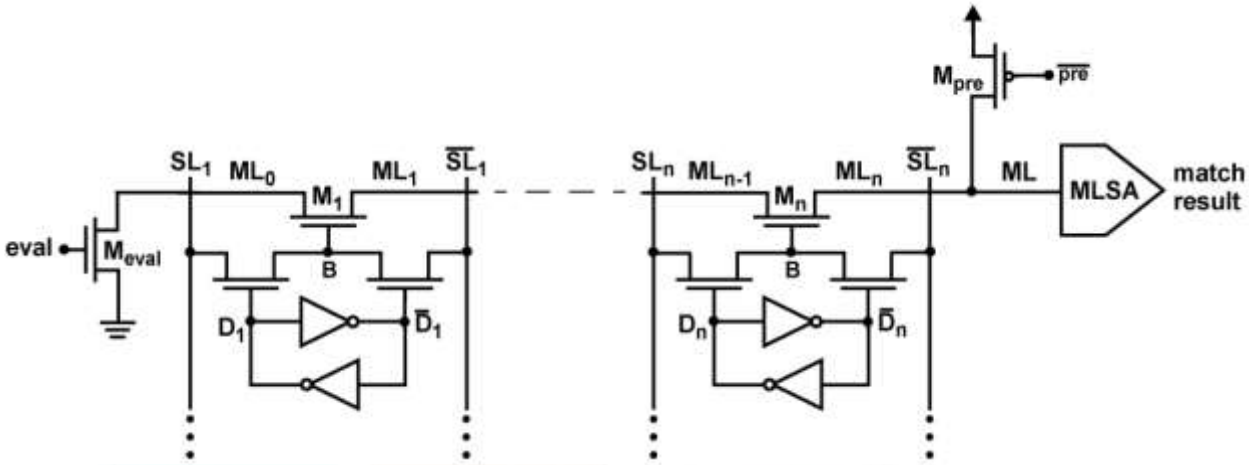


Fig.2.6 Structure of a NAND match line with n cells

III. MATCH LINE SENSING SCHEMES

3.1 Selective-Precharge Scheme

This scheme performs a match operation on the first few bits of a word before activating the search of the remaining bits [5]. For example, in a 144-bit word, selective precharge searches only the first 3 bits and then searches the remaining 141 bits only for words that matched in the first 3 bits., The initial 3-bit search should allow only ½ words to survive to the second stage saving about 88% of the matchline power by assuming uniform distribution. There are two sources of overhead that limit the power saving in practice. First, the initial match implementation may draw a higher power per bit than the search operation on the remaining bits to maintain speed. Second, an application may have a data distribution that is not uniform and the initial match bits are identical among all words in the CAM, eliminating any power saving.

Fig. 7 is a simplified schematic of an example of selective precharge similar to that presented in the original paper [5]. The example uses the first bit for the initial search and the remaining bits for the remaining search. To maintain speed, the implementation modifies the precharge part. The ML is precharged through the transistor , which is controlled by the NAND CAM cell and turned on only if there is a match in the first CAM bit. The remaining cellsareNOR cells. Note that the ML of the NOR cells must be pre-discharged to ground to maintain correct operation in the case that he previous search left the matchlinehigh . Thus, one implementation of selective precharge is to use this mixed NAND/NOR matchline structure. Selective precharge is perhaps the most common method used to save power.

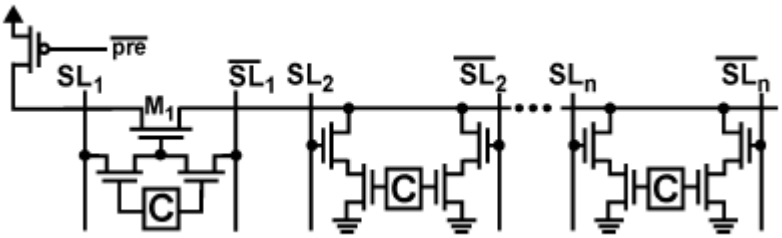
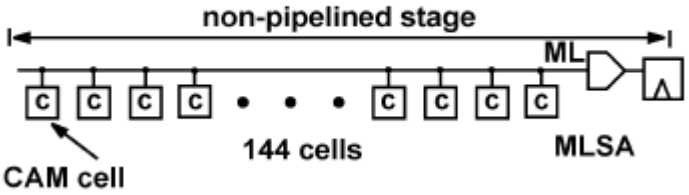


Fig.3.1 Selective-Precharge technique

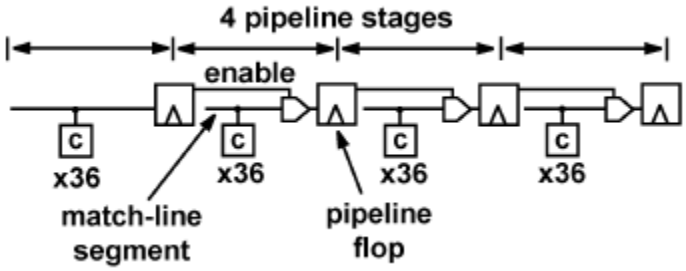
3.2Pipelining Scheme

In selective precharge, the matchline is divided into two segments. More generally, an implementation may divide the matchline into any number of segments, where a match in a given segment results in a search operation in the next segment but a miss terminates the match operation for that word. A design that uses multiple matchline segments in a pipelined fashion is the pipelined

matchlines scheme [6], [7]. Fig. 8(a) shows a simplified schematic of a conventional NOR matchline structure where all cells are connected in parallel. Fig. 8(b) shows the same set of cells as in Fig. 8(a), but with the matchline broken into four matchline segments that are seriallyevaluated. If any stage misses, the subsequent stages are shut off, resulting in power saving. The drawbacks of this scheme are the increased latency and the area overhead due to the pipeline stages. By itself, a pipelined matchline scheme is not as compelling as basic selective precharge; however, pipelining enables the use of hierarchical searchlines, thus saving power. Section IV discusses hierarchical searchlines in detail. Another approach is to segment the matchline so that each individual bit forms a segment [51]. Thus, selective precharge operates on a bit-by-bit basis. In this design, the CAM cell is modified so that the match evaluation ripples through each CAM cell. If at any cell there is a miss, the subsequent cells do not activate, as there is no need for a comparison operation. The drawback of this scheme is the extra circuitry required at each cell to gate the comparison with the result from the previous cell.



(a)



(b)

Fig.3.2Pipelined match lines reduce the power after the miss in a stage

3.3 Current Saving Scheme

The current-saving scheme [9], is another data-dependent matchline-sensing scheme which is a modified form of the current-race sensing scheme. Recall that the current-race scheme uses the same current on each matchline, regardless of whether it has a match or a miss. The key improvement of the current-saving scheme is to allocate a different amount of current for a match than for a miss. In the current-saving scheme, matches are allocated a larger current and misses are allocated a lower current. Since almost every matchline has a miss, overall the scheme saves power. Fig. 9 shows a simplified schematic of the current-saving scheme. The main difference from the current-race scheme is the addition of the current-control block. This block is the mechanism by which a different amount of current is allocated, based on a match or a miss. The input to this current-control block is the matchline voltage, and the output is a control voltage that determines the current, , which charges the matchline. The current-control block provides positive feedback since higher results in higher, which, in turn, results in higher .

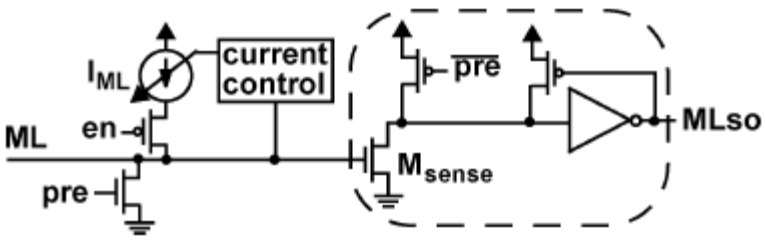


Fig.3.3 Current Saving Match lines Scheme

3.4 Parity-Bit based Scheme

A versatile auxiliary bit to boost the search speed of the CAM at the cost of less than 1% area overhead and power consumption extra bit. During the search operation, there is only one single stage assign conventional CAM. Hence, the use of these parity bits does not improve the power performance[8]. However, this additional parity bit, in theory, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half, as discussed below. In the case of a matched in the data segment the parity bits of the search and the stored word is the same, thus the overall word returns a match. When mismatching of 1 occurs in the data segment, numbers of "1"s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different. Therefore now we have two mismatches (one from the parity bit anode from the data bits). If there are two mismatches in the data segment or the parity bits are the same and overall we have two mismatches. With more mismatches, we can ignore these cases as they are not crucial cases. The sense amplifier now only has to identify between the 2-mismatch cases and the matched cases. Since the driving capability of the 2-mismatch word is twice as strong as that of the 1-mismatch word, the proposed design greatly improves the search speed.

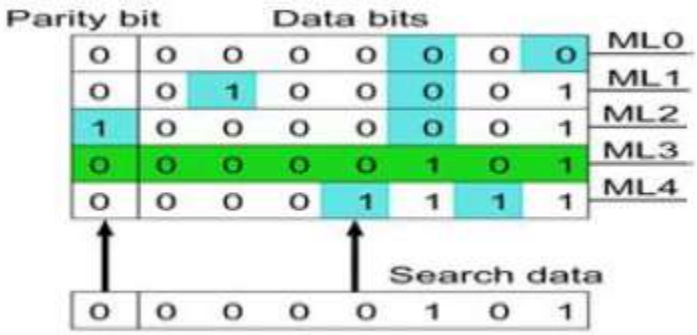


Fig.3.4 Parity-Bit Based Scheme

3.5Eliminating Search line Precharge

We can save search line power by eliminating the SL precharge phase. Eliminating the SL precharge phase reduces the toggling of the searchlines, thus reducing power. The match line-sensing schemes that precharge the match line low eliminate the need for SL precharge, since activating the pull down path in the NOR cell does not affect with match line precharge. These schemes directly activate the searchlines with their search data without going through an SL precharge phase. Since, in the typical case, about 50% of the search data bits toggle from cycle to cycle, there is a 50% reduction in search line power, compared to the precharge-high matchlinesensing schemes that have an SL precharge phase. The reduced power equation in this case is

$$P_{SL} = \frac{1}{2} n C_{SL} V_{DD}^2 f \quad (1)$$

This equation shows that match line-sensing schemes that precharge the match lines low also save power on the searchlines. In fact, in these precharge-low schemes, the reduction in search line power can be as large as, or even larger than, the reduction in match line power.

IV. LITERATURE REVIEW ON CAM

4.1 Pipelined match-lines and hierarchical search-lines for low-power content-addressable memories

Pagiamtzis K et al (2004) developed a Content Addressable Memory which is a combination of pipelined architecture and hierarchical architecture. The power can be saved by power adding pipelining to match-lines and adding hierarchy to search-lines in an otherwise non pipelined, non-hierarchical CAM. The power savings of the pipelined match-lines is a result of activating only a small portion of the match line segments. Similarly, the power savings of the hierarchical search-lines is a result of activating only a small portion of the local search lines [6]. Pipelining match-lines saves 56% power compared to non-pipelined match-lines. Adding hierarchy to search-lines saves 63% power compared to nonhierarchical search-lines. The combination of the two techniques reduces overall power consumption by 60% [4].

The match line is divided into five match line segments, each evaluated sequentially in a pipeline fashion. The left-most segment has 8 bits while the other four segments have 34 bits each, for a total of 144 bits (a typical word width used for IPv6 address lookup).The match line segment array (MLSA) current source that provides the current is divided among the five segments in

proportion to the number of bits in each segment. This is to guarantee identical speed in all match line segments and to allow a fair comparison with the non pipelined architecture. The pipelined match line operates from left to right, with each match line segment acting as an enable signal for the match line segment array of the subsequent segment. Hence, only words that match a segment proceed with the search in their subsequent segments [4-9]. Words that fail to match a segment do not search for their subsequent segments and hence consume no power.

Having pipelined the match-lines, the significant portion of the power is now consumed by the highly capacitive search lines. This problem is solved by observing how the search lines are activated in the pipelined match line architecture. As the match signals traverse the pipeline stages from left to right, fewer match lines segments survive the matching test and hence fewer match line segments will be activated. However, the search lines must be activated for the entire array at every stage of the pipeline, since the search-lines must reach the surviving match-line segments. This excessive power consumption is curtailed in our design by breaking the search-lines into global and local search-lines (GSLs and LSLs), with the global search-lines using low-swing signaling and the local search-lines using full-swing signaling but with reduced capacitance. Also, by global search-lines not directly serving every single Content Addressable Memory cell on a search line, the global search-lines capacitance is further reduced, resulting in extra power savings.

4.2 A low-power pre computation based fully parallel content-addressable memory

Lin C et al (2003) developed an architectural technique for saving power, which applies only to binary CAM, is pre-computation. Pre-computation stores some extra information along with each word that is used in the search operation to save power. These extra bits are derived from the stored word, and used in an initial search before searching the main word. If this initial search fails, then the Content Addressable Memory aborts the subsequent search, thus saving power[1]. The extra information holds the number of ones in the stored word. For example when searching for the data word, 10111, the pre-computation circuit counts the number of one's (which is four in this case). Hence PB-CAM is also known as 1's count [9]. First, it counts the number of ones in an input and then compares the result with that of the entries using an additional CAM circuit that has the number of ones in the CAM data previously stored. This activates a few MLs and deactivates the others. In the second stage, a modified Content Addressable Memory hierarchy is used, which has reduced complexity, and has only one pull-down path instead of two compared with the conventional design. The modified architecture only considers 0 mismatches instead of full comparison since the 1s have already been compared. The number of comparisons can be reduced to $M \times [\log (N+2)] + (M \times N)/(N+1)$ bits, where M is the number of entries in the Content Addressable Memory and N is the number of bits per entry [3]. In the proposed design, we demonstrate how it is possible to reduce the number of comparisons to only N bits. Furthermore, in PB-CAM, the increase of the tag length affects the energy consumption, the delay, and also complicates the pre computation stage.

4.3 Use of selective precharge for low power on the match lines of content-addressable memories

Zukowski C et al (1997) developed a CAM aimed at reduced energy consumption. Energy reduction of Content Addressable Memory employing circuit-level techniques are mostly based on the following strategies: 1) reducing the SL energy consumption by disabling the precharge process of SLs when not necessary and 2) reducing the ML precharging, for example, by segmenting the ML, selectively precharging the first few segments and then propagating the precharge process if and only if those first segments match [6]. This segmentation strategy increases the delay as the number of segments is increased. A hybrid-type CAM integrates the low-power feature of NAND type with the high-performance NOR is type while similar to selective precharging method, the ML segmented into two portions. The high-speed CAM designed in 32-nm CMOS achieves the cycle time of 290 Ps using a swapped Content Addressable Memory cell that reduces the search delay while requiring a larger Content Addressable Memory cell (11-transistors) than a conventional Content Addressable Memory cell [9 transistors(9T)] used in SCN- Content Addressable Memory . A high-performance AND-type match-line scheme is proposed in, where multiple fan-in AND gates are used for low switching activity along with segmented-style match-line evaluation to reduce the energy consumption

4.4 Precharge-Free, Low-Power Content-Addressable Memory

Zackriya V. M et al(2016) developed a Precharge-Free CAM to reduce power consumption. The development of a CAM structure is carried out with a PRE signal, which ends up at a lower speed of search operation. In this drawback has been eliminated by removal of the PRE phase.Instead, they used control bits (CBs), which reduced the overall search time by one level. In a CAM, the first operation is write, followed by precharge, and then search. However, in the PF-CAM architecture[12], the write is followed directly by the search phases. The operation of the PF-CAM is as follows.

1) While storing the data, CB is set to a high value (logic 1). This setting of CB turns M0 OFF and, simultaneously, M1,……MN−1 will be turned OFF as T0,T1,……TN−1 are ON, which will provide GND directly to the gate of M1,……MN−1, as shown in Fig. 3.1.

2) Once the data are stored, CB is reset (0) and this will turn ON M0 as M0 is a pMOS, since the source of M0 is connected as a control to M1, thus S0 value is passed to the gate of M1, which is an nMOS. If CAM cell-1 is matched, M0 will pass logic high to M1, which will result in turning ON of M1. If CAM cell-2 is also matched, then in a similar fashion logic high will be passed to M3 from CAM cell-2, and likewise a cascaded chain of CBs will be passed from one cell to another. If there is a mismatch at any cell, then the forthcoming cells will be turned OFF.

The PF-CAM structure gives advantage by reduction in the number of SC paths, which in turn results in overall reduction of power; however, due to cascading of CAM cells overall, the speed of search operation is significantly reduced.

4.5 Self-Controlled High-Performance Precharge-FreeContent-Addressable Memory

TelajalaVenkataMahendraet al(2017) developed a Self-Controlled Precharge-Free CAM to increase the search speed . Precharged MOS connected to all MLs of CAM architectures are available in the literature. The CAM precharges and evaluates all the MLs for every PRE cycle during the low and high level of the PRE signal, respectively. In butterfly and hierarchical manner word structures are designed based on splitting the complete word structure into fragments[11]. Precomputation-based precharging has been used by selectively precharging all MLs. PRE-based CAMs mainly suffer from the following.

1) The speed of the search operation is restricted by the precharge phase.

2) Dependence among CAM cells restricts the speed of search operation and this affects the overall performance.

3) NAND-type ML suffers from the charge sharing problem. In SCPF-CAM, the advantage of the PF-CAM structure is exploited; moreover, drawbacks of the precharge-based earlier reported circuits (which was cascading) are also taken care of by removing dependence among different CAM cells.

The advantage of this architecture is the design of larger word lengths with higher performance at a higher frequency of operation. Owing to the larger delay metric in PF-CAM, it is not useful for forming longer word lengths and cannot operate at a higher frequency of operation. Fig.3.2. illustrates the SCPF-CAM structure, which solves the deficiency of all the mentioned problems present in the precharge-based CAMs and improves the speed of operation compared to the PF-CAM architecture. An 8T CAM cell has been used as the basic block to design a word.

Two major contributions are made: 1) self-control operation, where the charge stored at the node S controls the ML transistors, thereby avoiding the dependence on previous ML value; and 2) the scheme eliminates the precharge phase to provide a higher search frequency. The SCPF-CAM is self-controlled; the node (S) value of the 8T CAM cell controls the evaluation logic and produces the output. If the search content matches the prestored data, then it passes a high value through M9; otherwise it passes a low value through M10 to the ML. The minimum operating voltage is limited to VTHP +2VTHN+VM. The voltage VM is mostly MLSA dependent and the most dominating among the three voltages. Transistor M9 is chosen to have a low threshold to push the supply voltage scaling limit.

The minimum amount of time required in the conventional CAM operation is

$$T_{total} = T_{write} + T_{precharge} + T_{search}. \quad (2)$$

The minimum amount of time required in the Self-controlled Precharge-Free CAM is

$$T_{total} = T_{write} + T_{search}. \quad (3)$$

V. COMPARATIVE ANALYSIS

Table 5.1: Comparative analysis on various content addressable memory architectures

AUTHOR	YEAR	ALGORITHM	ADVANTAGE	DISADVANTAGE
Pagiamtzis K et al	2003	Two techniques to reduce power consumption in content-addressable memories (CAMs). The first technique is to pipeline the search operation by breaking the match-lines into several segments. The second technique is to broadcast small-swing search data on less capacitive global search-lines, and only amplify this signal to full swing on a shorter local search-line.	Reduced power consumption.	High hardware complexity.
Lin C et al	2003	Precomputation based (PB) - content-addressable memory divides the comparison process and the circuitry into two stages. First stage counts the	Low power. Low cost. Low operating voltage.	The increase of the tag length affects the energy consumption, the delay, and complicates pre-computation stage.

		number of ones in an input and then compares the result with that of the entries using an additional content-addressable memory circuit that has the number of ones in the content-addressable memory -data previously stored. Second stage, a modified content addressable memory hierarchy is used, which has reduced complexity, and has only one pull-down path.		
Zukowski C et al	1997	The comparator or memory array is partitioned such that a small subset does a portion of each comparison calculation first, and each comparator in the main part of the array is only activated if still needed afterwards.	Reduces the search lines (SL) energy consumption by disabling the precharge process of SLs when not necessary. Reduces the match lines(ML) precharging, by segmenting the ML, selectively precharging the first few segments and propagates the precharge process if and only if those first segments match.	Delay increases number of segment increases.
Zackriya V. M et al	2016	The development of a CAM structure is carried out with a PRE signal, which ends up at a lower speed of search operation. In this drawback has been eliminated by removal of the PRE phase.Instead, they used control bits (CBs), which reduced the overall search time by one level.	Reduction in the number of SC paths Low power	Speed of search operation is reduced
TelajalaVenkataMahendra et al	2017	1) self-control operation, where the charge stored at the node *S* controls the ML transistors, thereby avoiding the dependence on previous ML value; and 2) the scheme eliminates the precharge	design of larger word lengths with higher performance at a higher frequency of operation. Dependence among CAM cells Increase in the	Slightly increase in power compared to the Precharge-Free CAM

		phase to provide a higher search frequency	search speed	

VI. CONCLUSION

In this paper, CAM and its application and basic operation related to it are introduced. Various cells of CAM mainly NOR cell and NAND cell and their match line structures are also discussed. This discussion is extended to these cells which are used to design a match line of CAM mainly the power consumption of CAM due to match line sensing techniques which are used to reduce the power consumption of CAM. This paper also reviews algorithm and architecture of a low power CAM. In addition other CAM architectures and a comparative study are also included here. As a resultof the analysis, Precharge-Free CAM reduce the power with the high search speed. In future, many techniques can be used to design Low power Precharge-Free CAMs.

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