High Speed Full Adder Design with Analog Switch Level Restoration Technique.

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Abstract: In the field of very large scale integration (VLSI) till date there are a plenty of 1-bit full adder. In this paper we have implementation the comparative analysis of 16 transistors Transmission function full adder circuit (TFA) and 20 transistors modified conventional full adder circuit. And we compare with different pass transistors for the decrease the count of transistors considering various elements in like power, delay and power delay product .These constraints are calculated by using cadence virtuoso platform in 180nm Technology. The full adder is part of the processor we can increases the n-bit full adder to implement the complex circuits.

Index Terms **- Full adder circuits, cadence virtuoso tool and Transistor count**.

I. INTRODUCTION

Many paper are in the VLSI filed most of publication in low power consumption and count of the transistors decrease the area of the chip. So In this paper a brief description of Transmission full adder and modified conventional full adder. But at the circuit level an optimized design is desirable have less number of transistor and decreasing the power and reducing the delay. There are different types of CMOS technology in vlsi like Transmission gate (TG), Pass-transistors logic (PTL) , complementary pass transistors logic (CPL) dual rail domino logic and gate diffusion input (GDI) but all types have the pros and cons. The threshold problems are logic 1 is not the value of v_{dd} and logic 0 is not value of zero. The threshold problems are reduced by using different levels of restoration factors. Many in this paper suggests a classification and clarifies the circuits of full adder single-bit adders based on 16 transistors and 20 transistors modified conventional CMOS full adder with reduce the low power and high speed. The comparative analysis has been carried out according to the simulation results of single-bit circuits are based on them taking into account the input currents at the same output load [1]. Recommendations on the use of circuits are given below.

Transmission gate full adder design

The Implementation of this full adder is realized by Reusing the C_{out} term in the sum term as a common sub expression. The logic function for this implementation are,

$$sum=A\oplus B\oplus C_{in} \quad (1)$$

$$C_{out}=(A\oplus B).C_{in}+A.B \quad (2)$$

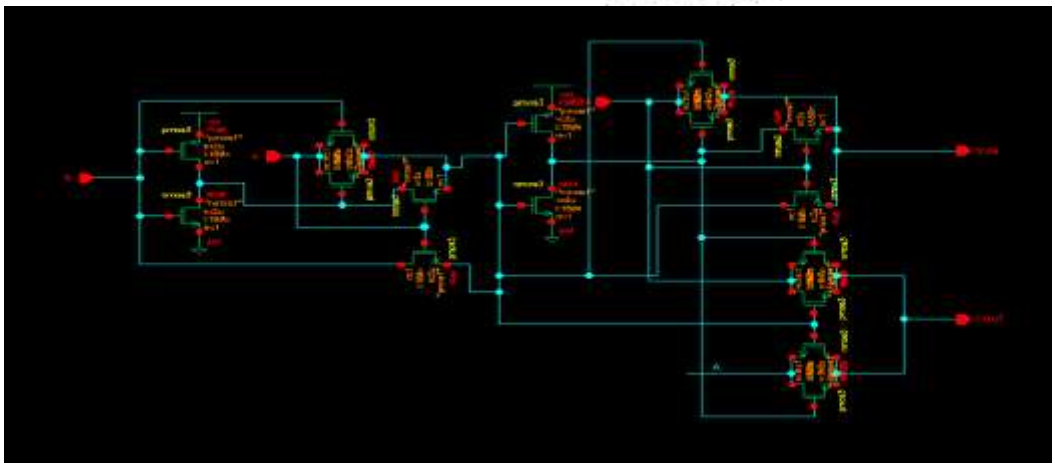

Figure1: Transmission Function Full adder (TFA)

In order to further simplify the full adder which is the fundamental unit of the arithmetic unit, a CMOS full adder based on the transmission function theory called as the transmission function adder (TFA), was developed as shown in above figure 1 . The TFA shown in above figure consists of 16 transistors [2] and dissipates less power than that of the conventional CMOS full adder.

The below circuit shows the modified conventional CMOS full adder in the figure 2 consists of 20 transistors are required compare to above transmission full adder the with increase of two transistors more it decrease the power and delay. The main problem of this modified circuit is its critical delay that limits the performance of the system. This problem is worse when two or more full adder circuit are cascaded together to perform multiple-bit addition. With drain diffusion area and Source diffusion area of NMOS 440f and PMOS 480f. Different parameters are differing in below the table.

II. Design of conventional CMOS Full adder

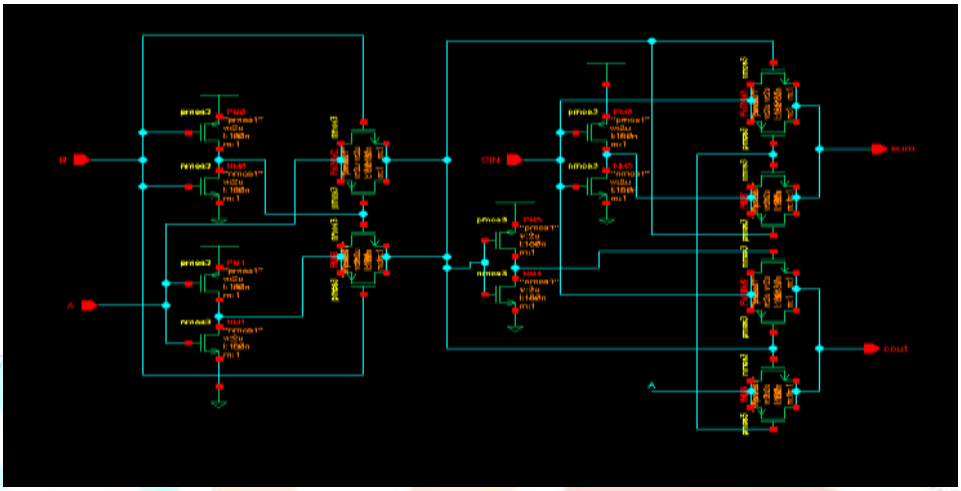

Figure2: Modified Conventional CMOS Full adder (MCFA)

In the cmos adder architectures multiple bit addition can be as simple as connecting several full adders in series or it can be more complex [3]. The 20 transistors full adder was designed using a transmission gate it produced for both the sum and carry with proper polarity the xnor and xor are used to generate the sum and cin again cin input is multiplexed which can simultaneously inputs are used to generate sum and cout

$$Cout = A.B+Cin\ .\ (A+B)$$

$$Sum = A.B.Cin + (A+B+CIn).Cout\ bar$$

$$= A.B.Cin + (A+B+Cin).\ (A.B.+Cin.(A+B))\ bar$$

The Equivalence gates of (XNOR/XOR) are realized using full swing restored complementary MCFA and sum and count expressions are realized in the below circuit diagram these are alternate structures of full adders are as shown below

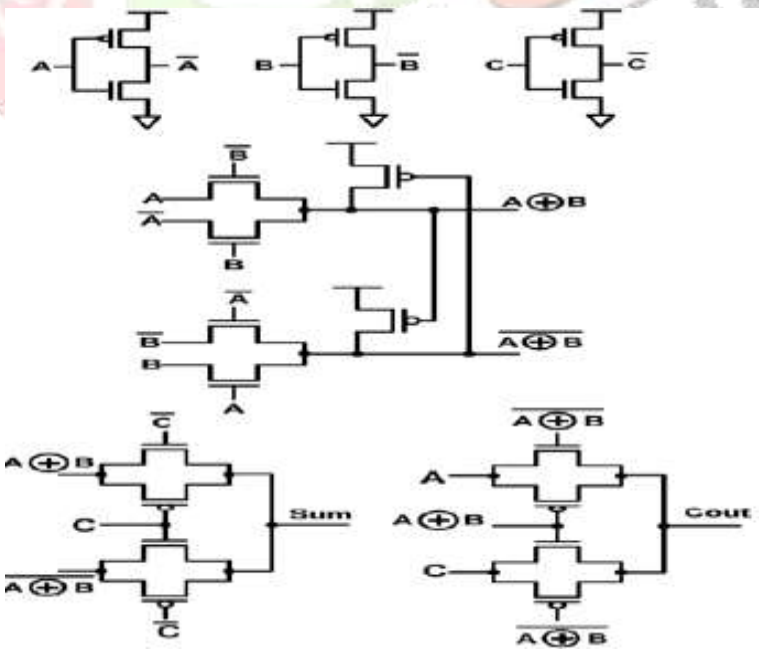

Figure3: Alternate circuit diagrams of Full adder

The different full adder circuits have the two states ON state and OFF state when all inputs are zero the SUM and Cout will be zero when all inputs are high then the sum and carry are in High[4,5]. The truth table is shown below.

Table1: Truth table of a full adder

Cin	A	B	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

In the below table shows the default properties of transistor in cadence design tool[6] to decrease the power to the make the IC to low power vlsi we can make the concept of transistor sizing to implement the less power consumption to the system. The results are shown below for double pass transistor and complementary pass transistor, Transmission function full adder circuit and Modified Conventional CMOS Full adder.

Tabel2: Properties of Transistor in cadence virtuoso tool

Model name	NMOS	PMOS
Length	180n M	180n M
Total width	2u M	2u M
Threshold	800n M	800n M
S/D metal width	400n M	400n M
Drain diffusion area	440f	480f
Source diffusion area	440f	480f
Drain diffusion area periphery	2.8u M	2.8u M
Source diffusion periphery	2.8u M	2.8u M

Table3: Results For average power and average Delay

S.No	Average Power	Average Delay
TFA	$696.0E^{-6}$	$47.78E^{-12}$
CPL	$410.0E^{-6}$	$62.01E^{-12}$
DPL	$248.0E^{-6}$	$28.15E^{-12}$
MCFA	$246.0E^{-6}$	$4.789E^{-12}$

The simulation results are taken as reference from [19-23]. In the below table shows the default properties of transistor in cadence design tool[7-10] to decrease the power to the make the IC to low power vlsi we can make the concept of transistor sizing to implement the less power consumption to the system[8-15]. The results are shown below for double pass transistor and complementary pass transistor[16-18], Transmission function full adder circuit and Modified Conventional CMOS Full adder.

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Results: The transient response output waves are eradicated by cadence virtuoso tool as shown in below

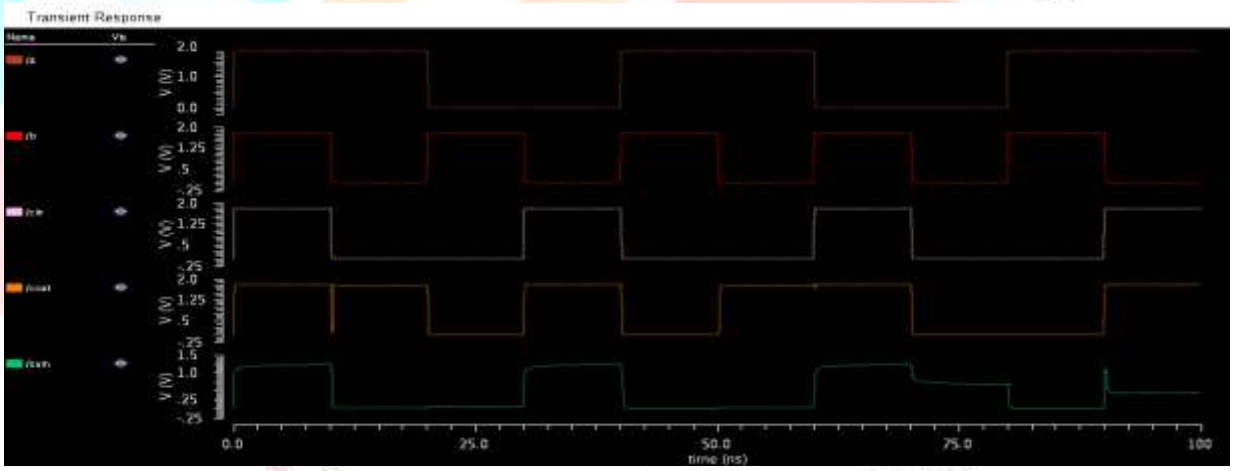

Figure4: TFA Wave Forms

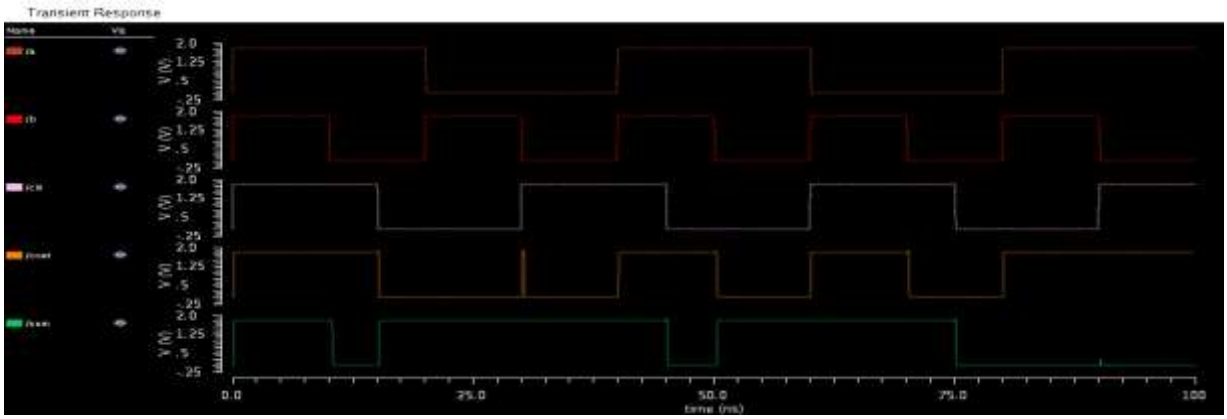

Figure5: MCFA Wave forms

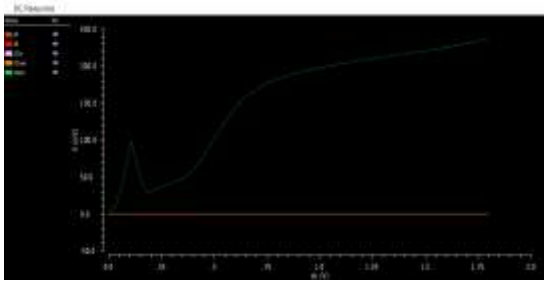

Figure6: DC-Characteristic of TFA

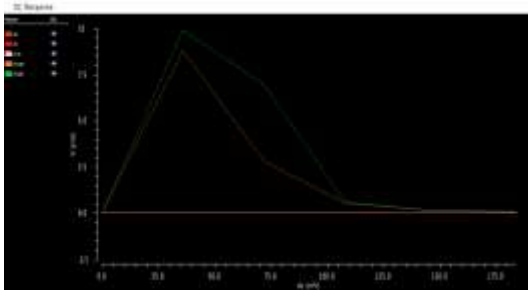

Figure7: DC-Characteristic of MCFA

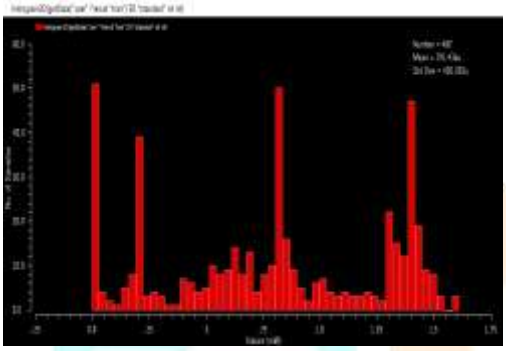

Figure8: average power histogram for MCFA

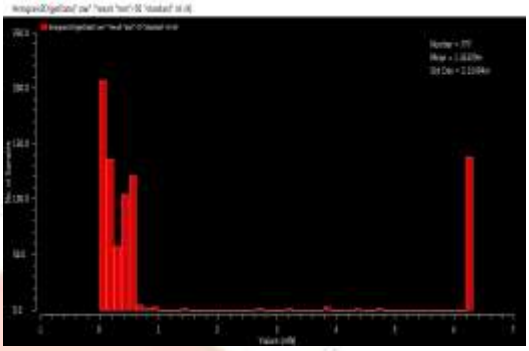

Figure9: average power histogram forTFA

Histogram for the modified conventional full adder diagram the indication of mean and standard Deviation by taking the x-axis on values mW and on Y-axis No of samples are taken

III. Conclusion

In this paper we are completed on cadence virtuoso tool and calculated the power and delay the circuit to the count of the transistor and the performance is calculated with several 1 bit full adder circuits. The full adder architectures are using in the microprocessor for the resulting the high performance

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