Stability Analysis of SRAM on Trip Point

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Abstract: The most important property of an SRAM cell is its ability to hold data under varying conditions. This property is commonly referred to as the stability of the cell. In this paper we describe this property of SRAM. The data stability affects by the various parameters like supply voltage, cell ratios, threshold voltages, and static noise sources, etc. This paper investigates the concept of SRAM cell data stability from the traditional approaches like trial and error technique.

Index Terms - Static Noise Margin, SRAM, VLSI, CMOS.

I. Introduction

As the year progresses, technology changes. In the initial level the main purpose was computation the things in accurate manner. Before the computer age, the computation was the toughest work. After abstain out this problem, new challenges began to come. More Challenges Increasing Day by day like speed, power consumption, delay and many more. At the time of desktop PC design era mainly focused on optimizing speed, because there were computationally intensive real-time functions such as video compression, gaming, graphics etc.

The most important property of an SRAM cell is its ability to hold data under varying conditions. This property is commonly referred to as the stability of the cell. This chapter discusses the theory of stability and analysis of stability on different points. Traditional approaches of data stability of SRAM cell are functions of static parameters such as supply voltage, threshold voltages, and static noise sources, etc. The conventional measure of the static d-stability of an SRAM cell is based on the static noise margin (SNM).Static Noise Margin (SNM) is the most important parameter for memory design. SNM, which affects both read and write margin, is related to the threshold voltages of the NMOS and PMOS devices of the SRAM cell that is why we have analyzed SNM with the Read Margin, Write Margin and also the Threshold voltage [1].The SNM is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. A basic understanding of the SNM is obtained by drawing and mirroring the inverter characteristics afterwards draw the Butterfly curve to find out the maximum square between them [2].

Noise margin can be defined using the input voltage to output voltage transfer characteristic (VTC). The noise margin is a value of noise which can be a accepted by the device while operation does not affected [3]. If the consequences of the noise applied to a circuit node are not latched, such noise will not affect the correct operation of the system and can thus be deemed tolerable. It is assumed that noise is present long enough for the circuit to react, i.e. the noise is “static” or dc. A Static Noise Margin is implied if the noise is a dc source. In case when a long noise pulse is applied, the situation is quasi-static and the noise margin asymptotically approaches the SNM [4].

II. Simulation Techniques for Data Stability Analysis

Simulation set up: In trial and error technique introduced two voltage sources between inverters. Two technologies 180nm and 65nm are used for simulations. In graphical technique SNM is calculated by using butterfly curve. Simulations are done on different SRAM circuits.

Tools used: Tanner EDAv13

S-edit is used for drawing circuit diagram. Simulations are done by using T-SPICE. This tool is the main tool to do all the simulations on different technology. By the help of W-edit we can see the waveforms.

Technology used: 65nm

Basic Trial and Error Technique

(a)Introduction of Technique

It is a basic technique, in which we find minimum noise voltage to flip the state of the cell. In this technique, we introduced two voltage sources between one inverter inputs to second inverter output as depicted in Figure 4.5 and s-edit circuit diagram is shown in Figure 4.6. Initially, noise source voltage is set to zero to check states; observed states are the same which were defined previously. Then, increase the noise voltage source for checking the states. The circuit remains stable until the states are same and the least noise voltage at which it upturns the state of the cell.

From this approach, the voltage which shows the deviation in the states of the cell is observed

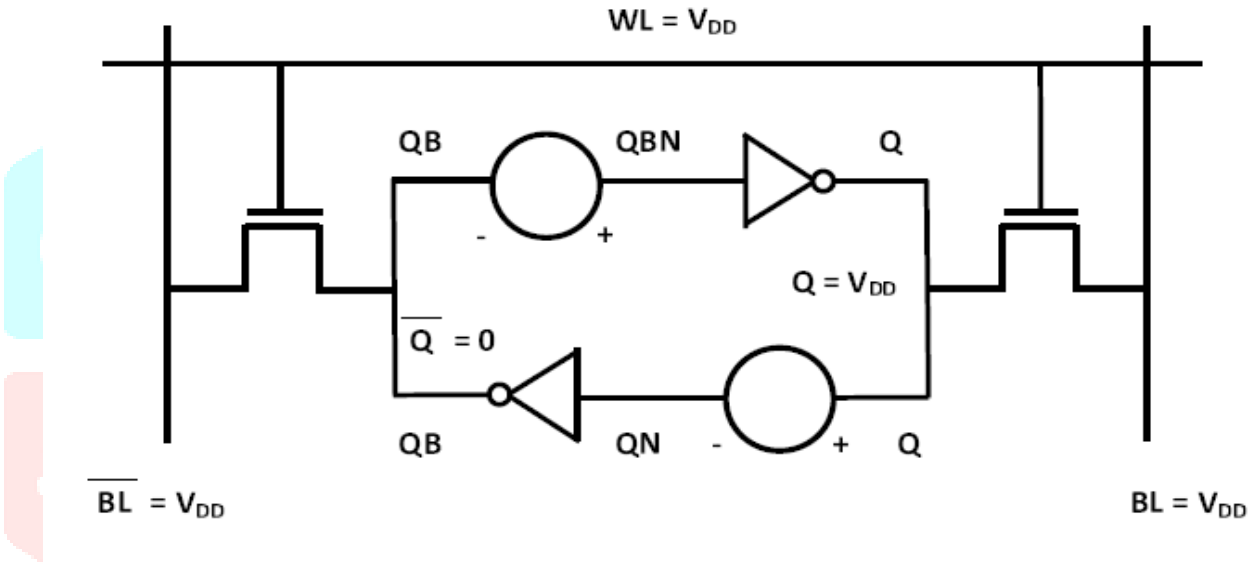


Figure 1 Basic Trial and Error technique with two noise sources

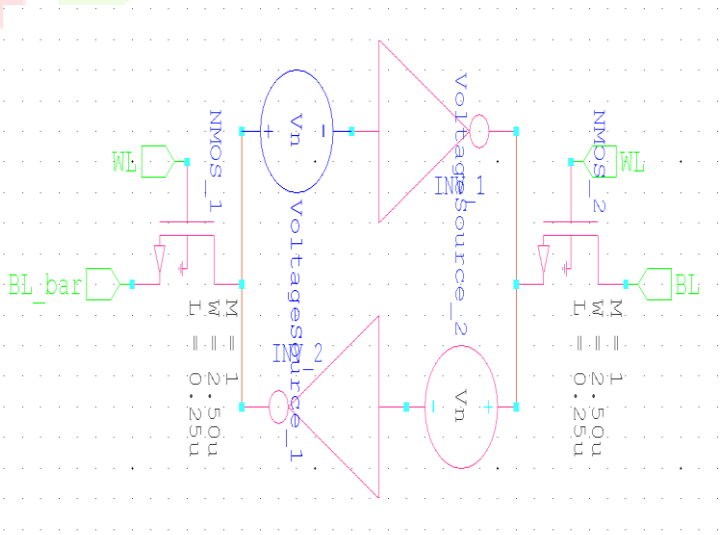


Figure 2 Noise voltage source induced for trial and error technique

(i)Conventional and ground gated 6T SRAM cell

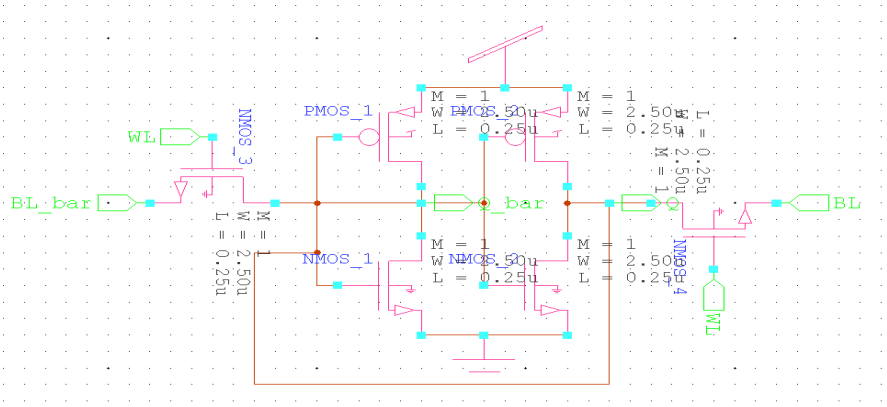
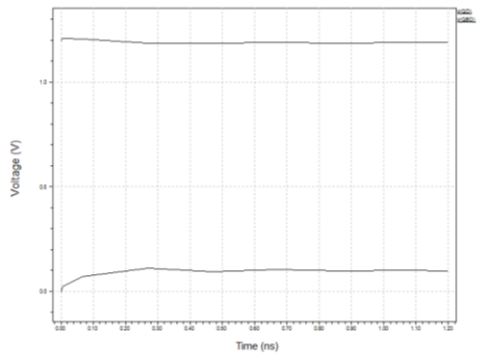


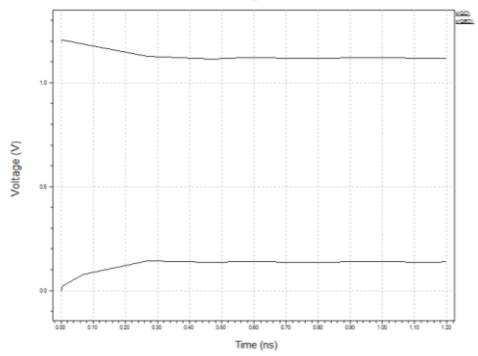
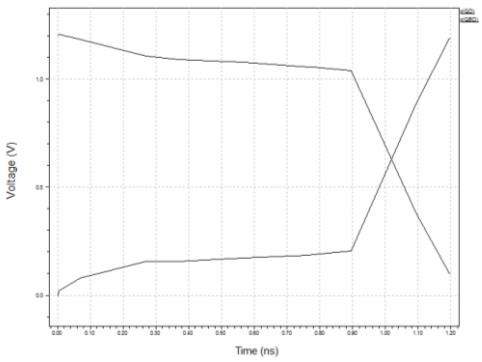
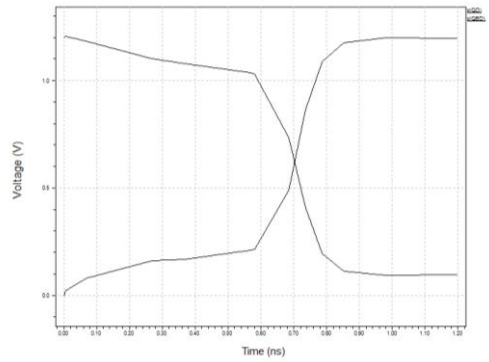
Figure 3 Conventional 6Transistor SRAM cell circuit diagram

The 6T SRAM cell consists of two access transistors (NMOS_3 and NMOS_4) connected with complementary bit lines and two cross-coupled CMOS inverters as illustrated at Figure 3. The PMOS transistors are called the pull-up transistors (PMOS_1 and PMOS_2) and the NMOS are called driver transistors (NMOS_1 and NMOS_2). The two inverters are connected in feedback loop so as to stabilize it into respective states. Due to this feedback loop, a high value on the second transistor is generated when first is fed with a low thereby storing the current logic value. The access transistors, bit lines (BL and BL_bar) and word lines (WL) are used to perform read and write operations of the cell, respectively. To write information, the data are imposed over the bit line (BL) and inverse bit line (BL_bar) and the word line (WL) is kept high for turning on the access transistor. For the data to be stored in the cell the word line (WL) is kept low thereby making the transistors off. The data stored in the cell can be read by triggering the access transistors, i.e., by making it high. Since a single bit line (BL) is used for read operation, read stability can therefore be improved by strengthening the driver transistor [1].

(b)Trip point at technology 65nm: Simulation is done using 65nm technology, which shown in Table I

Table I States of the Output on different Noise Voltage Source on 70 nm

S.No.	Noise Source	Simulation Result (initially: Q=Vdd and Q_bar=0)
1.	.25	

	.32	
	.335	
	.34	

6T SRAM cell with ground gating:

In this circuit two extra transistors NMOS and PMOS are added at the ground, illustrated at Figure 4. The detailed description is available in chapter4

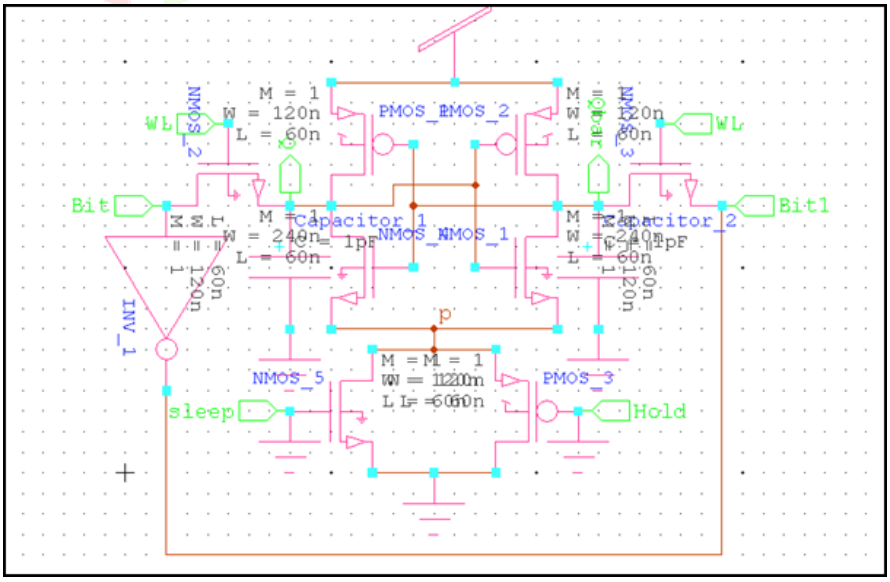
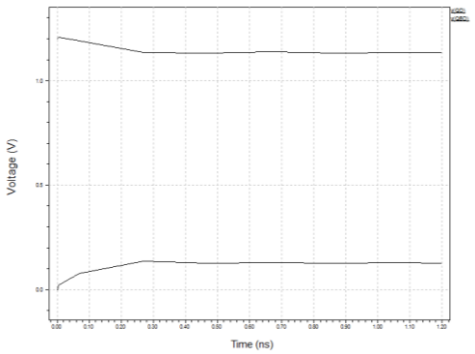
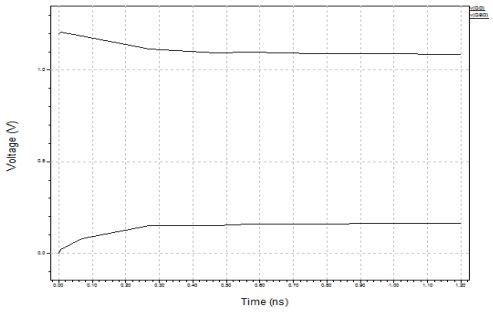
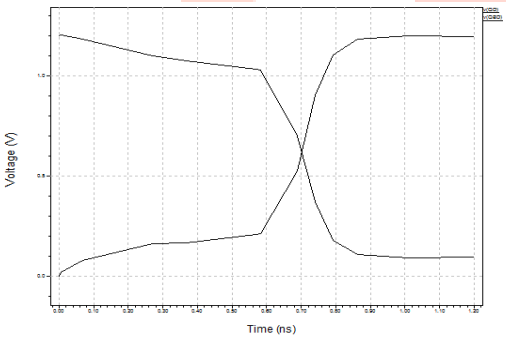
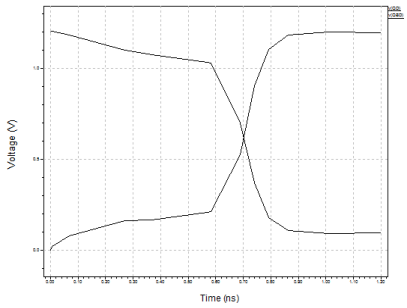


Figure 4 Conventional 6T SRAM with header and footer

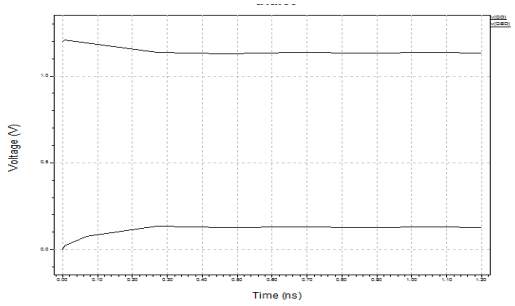
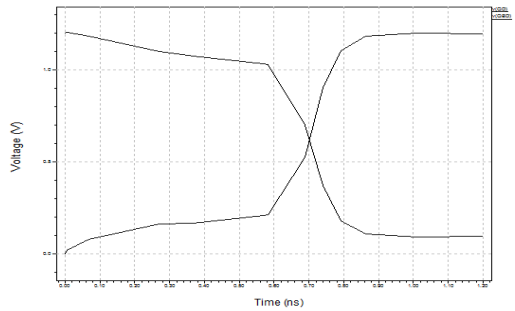
Simulation of Active mode: In this operation write signal is enabled. The driver transistor goes in active mode. Table II shows the results for finding trip point voltage.

Table II States of the Output on different Noise Voltage Source on active mode

S.No.	Noise Source	Simulation Result (initially: Q=Vdd and Q_bar=0)
	.31	
	.33	
	.34	
	.35	

Simulation of Sleep mode: When circuit is in off condition, data should remain same as store in write operation. But due to some noise data may vary. So from table III find out the trip point from variation of noise source.

Table III States of the Output on different Noise Voltage Source on sleep mode

S.No.	Noise Source	Simulation Result (initially: Q=Vdd and Q_bar=0)
1.	.31	
2.	.34	

(ii)Asymmetrical 8T SRAM cell with ground gating:

The conventional 6transistor SRAM cell can all the functions of memory like write, read and hold operation. But there is many parameters affect the operation. So introduced extra transistors to overcome the defaults. In this circuit diagram two transistors are added as depicted in Figure 5. One transistor is added two separate read and write operation and other is added to avoid direct connection of driver transistor to ground[5].

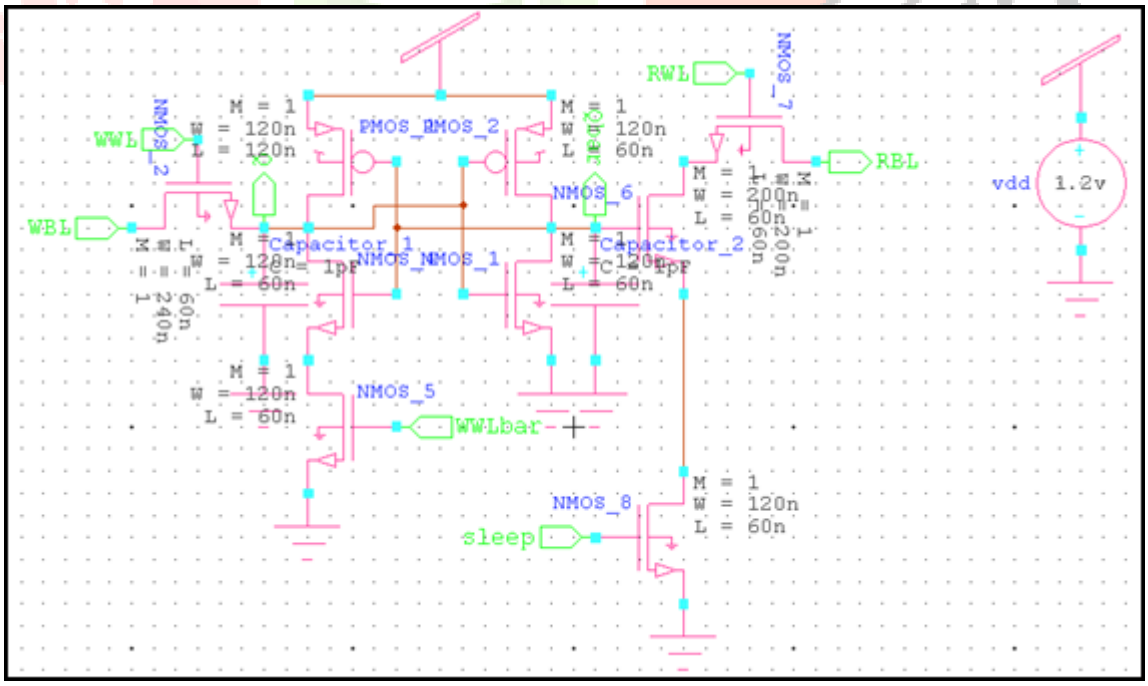
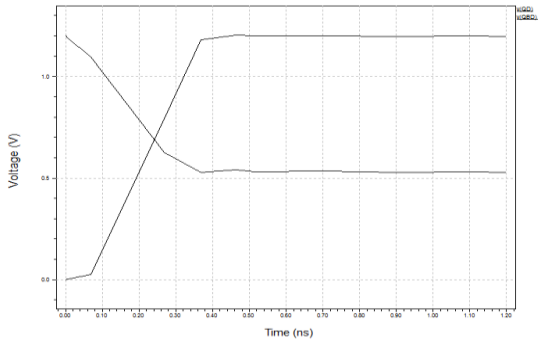
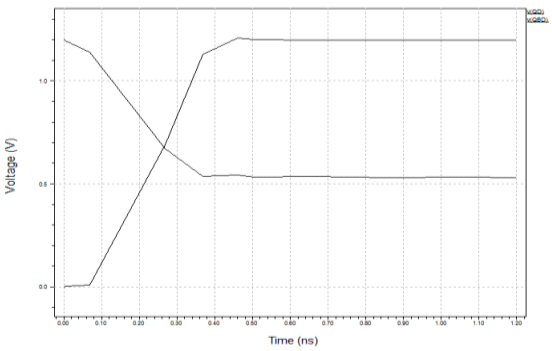
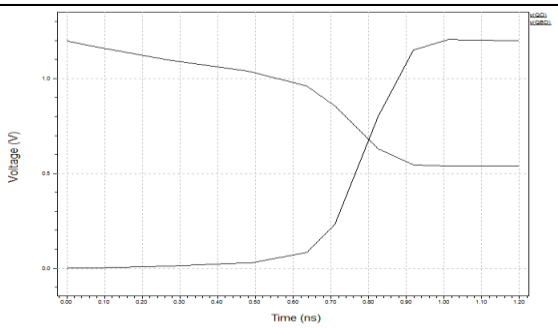
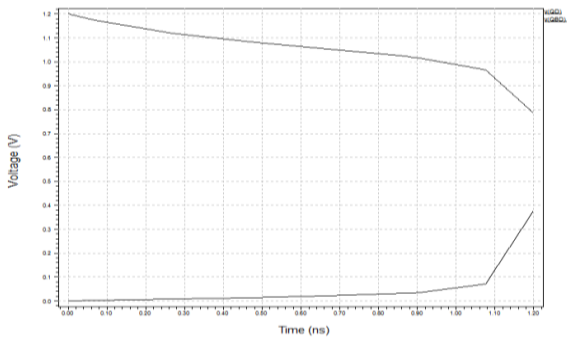


Figure 5 Asymmetrical 8T SRAM cell

Table IV States of the Output on different Noise Voltage Source of Asymmetrical 8T SRAM cell

S.No.	Noise Source	Simulation Result (initially: Q=Vdd and Q_bar=0)
1.	0.46	
2.	.43	
3.	.39	
4.	.38	

(iii)Asymmetrical 9T SRAM cell:

As discussed in the previous circuit diagram the transistors are adding to suppress the defaults, one more extra transistor is added between power supply to PMOS as illustrated in Figure 6. This transistor avoids the direct connection from power supply.[5]

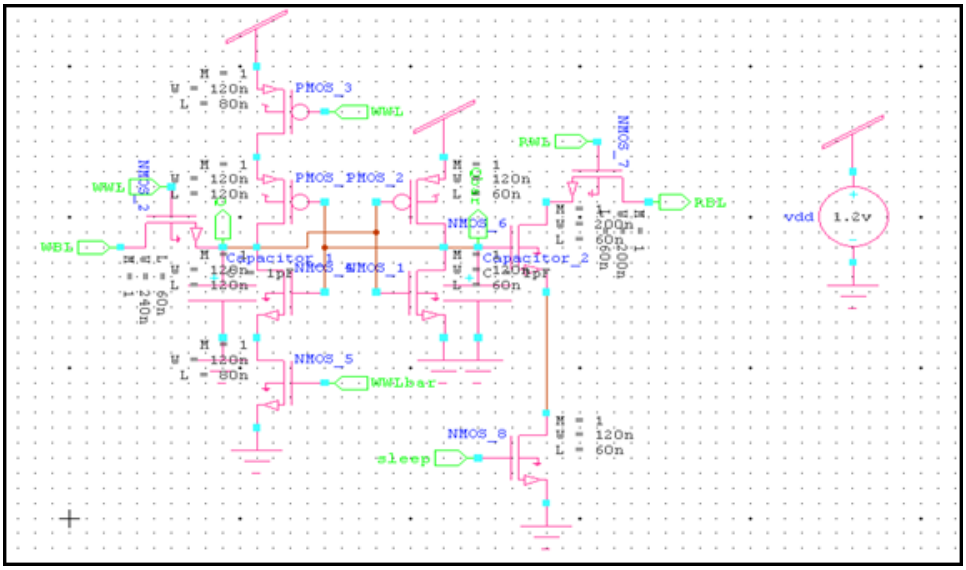
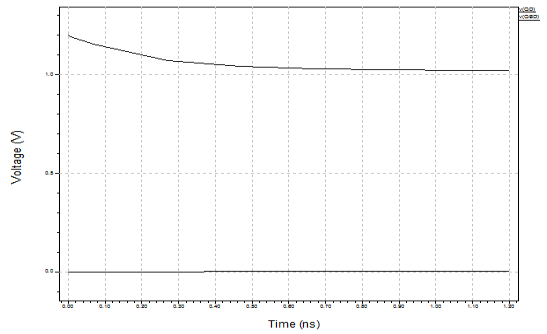
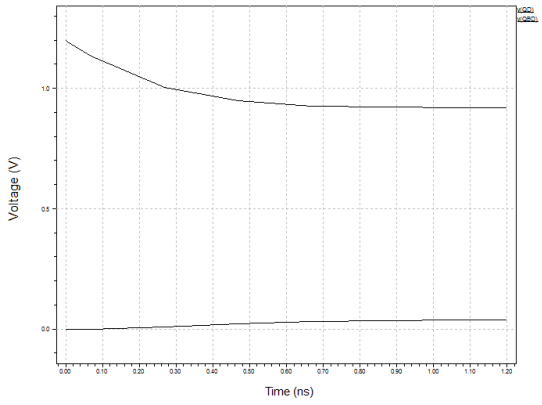
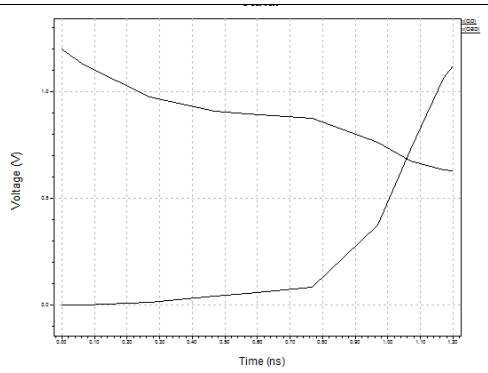
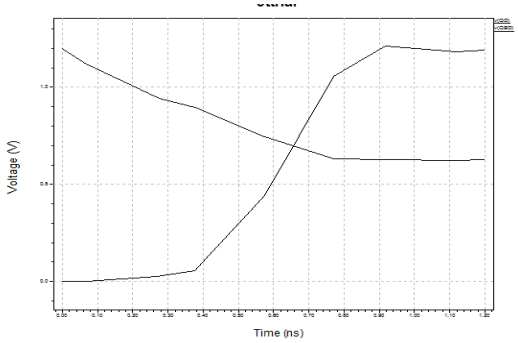


Figure 6 Asymmetrical 9T SRAM cell

The noise source is connected between two inverters as connected in 6T SRAM. Initially output sets 'Vdd' and '0' volts. Noise source starts from '0' and varies until output flipped out. Table V shows the output against the changes of noise source.

Table V States of the Output on different Noise Voltage Source of Asymmetrical 9T SRAM cell

S.No.	Noise Source	Simulation Result (initially: Q=Vdd and Q_bar=0)
1.	.25	
2.	0.28	

3.	0.29	
4.	0.30	

III. Conclusion: In this paper we analysed the concept of stability on different noise source voltage.Table I represents initially states of the cell at zero voltage. At 335 mv noise voltage source, states are flipped. Hence 6T SRAM cell is stable below 335 mv.Table II represents initially states of the cell at zero voltage. At 340 mv noise voltage source, states are flipped. Hence ground gated 6T SRAM cell is stable below 340 mv.From Table III the data can flip at 340mv.Below that value output is same as written during write operation.From Table IV,it is clear that output of 8T SRAM is flipped out at 460mV.From Table V,it is clear that output of 9T SRAM is flipped out at 300mV.From the above results 9T asymmetrical SRAM cell is stable on below voltage.

IV. ACKNOWLEDGEMENT

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