A PFC based improved three-level ZVS AC-DC converter with single phase AC source

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Abstract — In this paper we propose a PFC (Power Factor Correction) integrated improved three level ZVS DC-DC converter with high frequency operationfeeding from a single phase AC source. The rectifier stage is composed of four diodes in the center-tapped rectification. On the primary side of the transformer, the two transformers are connected in series. The middle node of the two transformers is connected to the neutral point of the split flying capacitors. Because it cooperates with the four-diode rectifier stage, the circulating current on the primary side of the transformer decays to zero during the freewheeling period. The zero-voltage switching (ZVS) of the leading switches is determined by energy stored in the output filter inductor, which is similar to the conventional TL converter. The output voltage comparison with input voltage and efficiency calculations are done with respect to change in load torque and the results are presented in MATLAB Simulink software.

I. INTRODUCTION

In order to extend the ZVS of lagging switches, an external inductor in series with the primary winding of the transformer is employed [2]. However, the inductor leads to a large duty cycle loss and a large ringing of the secondary rectifiers. An LC network with an inductor and two capacitors is used to achieve wide ZVS [4]. However, the additional inductor causes additional large Circulating currents. An additional inductor with two clamping diodes can be used to achieve ZVS for lagging switches, and overshoot for secondary rectifiers can be suppressed [5]. Nevertheless, it still results in large duty cycle loss. Another approach for achieving ZVS for lagging switches is to enhance the magnetizing current to charge and discharge the junction capacitors by using two coupling inductors integrated in one core [6]. Besides, a TL converter achieving the ZVS for all switches is proposed in [7] by using two series-connected transformers. For the sake of extending the ZVS range for lagging switches, a TL dc–dc converter with an auxiliary coupling inductor at the primary side is reduced [8]. The energy stored in the auxiliary circuit is minimal at full loads and gradually increases as the load current decreases. However, large circulating currents still freewheels at the primary side. Resonant TL dc–dc converters have been proposed to regulate the output voltage with high efficiency by modulating the switching frequency[9]–[11]. However, the switching frequency may vary in a wide range especially at the light loads, which makes the magnetic components and EMC design difficult. In order to overcome the drawback of wide switching frequency variation in conventional resonant converters, phase-shift control is extended to the resonant TL dc–dc converter [12]–[14].

In order to reduce the circulating current and conduction loss, a blocking capacitor is used to reset the primary winding current. In order to avoid the current flowing to the reverse direction during the freewheeling period, two diodes are series connected with the lagging switches [15]. Although the circulating current can be reduced, the conduction loss may not be optimized because of more conduction loss caused by the two additional diodes. Furthermore, the lagging legs will lose the ZVS conditions. Therefore, insulated-gate bipolar transistor (IGBT) can be used for lagging switches to achieve zero voltage and zero current switching (ZVZCS). For ZVZCS TL dc–dc converters, MOSFETs are used for leading switches to achieve ZVS, and IGBTs are used for lagging switches to achieve ZCS. However, using IGBTs limits the switching frequency of the converter and the power density cannot be high. Most of the researches on TL dc–dc converter focus on HB TL dc–dc converters. Full bridge (FB) TL dc–dc converters are investigated, but there are still some disadvantage to achieve soft switching, high efficiency, and high-frequency operation for the FB TL dc–dc converters.

In this paper, a hybrid TL and HB dc–dc converter with reduced circulating current and output filter inductance is proposed. A blocking capacitor is used to decay the primary circulating current. However, the lagging leg switches also can achieve ZVS by using the magnetizing inductor current of the HB transformer. At the secondary side of the transformer, a novel rectifier circuit configuration composed of four diodes is proposed, which forces the circulating current decreasing and equaling to zero instead of flowing to the opposite direction during the freewheeling period. The rectifiers of the hybrid converters are the same circuit, which is actually a center-tapped full waveform rectifier. Although the proposed converter has more diodes at the rectifier stage, the conduction loss at the secondary side is not increased. Due to the two more diode at the rectifier stage, the reverse flowing path at the primary side during the freewheeling period is cut off. Therefore, the diodes connected with lagging switches are unnecessary.This paper is organized as follows. The circuit and mode operation of the proposed converter is described in Section II. In Section III, the main features of the proposed converter are analyzed. The design simulation of the converter is presented in Section IV.

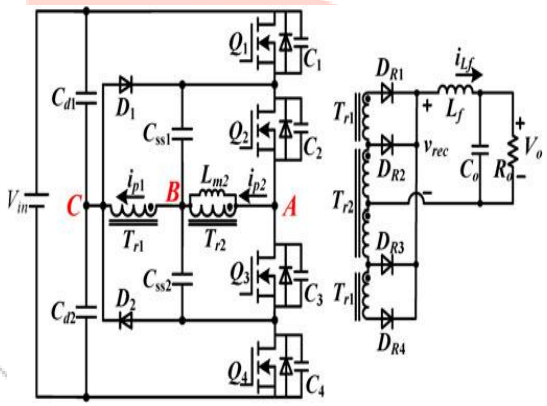

Fig. 1: Proposed converter

II. OPERATION OF PROPOSED CONVERTER

There are eight working stages in each half-switching period.

Stage 1([t0,t1]) [see Fig. 2]:Prior to t0, Q1, and Q3 are on, and Q2 and Q4 are OFF. The primary current in T r 1 stays at zero. The primary current in T r 2 is negative. The output filter inductor current flows through DR3 . At time t0, Q3 is turned OFF.

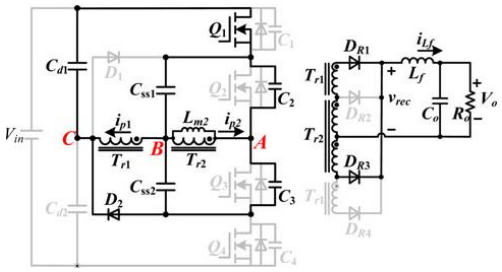

Fig. 2: Stage 1 operation

Stage 2 ([t1,t2]) [see Fig. 3]: At time t1, the drain-source voltage of Q2 reaches zero, and ip2 flows through the body diode of Q2. ip1 and ip2 both increase linearly. The blocking capacitor voltage vCb is charged by ip1 . Q1 and D2 still conduct to charge the flying capacitors Css1 and Css2.

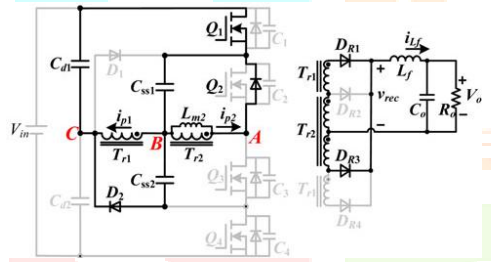

Fig. 3: Stage 2 operation

Stage 3 ([t2,t3]) [see Fig. 4]:Attime t2, Q2 is switched on with ZVS. iLf keeps on freewheeling through DR1 and DR3 . ip1 and ip2 still increase linearly as expressed in (2).

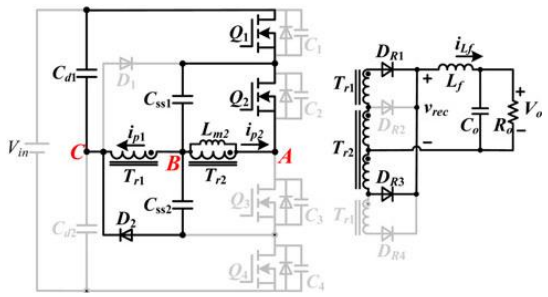

Fig. 4: Stage 3 operation

Stage 4 ([t3,t4]) [see Fig. 5]: At time t3, DR3 is reverse biased and all the filter inductor current flow through DR1 .TheTL transformer and the HB transformer transfer energy to the output.

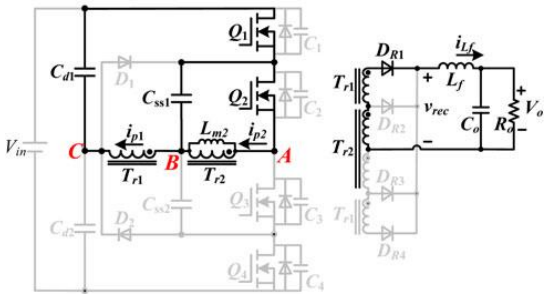

Fig. 5: Stage 4 operation

Stage 5 ([t4,t5]) [see Fig. 6]: When Q1 is turned OFF at t4, the voltages across the junction capacitors C1 and C4 are charged and discharged linearly by the energy stored in the output filter inductor Lf .ip1 starts to decrease, so the current inDR1 decreases and the current in DR2 increases.

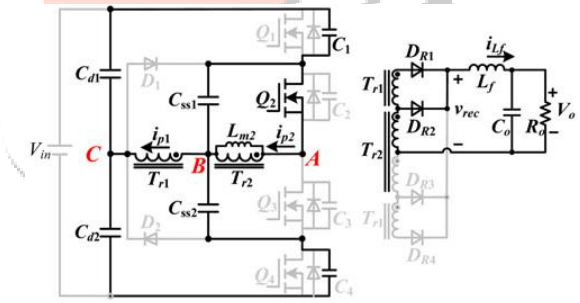

Fig. 6: Stage 5 operation

Stage 6 ([t5,t6]) [see Fig. 7]: When C1 reaches Vin/2 and C4 reaches zero, the body diode of Q4 is forward biased. ip1freewheels through D1 and Q2. The voltage across Cb is applied to the primary winding of T r 1 , which forces ip1 to decrease rapidly.

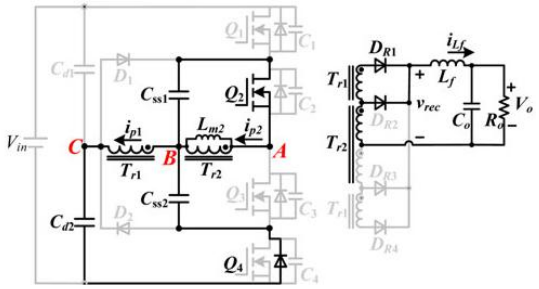

Fig. 7: Stage 6 operation

Stage 7 ([t6,t7]) [see Fig. 8]:Attime t6, Q4 is turned ON with ZVS. The primary winding current of T r 1 continues decreasing and freewheels through D1 and Q2. The current in DR1 continues reducing and the current in DR2 continues increasing.

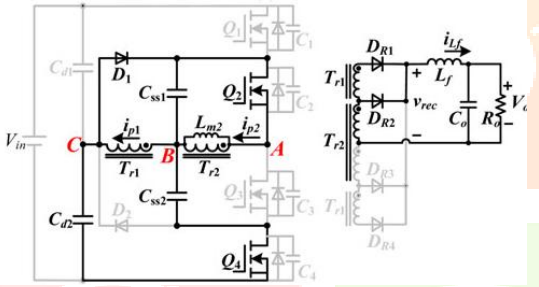

Fig. 8: Stage 7 operation

Stage 8 ([t7,t8]) [see Fig. 9]: Stage 8 starts when ip1 decays to zero. D1 and Q4 still conduct to charge flying capacitors Css1 and Css2. Then DR2 carries all the filter inductor current, and DR1 and DR4 are reverse biased. Therefore, the flowing path of the secondary current in T r 1 is blocked. The filter inductor current only can flow through DR2 and the secondary winding of T r 2 .

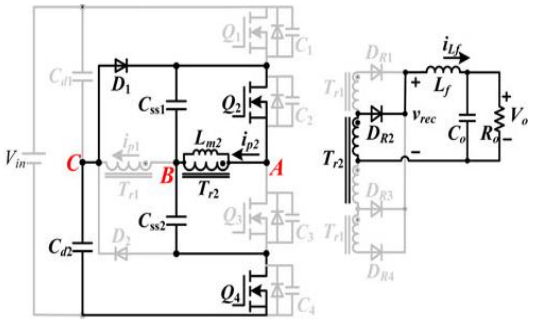

Fig. 9: Stage 8 operation

III. PFC CONVERTER

Two stage PFC converters are widely in practice in which first stage is used for the power factor correction which is preferably a boost converter and second stage for voltage regulation which can be any converter topology depending upon the requirement [7]. This two stage topology is complex and results in higher cost and more losses; hence a single stage Zeta converter is proposed in this paper which is used for DC link voltage control and power factor correction. The operation is studied for a Zeta converter working in DICM (Discontinuous Inductor Current Mode) hence a voltage follower approach is used. A voltage follower approach requires a single voltage sensor for the DC link voltage regulation while in case of CCM (Continuous Conduction Mode); current multiplier approach is normally used [8].

The proposed scheme maintains high power factor and low THD of the AC source current while controlling rotor speed equal to the set reference speed. A voltage follower approach is used for the control of Zeta DC-DC converter operating in DICM. The DC link voltage is controlled by a single voltage sensor. Vdc (sensed DC link voltage) is compared with Vdc* (reference voltage) to generate an error signal which is the difference of Vdc* and Vdc. The error signal is given to a PI (Proportional Integral) controller to give a controlled output. Finally, the controlled output is compared

with the high frequency saw tooth signal to generate PWM (Pulse Width Modulation) pulse for the MOSFET of the Zeta converter. A rate limiter is used to limit the stator current during step change in speed.

The duty ratio D for the Zeta converter (buck-boost) is given as [7],

D = Vdc / (Vin + Vdc) (2) where Vdc represents the DC link voltage of Zeta converter.

If the permitted ripple of current in input inductor Li and output inductor Lo is given as åiLi and åiLo respectively, then the inductor value Li and Lo are given as [8-11],

Li = D.Vin / {fS.(åLi)}

For the critical conduction mode,
åiLo = 2.Idc

i.e. Lo(critical) = (1-D) Vdc / {fS. (2.Idc)}

C1 = D.Idc / {fs. (VC1)}

Cd = Idc / (2.À.Vdc)

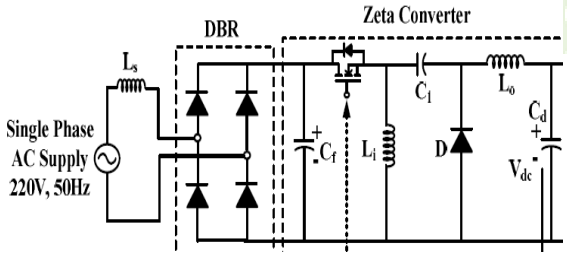

Fig. 10: PFC converter

IV. SIMULINK RESULTS AND OUTPUTS

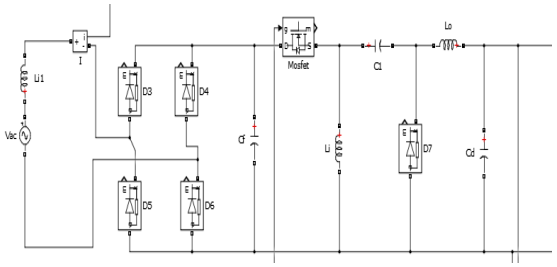

Fig. 11: Simulink modeling of PFC converter

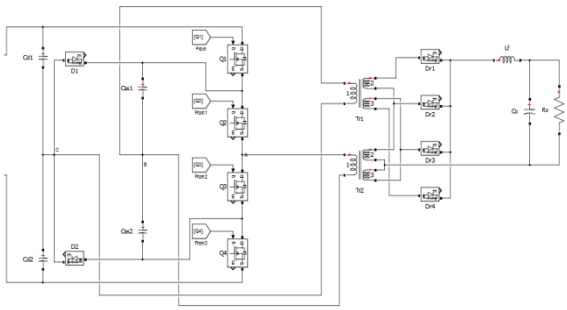

Fig. 12: Proposed DC-DC full bridge converter

The above are the simulink models of proposed converter with PFC circuit. The circuit is spilt to two catagories, PFC circuit Fig. 11 and DC-DC full bridge converter Fig. 12.

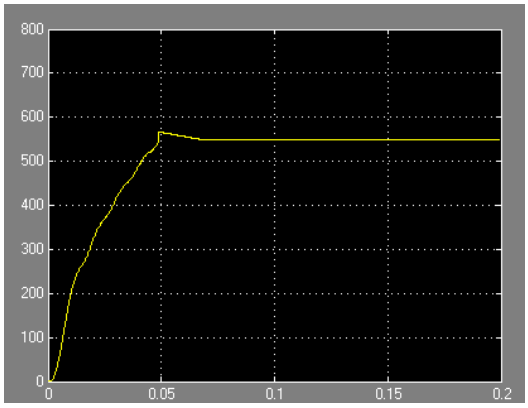

Fig. 13: Output voltage of PFC converter

The above graph is the output voltage of the PFC converter with transient at the inital

condition and reduced ripple output with 550V as given in reference value. The output voltage of the PFC converter changes with respect to reference value given by the user.

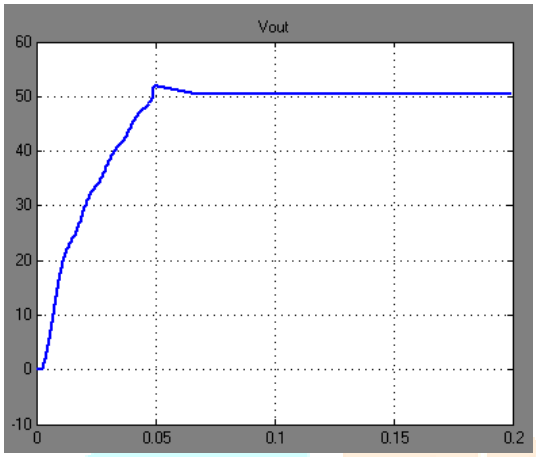

Fig. 14: Output voltage of full bridge converter

FIg. 14 shows the output voltage of DC-DC full bridge converter with reduced votlage to 50V from 550V feeding a resistive load with heavy power cosumption of 1kW. The votlage is very stable with lowest ripple even in heavy load conditions.

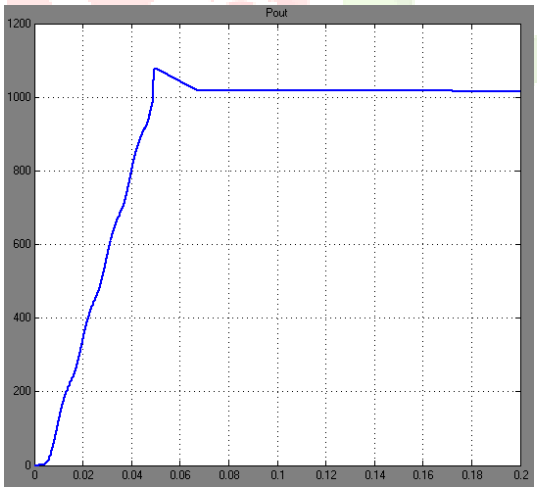

Fig. 15: Output power at load

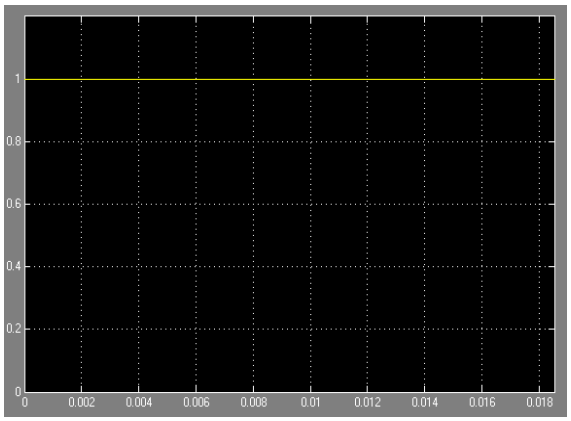

Fig. 16: Power factor of source

The power factor of the input AC source is maintaned at '1' which is said to be unity power factor with feeding a heavy resistive load of 1kW.

V. CONCLUSION

In this paper, a hybrid TL and HB dc–dc converter by sharing the lagging switches to reduce the circulating current and output filter inductance is proposed for higher efficiency. Since the switches only undergo half of the input voltage, the proposed converter is suitable for high input voltage applications. The magnetizing inductor of the HB transformer can extend the ZVS of the lagging switches. The blocking capacitor together with the secondary novel-rectifying configuration can reset the circulating currents at the primary windings. Compared with the conventional TL dc–dc converter, the current stress of the switches and clamping diodes are all reduced, resulting in lower conduction loss. With introduction of PFC converter the power factor is also maintained at unity even in heavy load conditions of 1kW.

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