An Efficient VLSI Implementation 32-Bit Baugh-Wooley Multiplier

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Abstract: We proposed upon the Design and Implementation of 32-bit Baugh-Wooley multiplier in this paper. These include designs for adders and multipliers.Multiplication of signed number with two's complement form, namely the Baugh-Wooley multiplier. Tool for this design and implementation was Xilinx ISE 14.5.The Baugh-Wooley multiplier with its basic functions and its Mathematical calculation by using 4-bit architecture as reference 32-bit multiplier was designed using half adders and full adders.Research in various electronic devices based on VLSI technology in several levels. These VLSI technology based on CMOS have emerged from the devices. Due to this it increase in speed and performance to be area efficient multipliers. The efficiency of the Baugh-Wooley multiplier we observed that the circuit consists of several number of full-adders in Verilog-HDL. Using Xilinx ISE 14.5the full-adder can be observed.We implement with the design of Full Adder and XOR Gate with the Diffusion Input Technique due to this the transistor numbers. Transistor count and the Area design in Xilinx and the simulation is analysed result for the Baugh- Wooley multiplier. The design of multiplier for two's complement numbersdesign was found to be efficient than the existing.

IndexTerms - Full Adders, Half Adders, Baugh-Wooley multiplier.

I. INTRODUCTION

A binary multiplier is an electronic circuit used in digital electronics used to multiply two binary numbers in the computers. It is built using binary adders. Multipliers play a pivotal role in many high performance systems such as Microprocessor, FIR filters, Digital Processors, etc. Baugh-Wooley and Hwang proposed multiplication algorithm for numbers in two's complement form. Multiplication are higher speed, lower cost and lower power in hardware intensive and the main criteria of interest. In its early stage, multiplication algorithms were proposed by Burton and Noaks in the year 1968, by Hoffman in the year 1986 and by Guilt and De Mori in the year 1969 for positive numbers. In the year of 1973 and 1979.

The generation of the partial product and their accumulation are the two basic operations in multiplication. . Most techniques involve computing a set of partial products, and then summing the partial products together. Therefore, there are possible ways to speed up the multiplication that reduces the complexity, and as a result reduces the time needed to accumulate the partial products. Both solutions can be applied simultaneously. Many current Digital Signal Processing applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints.

The Baugh-wooley multiplier has a drawback as hardware complexity, need large routing area. This Technique is not apt for VLSI Design of multipliers. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design Algorithms. Since due to time complexity the array Multiplier has effected from delay having large size of Operand and with the complexity in space of O(n2), and Requires n2 cells for multiplication and the result will increase in size and power for large operands. A variety of Computer arithmetic technique can be used to implementation digital multiplier.

A multiplier is one of the key hardware blocks in most Digital Signal Processing systems. In Digital Signal Processing applications multiplier plays an important role include digital filtering, digital communications and spectral analysis. As many DSP based task which works in real time need to perform multiple tasks in a fast manner with the demise in power along with area.

II. SERIAL/PARALLEL MULTIPLIERS

The Design of serial and parallel multiplier circuit is represented. The signed or unsigned 2"s complement numbers and produce in this multiplier. The input y data and input x data is functioned in parallel and bit serial can be performed for multiplication and is feed across the multiplier for serial operation. For each and every cycle N numbers of partial products are generated. For each interval, each bit is added to the m*n partial Products. The overall outcome accumulated after the n-m interval, the needed area is n-1 for equal number of M-N. Depending on LSB Bit of multiplier, for every continuous clock, the bits of multiplier succeed to right and checked. If LSB bit is logic one then it acts upon shift operation. And its value isone then multiplicand is further added to accumulator after that succeeded to right for one bit.

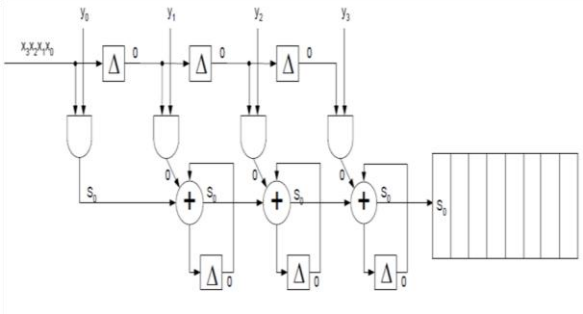

Fig 1.Design of Serial/Parallel Multiplier

Baugh-Wooley multiplier is compared to the advantage in hardware of this multiplier. The architecture represents the 32 bit Shift and Add multiplier for Multiplication of 64 bits. After the all 32 bits operation over then the multiplier bits are checked and product to accumulator. The size of accumulator is 2N (M-N), multiplier has N is initially in LSB. In asynchronous circuits, multipliers have more improvements.

III. BAUGH-WOOLEY ARCHITECTURE

Baugh-Wooley multiplier hardware architecture it follows left shift algorithm. Mux can select which bit will multiply. Suppose we multiply +4 and -4 in decimal we get '0'. Now, after representing these numbers in two's compliment form we get +4 as 0100 and -4 as 1100. On adding these two binary numbers we get 10000. Discard carry, then number is represented as '0'Thetemplateisusedtoformatyourpaperandstylethetext.Allmargins,columnwidths,linespaces,andtextfontsareprescribed;pleased onotalterthem.Youmaynotepeculiarities.Forexample,theheadmargininthistemplatemeasuresproportionatelymorethaniscustomary .Thismeasurementandothersaredeliberate,usingspecificationsthatanticipateyourpaperasonepartoftheentireproceedings,andnotasa nindependentdocument.Pleasedonotreviseanyofthecurrentdesignations.

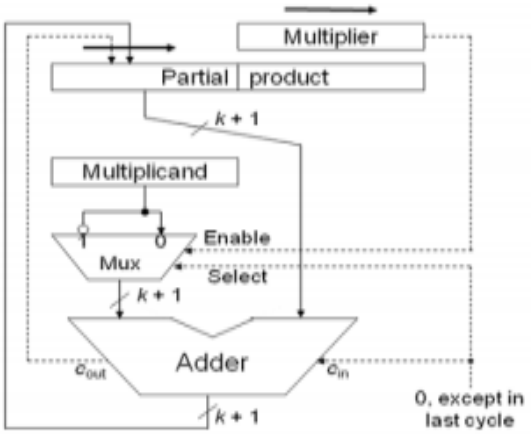

Fig 2.Hardware implementation of Baugh-Wooley Multiplier

IV. BAUGH-WOOLEY MULTIPLIERS

The algorithm which is having array multiplication for two"s complement bits is Baugh and Wooley. The focal point of this multiplier is the sign bits of all the multiplicand and multiplier is unsigned or positive. This algorithm is completely designed by using the conventional logic full adders. Here two"s complement numbers multiplied and then finally we get the products as (p0 –p6). The multiplication proposes of Baugh-Wooley Multiplier approach is represented.

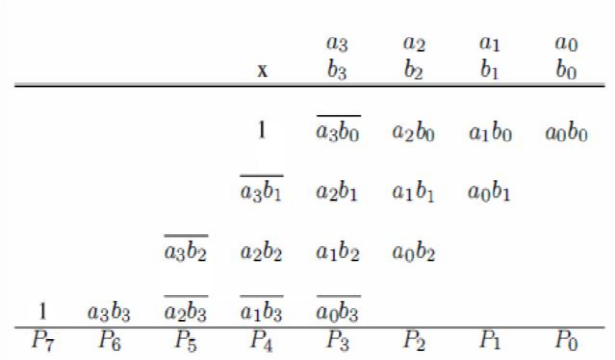

Fig 3.Baugh-Wooley multiplier for 4X4 bits

In this report, the research work has been presented for the Xilinx based VLSI design of the 32-bit Baugh-Wooley multiplier with the technique used for the design of Full-adder unit cell. Since the Baugh-Wooley multiplier which were having very significant application in DSP processors, signal and systems where convolution of signal is required. The authors in various papers shows a traverse approach to system design, through dealings among the algorithm design and core architecture and circuit accomplishment, can capitulate the most significant up gradation in design.

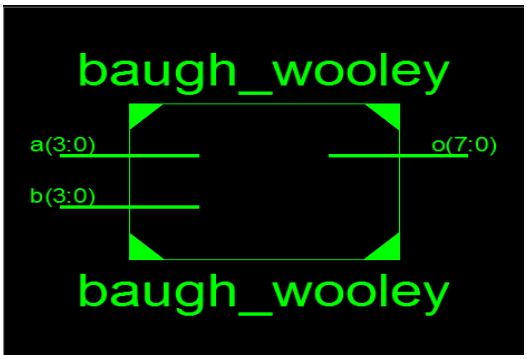

Fig 4.RTL View Of 4-bit Baugh Wooley Multiplier

In this work has been showing by the Verilog implementation for system design to obtain the results of various mathematical concepts. The based designing of the multiplier at various CMOS technology level gives various result of improvement in the field of complexity reduction. The optimization of transistor or chips is the major concern in the growing technology in the design of various multiplier architecture with applied algorithms.

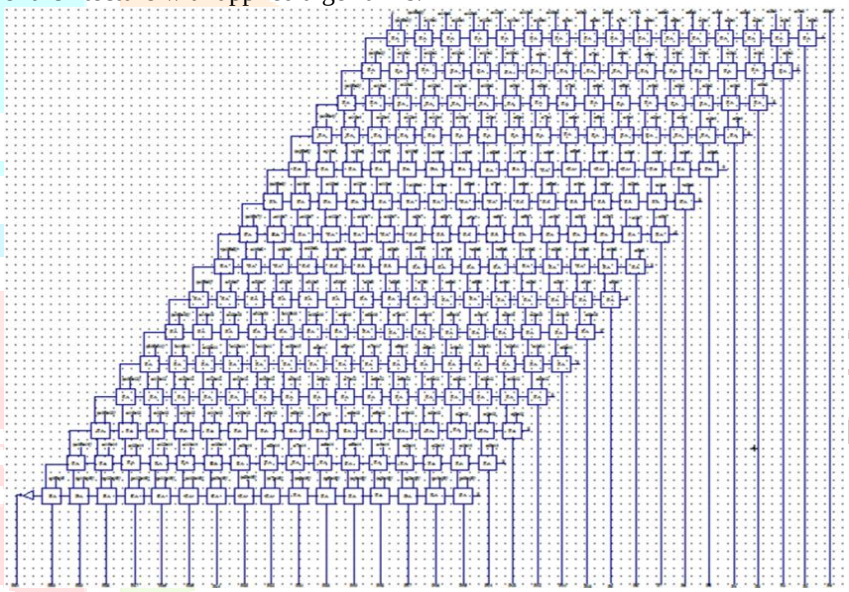

Fig 5.Block Architecture of 32x32 bit Baugh-Wooley Multiplier

V. RESULT

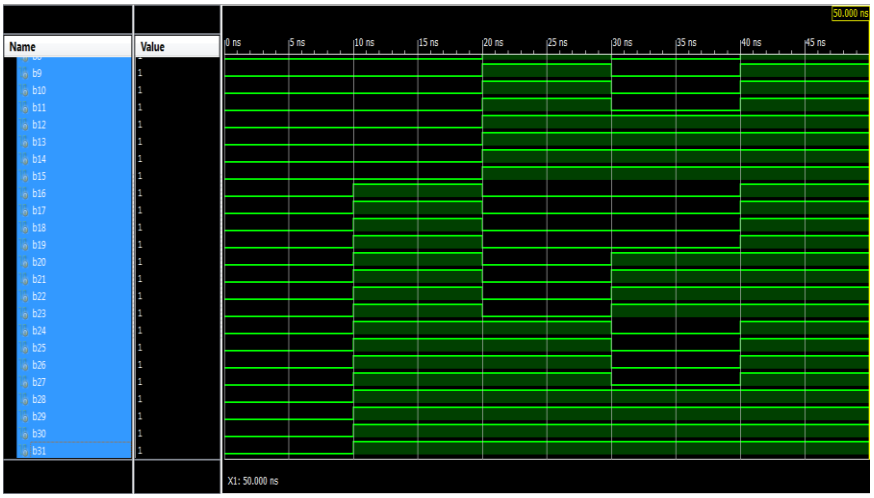

Fig 6.Output 32-bit Baugh Wooley Multiplier

VI. CONCLUSION

The proposal, multipliers have innumerous problems in all layout floor planning, levels of the design flow and fault problems due to delay paths. This proposed design which are presented the design of a 32-bit Baugh Wooley Multiplier using the based Adder's. Thepartial product terms using and gate &nand gate Boolean expressions are the basic steps were the Formulation of multipliers. In the procedure of designing the multiplier was assembled using the based Full Adder generated.In this design, we have showed the design of the 32-bit Baugh-Wooley multiplier with based Full Adder in Xilinx. The designs are based on some results in logic and the designs have been simulated and results show that the proposed design has low area as well as low transistor Count. This report also proposed a design methodology for multiplier circuits through the simulation of the full-adder based on Gate Diffusion Input technique. The Simulation Results from Xilinx ISE 14.5 is obtained. The layout is adopted from the RTL Generated from the ISE one used to balance the pipelined circuits. The proposed design methodology will speed up and facilitate the design of large based digital circuits much more. A design example proves the correctness and accuracy of this design methodology.

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