A Full-Bridge DC–DC Converter with Capacitive Output Filter for PHEV Driven Induction Motor Drive

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Abstract-A new topology of full-bridge dc–dc converter is proposed featuring zero-voltage-switching (ZVS) of active switches over the entire conversion range. The battery charging system is a critical part of a plug-in hybrid electric vehicle (PHEV). The efficiency, charging speed, and cost of such chargers are crucial to the commercialization of PHEVs. It was concluded that a full-bridge based PHEV charger is the most favorable choice among the four available topologies due to its power capability, soft switching capability, low electric stress, high efficiency but slightly elevated cost. This charger is able to control the values of the load voltage and c urrent and thenmaintain them at a desirable value. The proposed topology consists of super capacitor, which connected across the hybrid electrical vehicle. In this paper, a novel zero-voltage switching full bridge converter with trailing edge pulse width modulation and capacitive output filter is presented. Here presented synchronous rectified soft-switched phase-shift (PS) full-bridge (FB) converter with primary-side energy storage inductor, which is fit for low output voltage and high output current applications. For this application the objective is to achieve high efficiency and low cost in order to minimize the charger size, charging time, and the amount and the cost of electricity drawn from the utility. The simulation results are obtained using MATLAB/SIMULINK software.

Index Terms—Battery charger, capacitive filter, dc–dc converter, full-bridge, plug-in hybrid electric vehicle (PHEV), resonant converters, zero-voltage switching (ZVS).

I. INTRODUCTION

Alternative vehicle technologies to replace conventional vehicles consist of electric vehicles, hybrid electric vehicles (HEVs), plug in hybrid electric vehicles (PHEV) or else commonly called battery electric vehicles (BEVs), and fuel cell vehicles (FCVs). Battery Electric Vehicles (BEV's) refer to vehicles propelled exclusively by electric motors. The source of power stems from the chemical energy stored in battery packs which can be recharged on the electricity grid. The scope of such vehicles strongly depends on the battery and battery charger developments. EV battery chargers can be classified as on-board and off-board with unidirectional or bidirectional power flow. Unidirectional charging limits hardware requirements, simplifies interconnection issues, and tends to reduce battery degradation. A bidirectional charging system supports charge from the grid, battery energy injection back to the grid, and power stabilization with adequate power conversion. In order to make the charging easy, on-board chargers have been developed. The charger should to be able to plug into a socket and moreover, it should to be a grid friendly in order not to pollute the electrical network. The most general charger topologies includes an ac–dc converter with power factor correction (PFC) [1] followed by an isolated dc–dc converter. There are many high efficiency full bridge dc-dc converters [2]-[3] that can be used as the second stage converter. Phase shifted gating scheme [4]-[5] for full bridge dc-dc converter is most commonly used. Soft switching for the switches is achieved using an external inductor in addition to the leakage inductance of the transformer and the output capacitance of the switch. This converter has many improvements [6]-[7] but these improvements increase the number of components and also losses. Current fed topologies with capacitive output filter naturally minimize diode rectifier ringing since the transformer leakage inductance is effectively placed in series with the supply side inductor .In addition, high efficiency can be achieved with ZVS, using pulse width modulation technique. Current fed topologies with capacitive output filter inherently minimize diode rectifier ringing since the transformer leakage inductance is effectively placed in series with the supply side inductor. In addition, high efficiency can be achieved with ZVS, in particular the trailing edge PWM full-bridge gating scheme proposed in [35] is an attractive solution to achieve ZVS. In this paper, a novel PWM ZVS full-bridge dc–dc converter with the trailing edge pulse width modulation and capacitive output filter is presented.

II. OPERATING PRINCIPLES

The proposed ZVS full-bridge converter topology is illustrated in Fig. 1. The converter primary side circuit consists of a traditional full-bridge inverter. However, rather than driving the diagonal bridge switches simultaneously, the lower switches (Q3 and Q4) are driven at a fixed 50% duty cycle and the upper switches (Q1 and Q2) are PWM on the trailing edge [35]. Although the proposed converter can operate in either discontinuous conduction mode (DCM) [33], boundary conduction

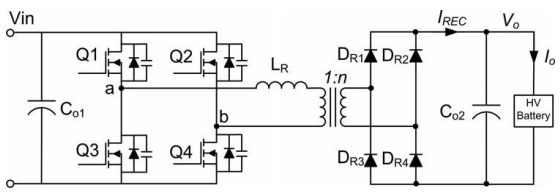

Fig.1. PWM ZVS full-bridge converter topology with a capacitive output filter.

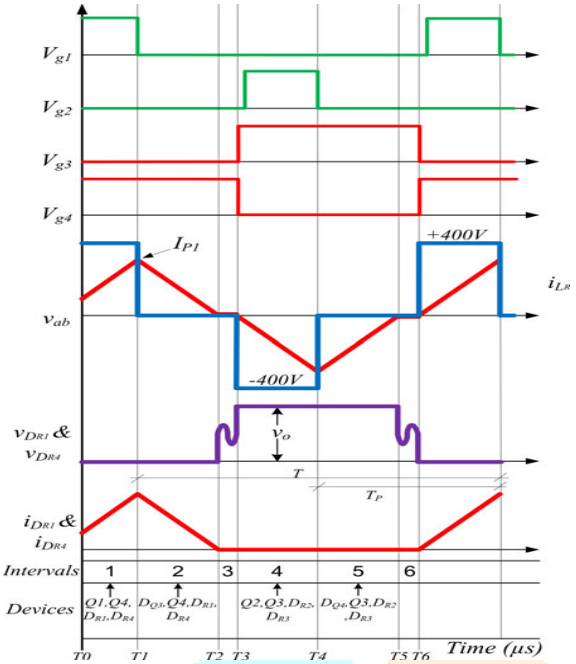

Fig. 2. Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a DCM mode.

mode (BCM), or continuous conduction mode (CCM), only the DCM and BCM modes are desirable, as discussed in section III. The detailed circuit operation in all three modes is given next. This converter has six operating intervals for DCM, BCM, or CCM. The operating intervals are determined by the ON/OFF states of the four primary switches. Detailed operating waveforms are provided for DCM in Fig. 2, for BCM in Fig. 3 and for CCM in Fig. 4. In the analysis that follows, the power semiconductor switches have been modeled with parallel diodes and parasitic capacitances. All parasitic capacitances in the circuit including winding and heat sink capacitance have been lumped together with the switch output capacitance. The output rectifiers are considered ideal and the external resonant inductor also includes the transformer leakage inductance.

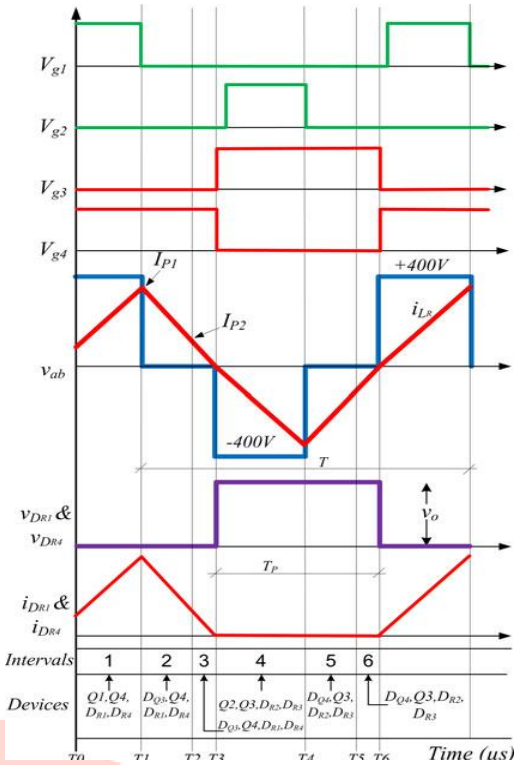

Fig 3. Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a BCM mode.

A. Interval 1 (T0−T1)

Referring to Figs. 2–4, during Interval 1 (T0–T1), switches Q1 and Q4 are ON and Q2 and Q3 are OFF. This is a power transfer interval and the primary current flows through Q1, resonant inductor L_R, transformer primary and Q4, as illustrated in Fig. 5. The rate of rise of the current (di/dt) through L_R is proportional to the difference between the input voltage V_{in} and the output voltage V_o. During this mode power flows to the output through rectifier diodes D_{R1} and D_{R4} and also energy is stored in L_R. The resonant inductor current $i_{LR}(t)$ using initial condition $i_{LR}(0) = 0$ is given by

$$i_{L_R}(t) = \frac{\left(V_{\text{in}} - \frac{V_o}{n}\right)}{L_R}(t - T_o).$$

B. Interval 2 (T1–T2)

1) Case (a): Operating in DCM: Referring to Fig. 2, interval 2 begins after switch Q1 turns OFF, as determined by the PWM duty cycle. Since the current flowing in the primary side cannot be interrupted instantaneously, it finds an alternate path and flows through the parasitic switch capacitances of Q3 and Q1 which discharges the node “a” to 0 V and then forward biases the body diode D3. During this switch transition, the energy stored in the resonant

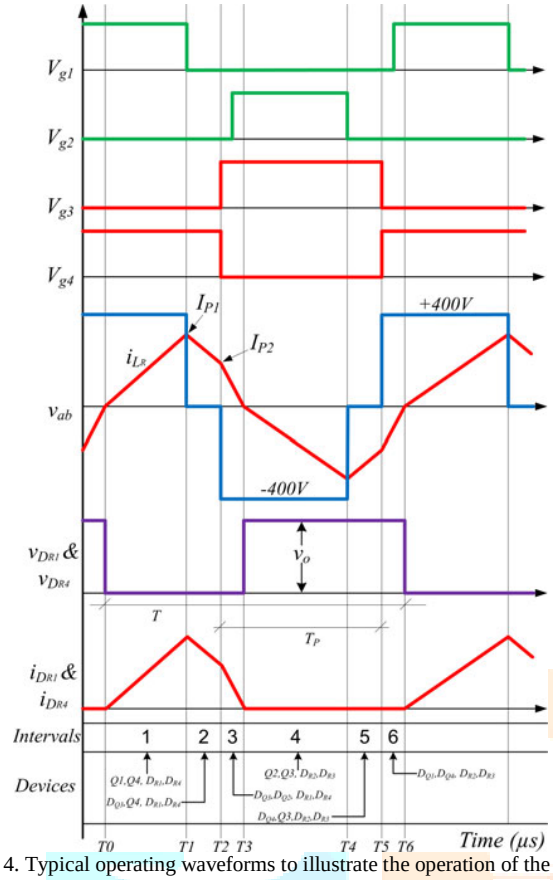

Fig. 4. Typical operating waveforms to illustrate the operation of the ZVS full-bridge converter in a CCM mode.

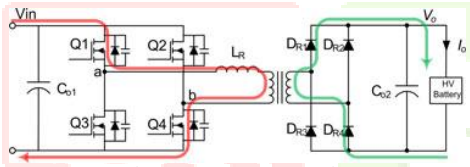

Fig. 5. Equivalent circuit for Interval 1 (T0–T1) for DCM, BCM and CCM.

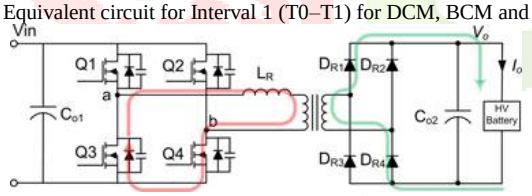

Fig. 6. Equivalent circuit for Interval 2 (T1–T2) for DCM, BCM, and CCM and Interval 3 (T2–T3) for BCM.

inductor *LR* assists in transferring energy from the lower to upper bridge MOSFET capacitances. Therefore switches Q3 and Q4 always achieve ZVS with the help of the energy stored in the resonant inductor *LR* for nearly the entire load current *Io* range. During this interval the energy stored in *LR* is transferred to the output. The primary resonant Inductor *LR* maintains the current, which circulates around the path of D3, resonant inductor *LR*, transformer primary and Q4, as illustrated in Fig. 6. The rate of the down slope of the current through *LR* is proportional to the output voltage *Vo*. At *T*2 the energy stored in *LR* is transferred to the output and the current becomes zero and the

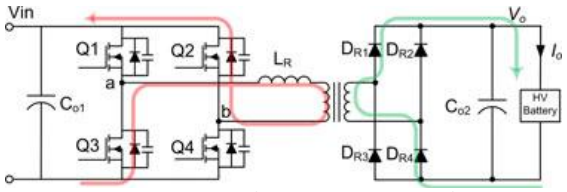

Fig. 7. Equivalent circuit for Interval 3 (T2–T3) for CCM.

rectifier diodes D_{R1} and D_{R4} turn OFF. The resonant inductor current $i_{LR}(t)$ using initial condition $i_{LR}(0) = I_{P1}$ is given by

$$i_{L_R}(t) = I_{P1} - \frac{V_o}{nL_R}(t - T_1)$$

C. Interval 3 (T2–T3)

1) Case (a): Operating in DCM: Referring to Fig. 2, during this interval no power is transferred to the secondary. Accordingly, this interval is a passive interval. In this interval, the parasitic capacitances of the rectifier diodes resonate with *LR*. This resonance appears across the rectifier diodes*DR*1 and*DR*4 as illustrated in Fig. 2. For this interval, current in the resonant inductor remains zero (*iLR* = 0).

2) Case (b): Operating in BCM: During this interval the resonant inductor current continues to circulate around the path of D3, resonant inductor *LR*, transformer primary and Q4, as illustrated in Figs. 3 and 6. The rate of the downslope of the current through *LR* is proportional to the output voltage *Vo*. At *T*3 the entire energy stored in *LR* is transferred to the output and the current becomes zero and the rectifier diodes *DR*1 and *DR*4 tur n OFF. The resonant inductor current *iLR* (*t*) using initial condition *iLR* (0) = *IP* 2 is given by

$$i_{L_R}(t) = I_{P2} - \frac{V_o}{nL_R}(t - T_2)$$

3) Case (c): Operating in CCM: Referring to Figs. 4 and 7, in CCM at *T*2, Q3 and Q4 toggle. The timing of this toggle is dependent on the resonant delay which occurs prior to Q2 turning ON. When Q3 and Q4 toggle, the primary resonant inductor current that was flowing through Q4 finds an alternate path by charging/discharging the parasitic capacitances of switches Q4 and Q2 until the body diode of Q2 is forward biased. If the resonant delay is set properly, switch Q2 can be turned ON with ZVS. At *T*3 the entire energy stored in *LR* is transferred to the output and the current becomes zero and the rectifier diodes D_{R1} and D_{R4} turn OFF. The resonant inductor current $i_{LR}(t)$ using initial condition $i_{LR}(0) = I_{P2}$ is given by

$$i_{L_R}(t) = I_{P2} - \frac{\left(V_{\text{in}} + \frac{V_o}{n}\right)}{L_R}(t - T_2)$$

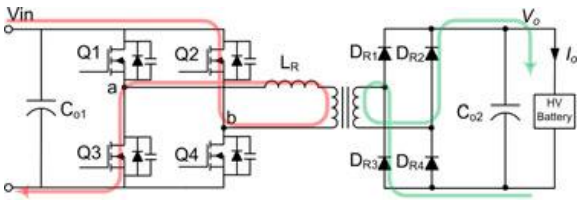

Fig. 8. Equivalent circuit for Interval 4 (T3–T4) for DCM, BCM, and CCM.

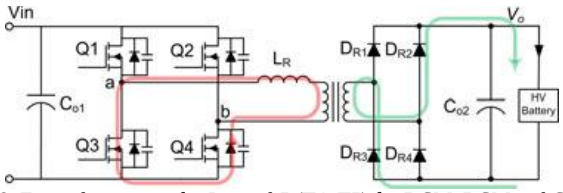

Fig. 9. Equivalent circuit for Interval 5 (T4–T5) for DCM, BCM and CCM and Interval 6 (T5–T6) for BCM.

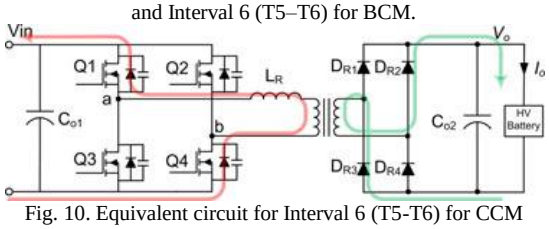

Fig. 10. Equivalent circuit for Interval 6 (T5-T6) for CCM

D. Interval 4 (T3–T4) Through Interval 6 (T5–T6) Intervals 4 to 6 are the negative equivalent of Intervals 1 to 3 as shown in Figs. 8–10.

III. SIMULATION RESULTS

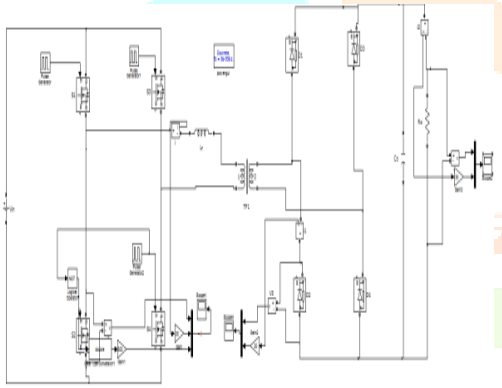

Fig.11. Matlab/Simulink model of proposed converter

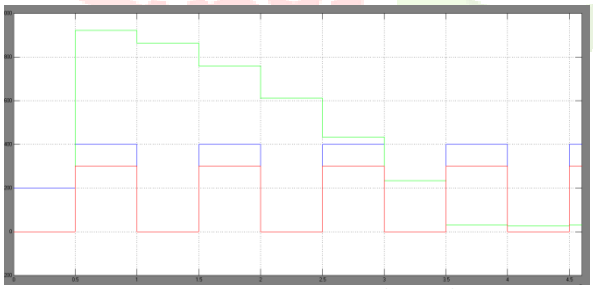

Fig.12. Proposed converter experimental waveforms of the MOSFET Q3 voltage and resonant inductor *LR* current

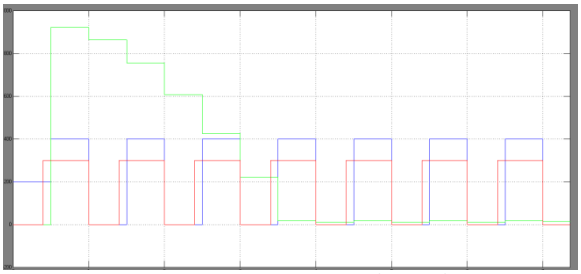

Fig.13. Proposed converter experimental waveforms of the MOSFET Q3 voltage and resonant inductor L_R current

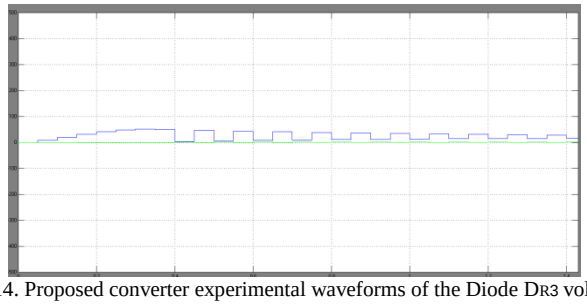

Fig.14. Proposed converter experimental waveforms of the Diode D_{R3} voltage and current

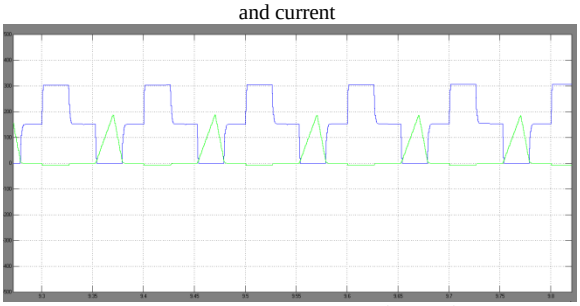

Fig.15. Proposed converter experimental waveforms of the Diode *DR*3 voltage and current

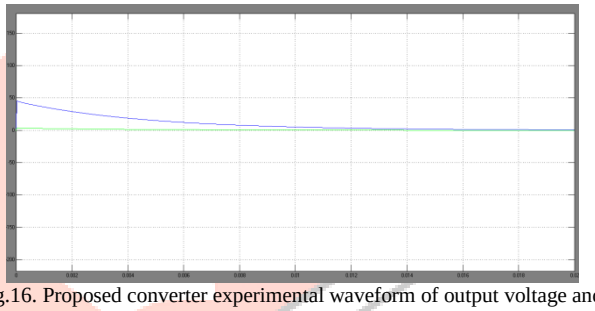

Fig.16. Proposed converter experimental waveform of output voltage and current

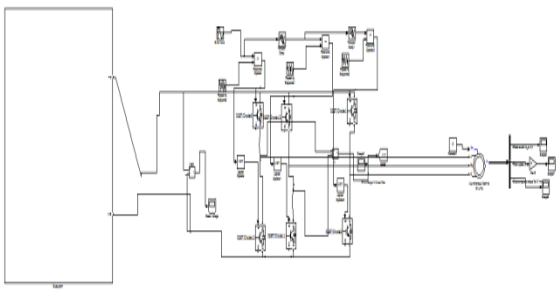

Fig.17.Matlab/Simulink model of proposed drive

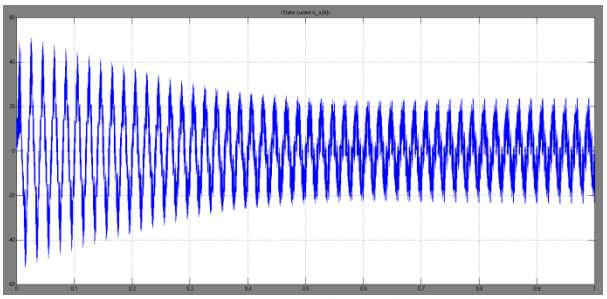

Fig.18 shows the simulation output waveform of stator current of induction motor

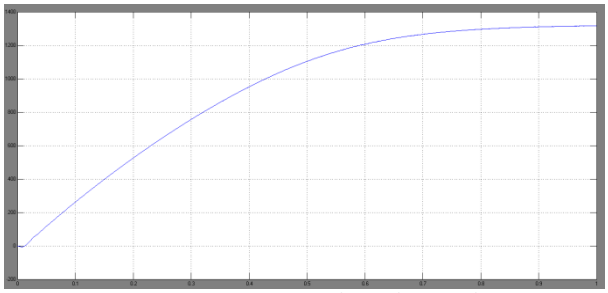

Fig.19 shows the simulation output waveform of speed of induction motor

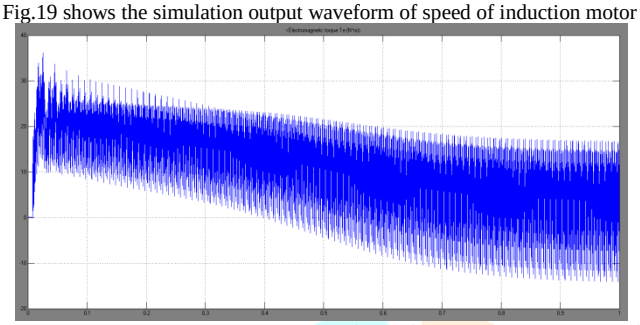

Fig.20 shows the simulation output waveform of electromagnetic torque of induction motor

IV CONCLUSION

The performance of the proposed converter with Stealth diodes is very similar to that with silicon carbide (SiC) diodes. Therefore, this converter permits use of inexpensive hyper fast diodes, which are typically one quarter of the price of SiC diodes. A novel ZVS full-bridge dc–dc converter with capacitive output filter has been presented for application in PHEV battery charging. The detailed operating intervals in DCM, BCM, and CCM were presented in addition to a step by step design procedure, simulation results and experimental waveforms. The proposed topology achieves soft switching for the full-bridge primary switches, naturally clamps the voltage across the output rectifier to the output voltage and the current through the rectifier diodes has a low *di*/*dt*, which helps to minimize reverse recovery losses.

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