PERFORMANCE ANALYSIS OF NON IDEAL BEHAVIOUR OF MOSFET WORKING

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***Abstract* — One of the most widely used electronic devices, particularly in digital integrated circuits, is the metal insulator semiconductor (MIS) transistor. In this device the channel current is controlled by a voltage applied at a gate electrode that is isolated from the channel by an insulator. The resulting device may be referred to generically as an insulated gate field effect transistor (IGFET).The main drives for reducing the size of the transistors, i.e., their lengths, is increasing speed and reducing cost. When you make circuits smaller, their capacitance reduces, thereby increasing operating speed. In the same token, smaller circuits allow more of them in the same wafer, dividing the total cost of a single wafer among more dies. However, with great reduction come great problems, in this case in the form of unwanted side effects, the so called short-channel effects. When the channel of the MOSFET becomes the same order of magnitude as the depletion layer width of source and drain, the transistors start behaving differently, which impacts performance, modeling and reliability.**

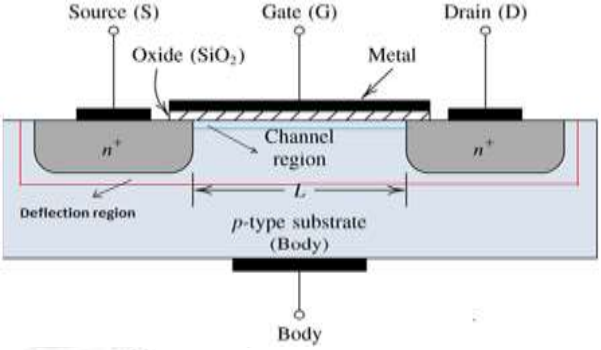
***Keywords* — MOSFET, DBIL, Velocity Saturation, Threshold voltage, surface scattering, impact ionization**

I. INTRODUCTION

A conceptually similar structure was first proposed and patented by Lilienfeld and Heil[2] in 1930, but was not successfully demonstrated until 1960. The main technological problem was the control and reduction of the surface states at the interface between the oxide and the semiconductor. Initially it was only possible to deplete an existing n-type channel by applying a negative voltage to the gate. Such devices have a conducting channel between sources and drain even when no gate voltage is applied and are called "depletion-mode" devices. A reduction of the surface states enabled the fabrication of devices which do not have a conducting channel unless a positive voltage is applied. Such devices are referred to as "enhancement-mode" devices. The electrons at the oxide-semiconductor interface are concentrated in a thin (~10 nm thick) "inversion" layer. By now, most MOSFETs are "enhancement-mode" devices. This device can be used as switch in many applications and offers little parasitic effects [1]. The drift of scaling was predicted by Moore's law, according to which the transistor count on an integrated circuit doubles every 18 months [3]. Alternative gate materials with dielectric constant higher than that of SiO_2 help to keep up with the trends of Moore's law [3, 4].The layers of these high – k materials can be grown thick to reduce the direct tunneling current through gate. A MOSFET device is considered to be short when the channel length is the same order of Magnitude as the depletion-layer widths (x_{dD}, x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel (Non Ideal) effects arise.

II. DEVICE OPERATION AND STRUCTURE

We used the simplest two dimensional three terminal device model for n-type MOSFET as shown below in Fig. 1. It is called an NMOS transistor because the major charge Carriers that form current are negatively charged electrons. The fourth terminal called body is not considered due to its secondary function in the MOSFET operation.



Fiq.1 MOSFET Block Diagram

For the case of an enhancement mode n channel device formed on a p type Si substrate. The n^+ source and drain regions are diffused or implanted into a relatively lightly doped p type substrate and a thin oxide layer separates the conducting gate from the Si surface. No current flows from drain to source without a conducting n channel between them. This can be understood clearly by looking at the band Diagram of the MOSFET in equilibrium along the channel[5]. The Fermi level is flat in equilibrium. The conduction band is close to the Fermi Level in the n+ source/drain, while the valence Band is closer to the Fermi level in the p-type material. Hence there is a potential barrier for an electron to go from the source to the drain, corresponding to the built in potential of the back to back p-n junctions between the source and drain. [5, 6] when a positive voltage is applied to the gate relative to the substrate, positive charges are in effect deposited on the gate metal. In response, negative charges are induced in the underlying Si, by the formation of a depletion region and a thin surface region containing mobile electrons. These induced electrons from the channel of the FET, and allow current to flow from drain to source. As fig suggests the

effect of the gate voltage is to vary the conductance of this induced channel for low drain to source voltage[8].

Since electrons are electrostatically induced in the p-type channel region, the channel becomes less p-type and therefore the valence band moves down, farther away from the Fermi level. This obviously reduces the barrier for electrons between the source, the channel and the drain. If the barrier is reduced sufficiently by applying a gate voltage in excess of what is known as the threshold voltage V_T, there is significant current flow from the source to the drain. For a given value of V_G there will be some drain voltage V_D for which the current becomes saturated after which it remains essentially constant.

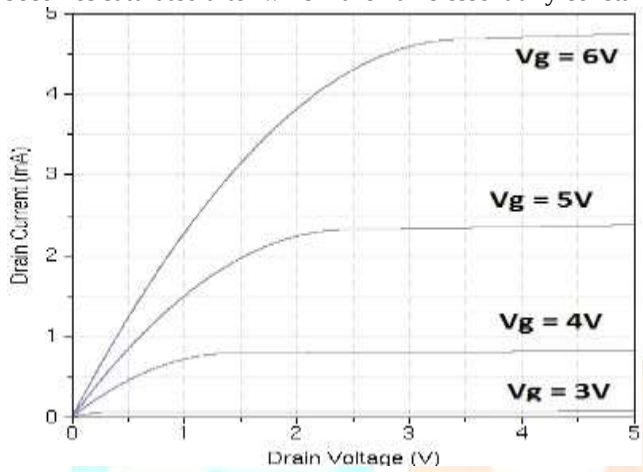


Fig. 2 I_d v/s V_{ds} characteristics of n-type MOSFET

The threshold voltage V_T is the minimum gate voltage required to induce the channel. The most common MOS transistor is normally off with zero gate voltage and operates in the enhancement mode by applying gate voltage large enough to induce a conducting channel. An alternative view of a MOSFET is that it is a gate-controlled resistor. if the positive gate voltage exceeds the threshold voltage in an n-channel device. Electrons are induced in the p-type substrate. Since this channel is connected to the n+ source source and drain regions, the structure look electrically like an induced n-type resistor. As the gate voltage increases, more electron charge is induced in the channel and therefore, the channel becomes more conducting. The drain current initially increases linearly with the drain bias (fig 2). As more drain current flows in the channel, however there is more ohmic voltage drops along the channel such that the channel potential varies from zero near the grounded source to whatever the applied drain potential varies from zero near the drain end of the channel. Hence the voltage difference between the gate and the channel reduces from V_G near the source to (V_G-V_D) near the drain end. Once the drain bias is increased to the point that (V_G-V_D) = V_T, threshold is barely maintained near the drain end, and the channel is said to be pinched off [9]. Increasing the drain bias beyond this point V_D(sat.) causes the point at which the channel gets pinched off to move more and more into the channel, closer to the source end. Electrons in the channel are pulled into the pinchoff region and travel at the saturation drift velocity because of the very high longitudinal electric field along the channel. Now the drain current is said to be in the saturation region because it does not increase with drain bias significantly. But actually there is a slight increase of drain current with drain bias due to various effects such as channel length modulation and drain induced barrier lowering (DBIL).where, k is the dielectric constant for gate oxide material, ε_0 is the permittivity of free space, and A is the gate area. Once the applied gate voltage is above threshold voltage, V_T channel is formed between source and drain diffusion region. As we increase the drain voltage, an increase in drain current is observed.

III. NON IDEAL EFFECT

1. Threshold Voltage: The voltage required to achieve flat band should be added to the threshold voltage equation obtained for the ideal MOS structure.

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F \cdots\cdots\cdots (1)$$

Thus the voltage required to create strong inversion must be large enough to first achieve the flat band condition (ϕ_{ms} and $\frac{Q_i}{C_i}$ terms),then accommodate the charge in the depletion region($\frac{Q_d}{C_i}$) and finally to induce the inverted region($2\phi_F$).Typically ϕ_{ms} is a negative quantity. The interface charge is positive so the contribution of the $-\frac{Q_i}{C_i}$ term is negative for either substrate type. On the other hand the charge in the depletion region is negative for ionized acceptors and is positive for ionized donors. Also the term ϕ_F which is defined as (E_i - E_F) / q in the neutral substrate can be positive of negative depending on the conductivity type of the substrate. Considering the sign in fiq.3

V_T =	ϕ_{ms}	$-\frac{Q_i}{C_i}$	$-\frac{Q_d}{C_i}$	$+2\phi_F$
	(-)	(-)	(+) n channel	(+) n channel
			(-) p channel	(-) p channel

We see that all the four terms give positive contribution in the n-channel case thus we expect positive threshold voltages for typical n-channel device. In n-channel positive value for V_T means the applied voltage means applied voltage must be larger than this threshold value to obtain strong inversion and conducting n channel.

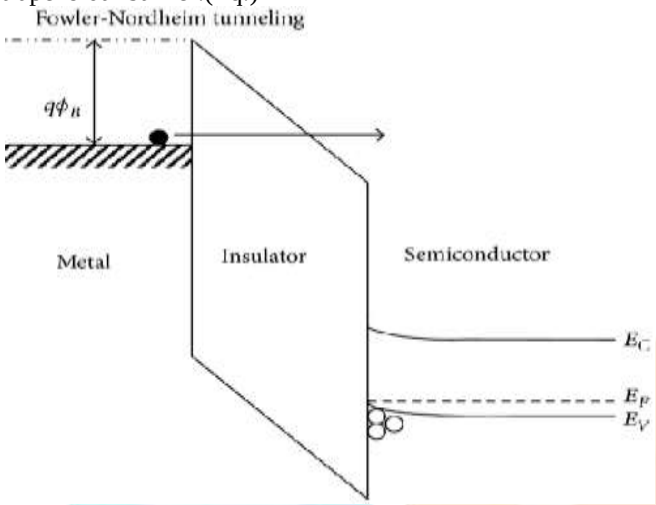
2. Tunneling Current:

An ideal gate insulator does not conduct any current, but for real insulators there can be some leakage current which varies with the voltage or electric field across the gate oxide. By looking at the band diagram of the MOS system perpendicular to the oxide silicon interface[9],we see that for electrons in the conduction band there is a barrier, ΔE_C (=3.1eV).Although electrons with energy less than this barrier cannot go through the oxide classically that quantum mechanically electrons can tunnel through a barrier especially if the barrier thickness is sufficiently small. As per the Fowler-Nordheim tunneling current I_{FN} can be expressed as a function of the electric field in the gate oxide.

$$I_{FN} \propto \varepsilon_{ox}{}^{2} \exp(\frac{-B}{\varepsilon_{ox}}) \cdots\cdots\cdots\cdots (2)$$

Where B is a constant depending on m_n and the barrier height.

As the gate oxides are made thinner in successive generations of MOSFETs, the tunneling barrier in the gate oxide becomes so thin that the electrons in the conduction band of Si can tunnel through the gate oxide and emerge in the gate without having to go via the conduction band of the gate oxide. This is known as direct tunneling rather than Fowler-Nordheim tunneling. For instance Fowler-Nordheim tunneling involves a triangular barrier while direct tunneling is through a trapezoidal barrier.(fiq.)



Such tunneling currents are becoming a major problem in modern devices because the useful features of high input impedance for MOS device degraded. It is necessary to increase the gate capacitance in successive generations of MOSFET in order to increase the drain current

$$C_i = \frac{\varepsilon_i}{d} \cdots\cdots\cdots (3)$$

We can achieve higher C_i by by using insulators with a dielectric constant higher than SiO_2 instead of reducing the gate oxide thickness d, as can be seen from eq. 4

$$V_i = \frac{-Q_s d}{\varepsilon_i} = \frac{-Q_s}{C_i} \cdots\cdots\cdots\cdots (4)$$

Where ε_i is permittivity of the insulator and C_i is the insulator capacitance per unit area. The charge Q_s will be negative for the n channel giving a positive V_i.

The advantage of not reducing d too much is that it keeps the tunneling barrier wide and the gate oxide field low, thereby keeping the gate tunneling barrier wide and the gate oxide field low, thereby keeping the gate tunneling leakage current low. Such high dielectric constant insulators such as hafnium dioxide, HfO_2 are also known as high K gate dielectrics because k is also sometimes used as symbol for dielectric constant.

3. Velocity Saturation (Mobility Effect)

In short channel devices the analysis has to be somewhat modified. As mentioned in the previous section the effective channel mobility decreases with increasing transverse electric field perpendicular to the gate oxide. Due to high electric field in the pinch off region under short channel the carrier velocity saturates. For short channel lengths the carriers travel at the saturation velocity over most of the channel. In that case the drain current is given by the width times the channel charge per unit area times the saturation velocity:

$$I_D(sat.) \approx ZC_i(V_G - V_T)V_s \cdots\cdots\cdots (5)$$

As a result the saturation drain current does not increase quadratically with $(V_G\text{-}V_T)$ as due to short channel. Drain current does not increase quadratically with $(V_G\text{-}V_T)$ as we studies earlier but rather shows linear dependence (equal spacing of curve).

4. Drain-Induced Barrier Lowering and Punchthrough

If small channel length MOSFET are not scaled properly and the source/drain junctions are too deep or the channel doping is too low there can be unintended electrostatic interactions between the source and the drain know as Drain Induced Barrier Lowering (DBIL).In this as the drain bias is increased the conduction band edge in the drain is pulled down and the drain channel depletion width expands.

$$x_{dD} = \sqrt{\left(\frac{2\varepsilon_{si}}{qN_a}\right)(V_{DS} + \phi_{si} + V_{SB})} \cdots\cdots\cdots (6)$$

$$x_{dS} = \sqrt{\left(\frac{2\varepsilon_{si}}{qN_a}\right)(\phi_{si} + V_{DB})} \cdots\cdots\cdots\cdots (7)$$

where V_{SB} and V_{DB} are source-to-body and drain-to-body voltages. When the depletion regions surrounding the drain extends to the source, so that the two depletion layer merge (i.e., when $x_{dS} + x_{dD} = L$), punchthrough occurs. Punchthrough can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels. The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the surface ($V_{GS}<V_{T0}$), the carriers (electrons) in the channel face a potential barrier that blocks the flow. Increasing the gate voltage reduces this potential barrier and, eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage V_{GS} and the drain-to-source voltage V_{DS}. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions ($V_{GS}<V_{T0}$) is called the sub-threshold current.

A variety of dielectric materials has been developed for gate oxide. Here, we have considered only Two popular materials, which are listed in Table 1.

TABLE 1
DIFFERENT OXIDE MATERIALS WITH THEIR DIELECTRIC CONSTANT

Sr. No.	Material	Dielectric constant (k)	Crystal Structures

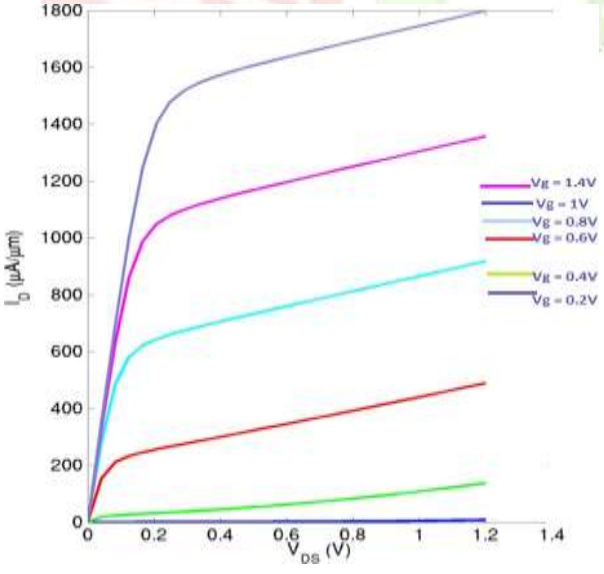
1	SiO_2	3.9	Amorphous
2	HfO_2	25	Monoclinic tetragonal cubic

5. Mobility Effect:

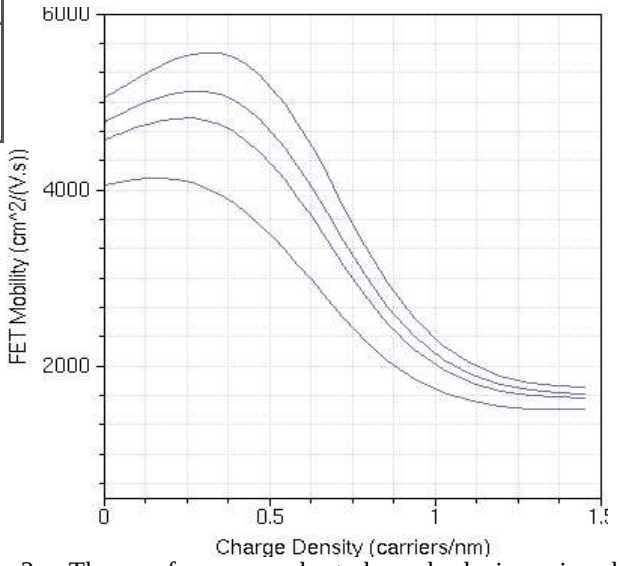
The mobility of carriers in the channel of a MOSFET is lower than in bulk semiconductors because there are additional scattering mechanisms. Since carrier in the channel is very close to the semiconductor-oxide interface, they are scattered by surface roughness and by columbic interaction with fixed charges in the gate oxide. When the carriers travel in the inversion layer from source to drain, they encounter microscopic roughness on an atomistic scale at the oxide-silicon interface and undergo scattering because any deviation from a perfectly periodic crystal potential results in scattering. This mobility degradation increase with the gate bias because higher gate bias draws the carriers closer to the oxide silicon interface, where they are more influenced by the interfacial roughness.

IV. SIMULATION RESULT

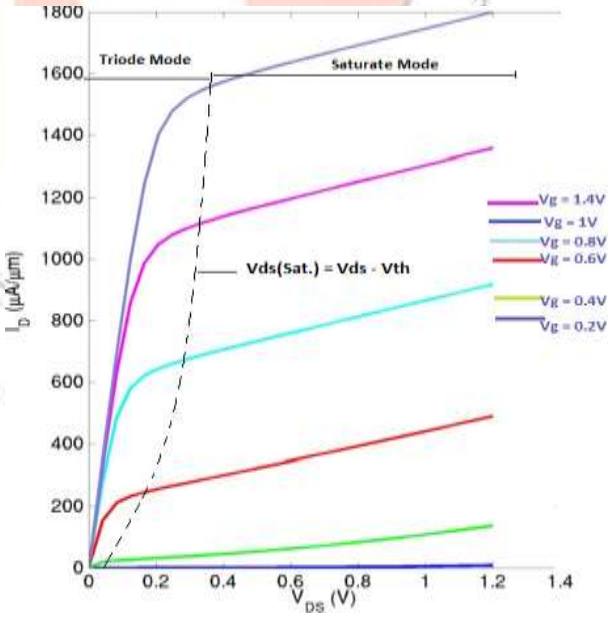
1. Short channel effect with reducing the length of channel and increase the drain to source voltage with different value of gate. As we decrease the channel length(short channel) we see that drain characteristics of MOSFET have non-zero slope, instead of ideal zero slope as shown in fiqure2. This non ideal effect occurs due to channel length modulation.



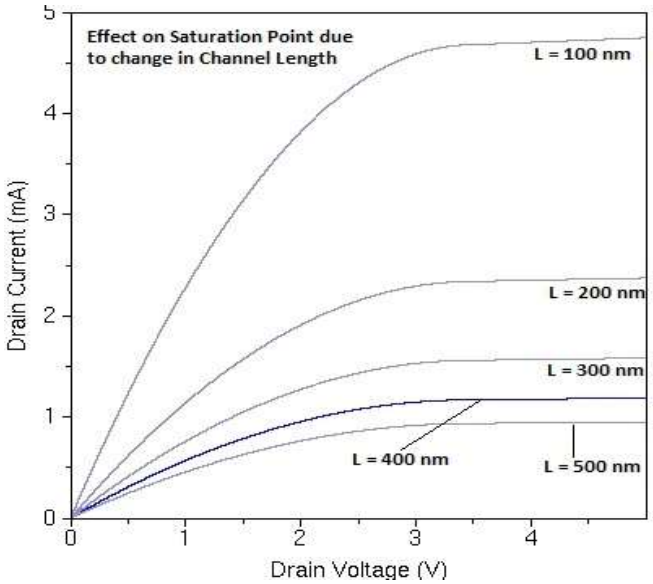
2. It is very interesting to note that if we plot the effective carrier mobility in the MOSFET as a function of the charge density in the middle of the inversion layer we get what is known as a universal mobility degradation curve for any MOSFET which is independent of the technology or device structural parameters such as oxide thickness and channel doping



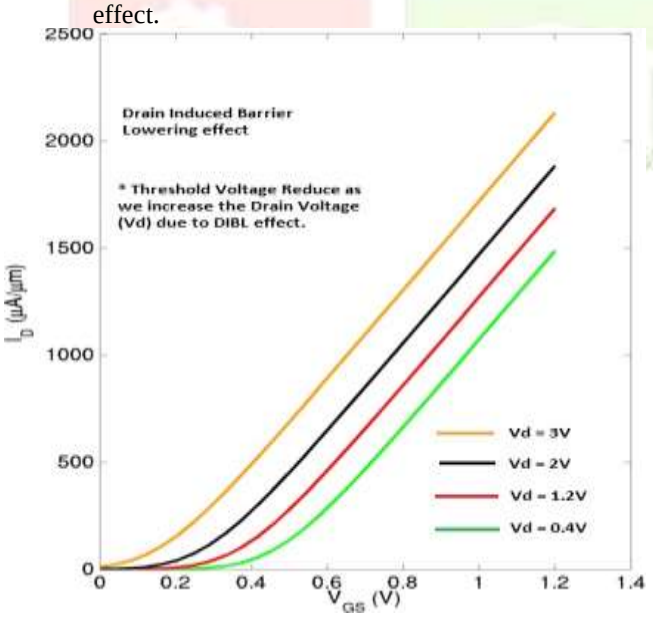
3. The performance short-channel devices is also affected by *velocity saturation*, which reduces the Transconductance in the saturation mode. At low *ey*, the electron drifts velocity *vde* in the channel varies linearly with the electric field intensity. However, as *ey* increases above 104 V/cm, the drift velocity tends to increase more slowly, and approaches a saturation value of *vde(sat)*=107 cm/s around *ey* =105 V/cm at 300 K.



4. Note that the drain current is limited by velocity saturation instead of pinch off. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages. Simulation result shows the effect of channel length on saturation point. as we increase the channel length saturation point goes also increasing.



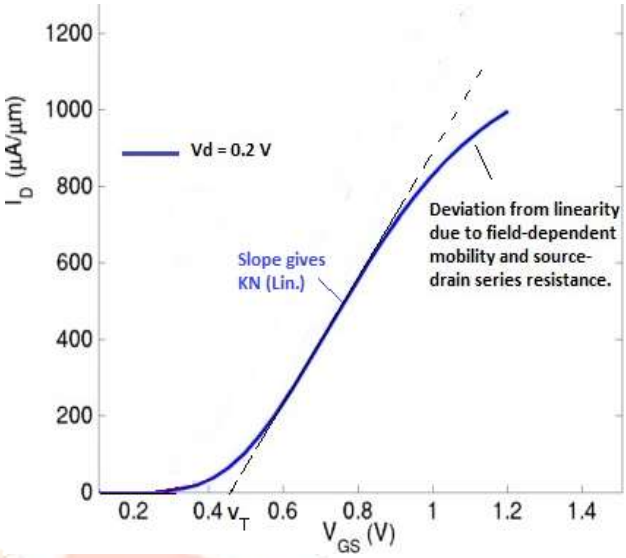
5. In the weak inversion regime there is a potential barrier between the source and the channel region. The height of this barrier is a result of the balance between drift and diffusion current between these two regions. If a high drain voltage is applied, the barrier height can decrease, leading to an increased drain current. Thus the drain current is controlled not only by the gate voltage, but also by the drain voltage. For device modeling purposes this parasitic effect can be accounted for by a threshold voltage reduction depending on the drain voltage.
Assume gate bias in all these simulations is 1.2 V and the applied drain bias varies between 0.4 V to 3 V.
Now Plot shows reduction in Threshold Voltage for different drain bias conditions to illustrate the DIBL effect.



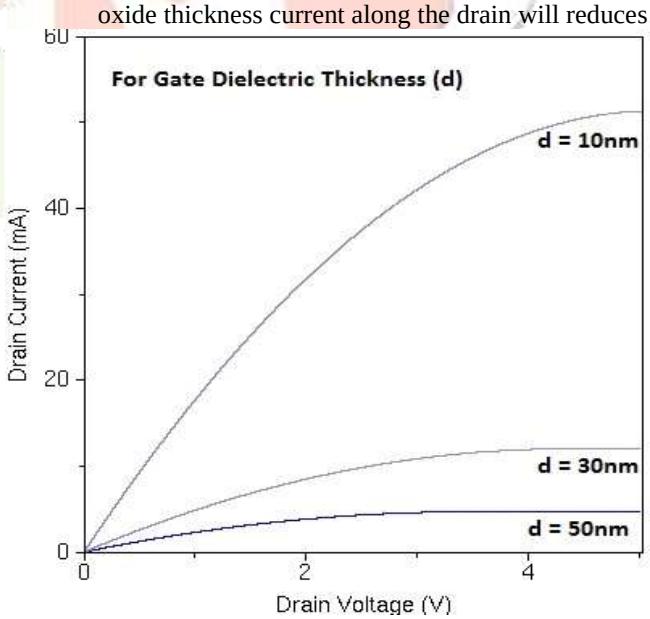
6. The transfer characteristics plot the output drain current as a function of the input gate bias,for fixed drain bias. Clearly in the linear region,I_D vs V_G should be a straight line from equation

$$I_D = \frac{\overline{\mu_n} Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D{}^2\right] \cdots\cdots(8)$$

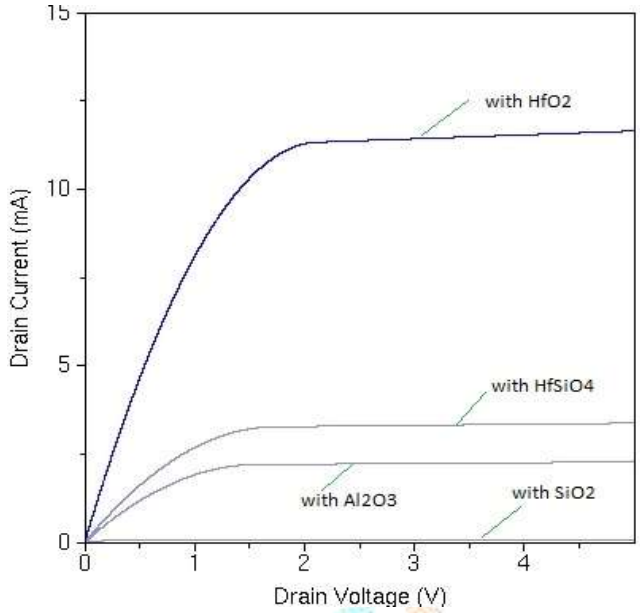
The intercept of this line on the V_G axis is the linear region threshold voltage,V_T(lin.), and the slope gives us the linear value of K_n of the n-channel MOSFET. But in actual we see that, while the characteristics are approximately linear at low gate bias, at high gate biases the drain current increases sub-linearly.



7. Now next one shows the effect of gate oxide thickness(d) on MOSFET working. We take three different value of thickness with constant gate voltage. Result will shows as we increase the gate oxide thickness current along the drain will reduces.



8. The choice of gate dielectric material plays a key role in channel inversion. the use of high k materials like hafnium/hafnium silicates results into more drain saturation current for same oxide thickness, with constant gate threshold voltage. Now the figure shows analysis of MOSFET working among the four oxide material SiO_2,Al_2O_3,$HfSiO_4$,HfO_2, the last one produces the maximum current for same gate voltage. Large saturation current with high k material is due to high permittivity, ε_{ox} offered by the material like HfO_2,$HfSiO_4$.



V. CONCLUSION

The designing of Integrated circuits in the past is simplified also due to over-designing. But as technology moves deeper into UDSM this is not a reliable approach. Too much performance is sacrificed or the area cost of over-designing leads to decreased contents. However, pushing the edge of the envelope may lead to under-design. Chips that have been under-designed often fail on the test bench or later in the field. Therefore, situations of over-design and under-design must both be identified when evaluating the integrity of a power distribution system. In the end, the design tradeoffs that satisfy all the necessary constraints are too complex to handle without tools that provide visibility into specific problems and their location on a chip. Designers are often required to tape out a design, and are left hoping that nothing will go wrong when the chip comes back from the fabrication.

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