New Multilevel Inverter topology with Reduced Number of Switches

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***Abstract*—**This paper introduces an novel topology of Multi-Level (seven level) Inverter (MLI) with reduced number of switches. Multilevel inverter targets Medium voltage, high power applications. This paper offers a new topology with reduced THD, switching losses and voltage overstress on switches. This multilevel inverter structured with the level module units to enhance the level of the voltage for levelled output. Since a level module unit consists of only a DC voltage source and a bidirectional switch, this structure allows a reduction of the system cost and size. Effectiveness of the proposed topology has been demonstrated by analysis and hardware implementation.

***Index Items*—** *Multilevel inverter, H-Bridge, Total Harmonic Distortion, Sinusoidal Pulse Width Modulation (SPWM)*

I. INTRODUCTION

Conventional two-level inverters, seen in Figure 1 are mostly used today to generate an AC voltage from a DC voltage. The two-level inverter can only create two different output voltages for the load, Vdc/2 or –Vdc/2 (when the inverter is fed with Vdc). To build up an AC output voltage these two voltages are usually switched with PWM, see Figure 2 Though this method is effective it creates harmonic distortions in the output voltage, EMI and high dv/dt (compared to multilevel inverters). This may not always be a problem but for some applications there may be a need for low distortion in the output voltage.

The concept of Multilevel Inverters (MLI) do not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform, see Figure 3, with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed.

Control method of inverter switches is shown in fig. 2. This technique is called as Sine Pulse Width Modulation (SPWM). This is achieved by generating output PWM signal with reference to sine wave, and generated using a triangular carrier wave signal comparing with sinewave signal.

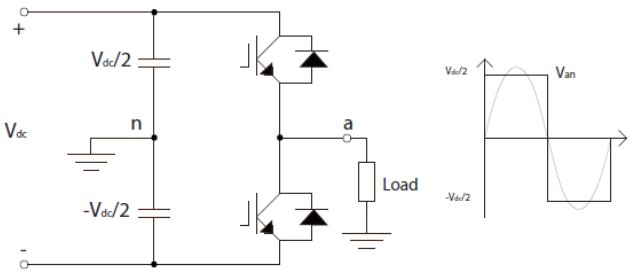

Fig. 1: Two-level inverter and a two-level waveform without PWM.

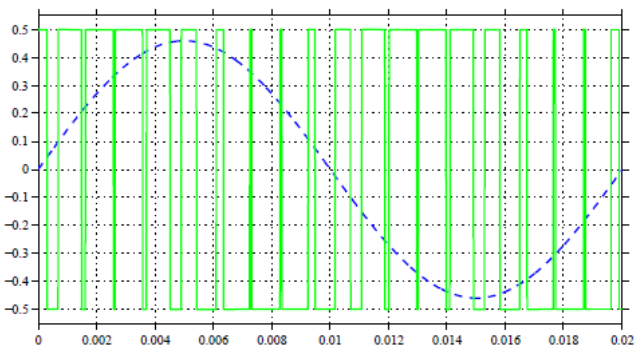

Fig. 2: SPWM voltage output, reference wave in dashed blue.

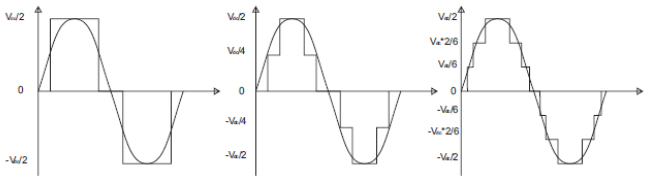

Fig. 3: A three-level waveform, a five-level waveform and a seven-level multilevel waveform, switched at fundamental frequency.

Some of the most attractive features in general for multilevel inverters are that they can generate output voltages with very low distortion and dv/dt, generate smaller common-mode voltage and operate with lower switching frequency compared to the more conventional two-level inverters. With a lower switching frequency the switching losses can be reduced and the lower dv/dt comes from that the voltage steps are smaller, as can be seen in Figure 3 as the number of levels increase. There are also different kinds of topologies of multilevel inverters that can generate a stepped voltage waveform and that are suitable for different applications. By designing multilevel circuits in different ways, topologies with different properties have been developed, some of which will be looked upon in this report. The Multilevel inverter topologies that are investigated in this report are: Diode Clamped Multilevel Inverter (DCMLI), Capacitor Clamped Multilevel Inverter (CCMLI) and Cascaded H-bridge Inverter (CHMLI). The most dominant multilevel inverters use one or more voltage sources, as the five-level inverter, and most topologies presented in this report will have voltage sources, so called Voltage Source Inverters (VSI).

II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed multilevel inverter topology consists of the level module units. A level module unit is constructed by one DC voltage source and two switches for bidirectional functionality which is switch capable of current conduction and blocking voltage in both directions as shown in Fig. 2. Also, discrete devices can be used to construct suitable switch cells. Advantage of this switch structure is that each level module unit requires only one isolated power supply instead of two for the gate driver. Advantage of modular approach is easy to enhance the voltage levels depend on voltage source availability.

As a result, the construction cost of the proposed topology is lower than other conventional and multilevel inverters with reduced number of switches. The generalized structure of the proposed multilevel inverter is given in Fig. 2. It is shown that this structure consists of two basic parts. The first is the side of level module units producing DC voltage levels. The second is H-bridge topology, which generates both of the positive and the negative output voltages.

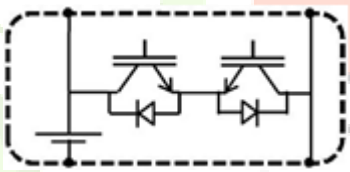

Fig. 2 A Level module unit

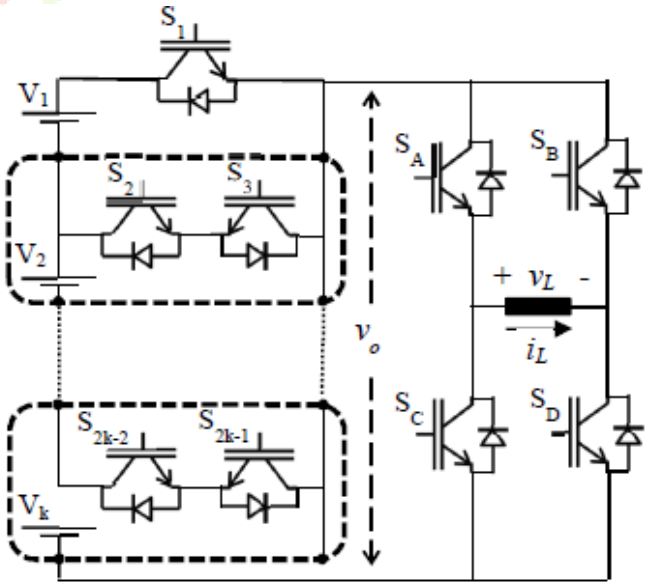

Fig. 3. The proposed structure of multilevel inverter

It is clear that system can be easily expanded by adding level module units and the voltage level number multilevel inverter can be increased.

Considering that k is the number of discrete DC voltage sources, the maximum and minimum values of output voltage of level module units are:

$Vo\_max = kVdc$ (1)

$Vo\_min = 0$ (2)

And if the power switches is turn on and turn off, Si(t) = 1 and Si(t) = 0 for i = 1,2, … , (2k − 1), respectively. So, the output voltage of level module units can be expressed by

$$Vo(t) = V_1S_1(t) + (V_2S_2(t) + V_3S_4(t) \ldots\ldots + V_kS_{2k-2}(t)) \quad (3)$$

The positive output voltage on the load is

$$Vo(t)^+ = V_1S_1(t) + V_2S_2(t) + \cdots + V_kS_{2k-2}(t)[S_B(t)\&S_D(t)] \quad (4)$$

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$$Vo(t)^- = V_1S_1(t) + V_2S_2(t) + \cdots + V_kS_{2k-2}(t)[S_A(t)\&S_C(t)] \quad (5)$$

As a result, the overall output voltage of the proposed multilevel inverter can be given as follows:

$$Vo(t) = Vo(t)^+ + Vo(t)^- \quad (6)$$

The maximum and minimum values of the generated output voltage are respectively

$$V_{L\_max} = kVdc \quad (7)$$
$$V_{L\_min} = -kVdc \quad (8)$$

If all discrete DC voltage sources V_k in Fig. 2 are equal, the number of the output voltage levels N_{level} is

$$N_{level} = 2k + 1 \quad (9)$$

The number of switch used is

$$S_{number} = 2k + 3 \quad (10)$$

This value is 4k in the H-bridge cascaded multilevel inverter.

III. THE CONTROL STRATEGY OF PROPOSED TOPOLOGY

In this paper, the number of switching angles which need to be calculated has been changed according to the number of output voltage levels. This quantity is also same as the number of DC voltage sources as seen in (11). The used switching angles have been calculated by (12).

$$N_\alpha = k = P\left(\frac{N_{level}-1}{2}\right) \quad (11)$$

$$\alpha_j = arsin\left(\frac{2_j-1}{N_{level}-1}\right) \quad j = 1,2,\ldots..k \quad (12)$$

In Fig. 4, the angles required are illustrated to obtain a full period of the output voltage in 5-level multilevel inverter. It is clear that the other angles can be easily derived from α_1 and α_2. The states of switches which cannot be on simultaneously are given in Table I in order to avoid a short circuit as understood from Fig. 3.

There are ten different switching states to obtain a full period of the output voltage in 5-level multilevel inverter. The used switching state quantities can be expressed by $N_{level} + 5$ according to the number of output levels or by $2k + 6$ according to the number of DC voltage sources.

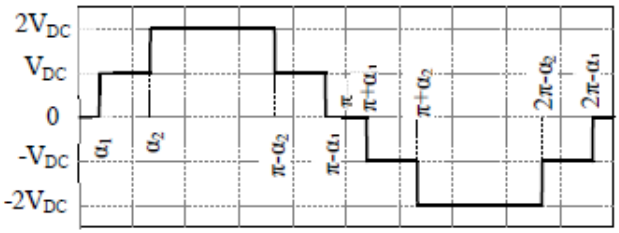

Fig. 4. The output waveforms of 5-level

Table I. Inconvenient switch states in the proposed multilevel inverter

	Switches cannot be on simultaneously					
1	S_A	S_C				
2	S_B	S_D				
3	S1	S3	S5	S7	…	S2k-1

The system Block diagram of the complete Multilevel inverter is as follows:

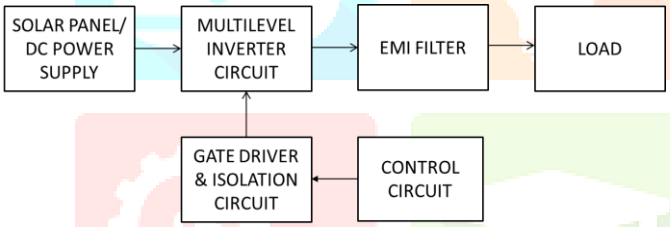

Fig. 5 complete model block diagram

All working states of power switches of the proposed 5-level multilevel inverter are summarized in Table II.

Table II. The output voltage and current values for state of power switches in the proposed 7- level multilevel inverter.

	States of power switches							voltage	current
	S1	S2	S3	S_A	S_B	SC	SD	V_L	I_L
1	off	off	off	on	off	off	off	0	+
2	off	off	off	off	off	on	off	0	-
3	off	on	off	on	off	off	on	V1	+
4	off	off	on	off	off	off	off	V1	-
5	off	off	on	off	off	off	off	-V1	+
6	off	on	off	off	on	on	off	-V1	-
7	on	off	off	on	off	off	on	V1+V2	+
8	off	off	off	off	off	off	off	V1+V2	-
9	off	off	off	off	off	off	off	-(V1+V2)	+
10	on	off	off	off	on	on	off	-(V1+V2)	-

IV. RESULT

Since the aim of this study is to introduce a novel multilevel inverter, it has not been mentioned about the improving of total harmonic distortion. Some simulation results for 5-level and 7-level inverters have been given to evaluate the performance of the proposed novel multilevel inverter in the synthesis of a requested load voltage waveform. In this study, a 5-level inverter can generate staircase voltage waveform respectively with maximum 24 V and 36 V, due to the values of the used DC voltage sources are 12 V. we can extend voltage upto 200V to 300V with the same designed circuit. The simulated multilevel inverters have been loaded by two different loads. The load at output is pure resistive load. In this study, the fundamental frequency switching pattern has been utilized. This switching pattern causes less switching losses from other patterns due to its low switching frequency.

In Fig. 6, the gate signals of all switches in 5-level multilevel inverter are clearly shown. While the staircase output voltage is synthesized, the power flow in this switching structure is bidirectional, both from source to load and from inductive load to source. Fig. 7 shows the voltage of 5-level multilevel inverter for pure resistive load. It is shown that the waveform of the load current is the stepped. Also, it has a unity power factor. The voltage and current of 5-level multilevel inverter for R-L load will be as same as pure resistive load but the output current will be sinusoidal waveform with a fundamental frequency due to inductive load. Also, the power factor cannot be not unity.

It is understood that the more the number of levels are increased, the more the output waveforms are similar to the pure sinusoidal. The number of output levels in the proposed multilevel inverter can be easily increased by connecting the level module units.

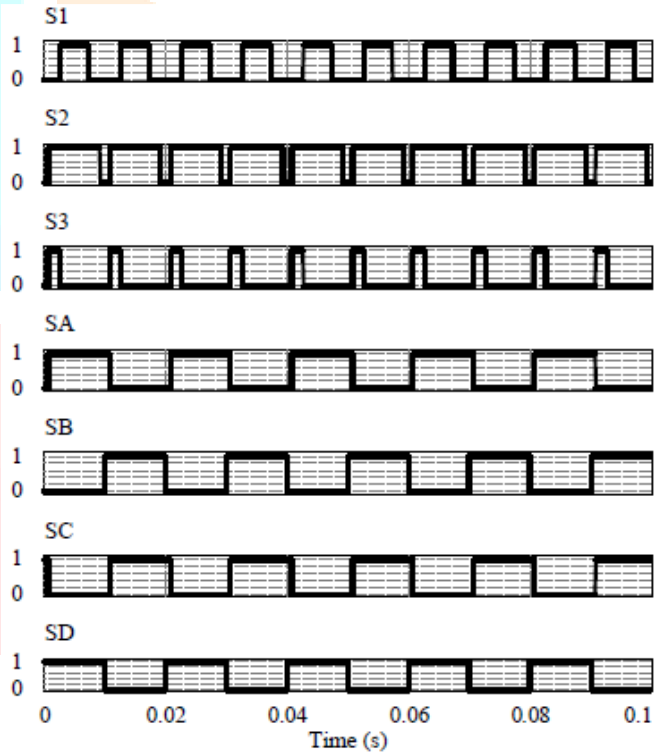

Fig. 6. Gate signals of all switches in 5-level multilevel inverter

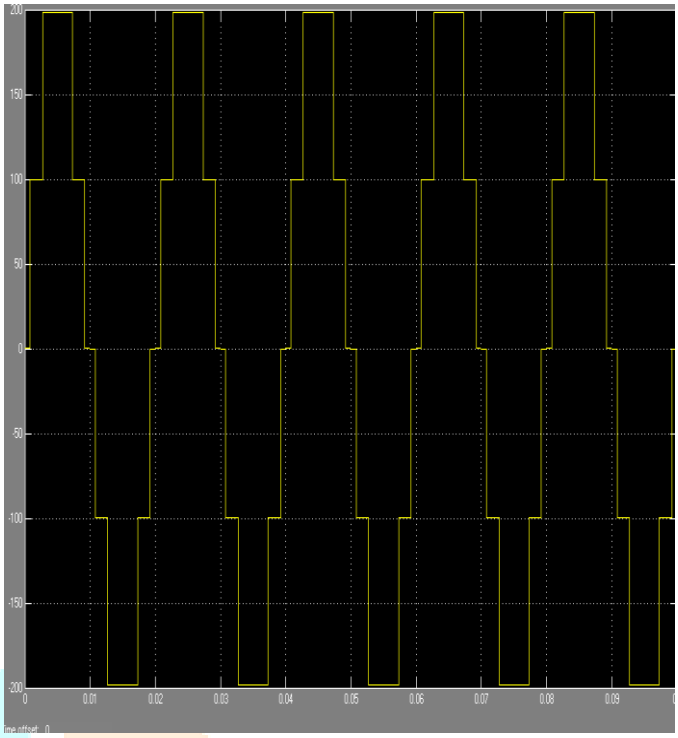

Fig. 7 Output voltage level of 5 level inverter.

V. CONCLUSION

A novel structure of multilevel inverter which needs the minimum number of switches has been proposed. The modulation technique and calculation of conducting angles for the proposed topology has been introduced. The additional level module units have been use to increase the output levels.

Since the devices in the level module units are common emitter back to back, each unit has been required only one isolated power supply for driver. Therefore, construction cost of the proposed multilevel inverter is lower and it is not bulky. The operation and performance of the proposed structure has been proved by simulations of 5-level and 7-level multilevel inverter.

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