# InGaAs Tunnel Field Effect Transistor with High-K Gate Dielectric

**Sawan Gupta**
**Assistant Professor**
**Department of Electronics and Communication Engineering**
**Vaish College of Engineering, Rohtak, India**

***Abstract*:** Tunnel Field Effect Transistor is considered as a very promising device for ultra-low power applications because of its steep sub-threshold slope prospects. The carrier injection mechanism in Tunnel Field Effect Transistor is band-to-band tunneling which reduces the leakage current because of high tunnel barrier width. Silicon as a Tunnel Field Effect Transistor channel material limits the thermal conductance, transit time and switching energy because of its high and indirect band gap. So, III-V direct and small band gap materials such as InGaAs, InAs, GaSb etc. are used to improve performance of the device. In this paper, Tunnel Field Effect Transistor using $In_{0.53}Ga_{0.47}As$ as channel material and high-k dielectric for gate using Cogenda Visual TCAD is presented. The proposed device showed better threshold voltage, DIBL and subthreshold swing as compared to MOSFET.

***IndexTerms*** : **TFET, Band to band tunneling (BTBT), Subthreshold swing (SS), Single Gate TFET, DIBL, ON current ($I_{ON}$) and OFF current ($I_{OFF}$).**

## I. INTRODUCTION

MOSFET, the metal–oxide–semiconductor field-effect-transistor has been the backbone of digital integrated circuits over the past three decades. The scaling of MOS devices plays an important role in the rapid development of the semiconductor electronics. The device scaling allows the more devices or functions to be integrated into a single chip within a given area, or allow the same number of devices or a given function to be realized on a chip with a smaller silicon area. This reduces the Cost per device and/or per function. But scaling of MOS devices into the nanoscale region is affected by various factors like short channel effects, non-scalability of subthreshold swing, threshold voltage roll-off, high standby leakage current etc. [1]. These factors degrade the performance of MOS devices. An alternate of MOS devices is Tunnel Field Effect Transistor (TFET) which has the capability of working in ultra-low power and achieving steep subthreshold slope [2]. TFET is simply a gated p-i-n diode which operates only in the reverse bias mode and has a different phenomenon of quantum barrier tunneling of electrons at the tunnel junction to provide the transport mechanism of carriers [3]. As the band-to-band tunneling is not a temperature dependent process, so TFETs have very weak temperature dependence. Hence, it can achieve lesser subthreshold swing than kT/q limit (60 mV/dec) at room temperature thus making it a promising device of future semiconductor era [4].

In TFET, gate modulated tunnel barrier is used to control I-V characteristics which allows it to bypass thermionic limit [5]. It can attain the subthreshold swing lower than 60 mV/dec at room temperature, even in some cases subthreshold swing nearly 25 mV/dec have been reported [6]. The lower subthreshold swing indicates that the switching of TFET is much faster than that of the conventional MOSFET's. Due to their built in tunnel barrier, they are almost immune against short channel effect [7]. In TFETs, gate controls the tunnel barrier width so very small leakage current flows because of high tunnel barrier width. This reduces the power dissipation of the device. In TFETs, both the dynamic and static power dissipations are small due to the steep subthreshold slope [8]. These properties of TFETs allow them to behave similar to an ideal ON/OFF switch with small variation of gate voltage at the threshold potential. Thus, TFETs are very promising candidate for ultra-low power era.

## II. BAND TO BAND TUNNELING MECHANISM (BTBT)

In this mechanism, electrons travel from the valence band of the semiconductor to the conduction band by tunneling across a potential barrier. The tunneling process is of two types.

### 2.1 Direct tunneling

The tunneling process in which electrons travel from the valance band to the conduction band without the absorption or emission of photon is known as direct tunneling.

### 2.2 Indirect tunneling

The tunneling process in which electron acquires a change in momentum by absorbing or emitting a photon is indirect tunneling. The indirect tunneling is the main tunneling process because the direct tunneling process is negligible in indirect band gap materials like silicon because the higher barrier width decreases the transmission probability rapidly.

## III. DEVICE STRUCTURE

The physical structure of TFET is same as that of MOSFET. TFET is also a voltage controlled current device with four terminals (source, drain, gate and body) in which source and body terminals are short circuited and a very thin oxide or dielectric layer is present between gate and intrinsic region. The only difference between MOSFET and TFET is that of doping. In MOSFET, source and drain are similarly doped but in TFET, source and drain are of opposite doping. Use of high-k dielectric instead of oxide layer gives more tunneling current and better subthreshold swing [9], [10]. The conventional N-TFET structure is shown in Fig. 1 in which the source is highly doped p-type, intrinsic region or body is moderately doped p-type and drain is highly doped n-type.

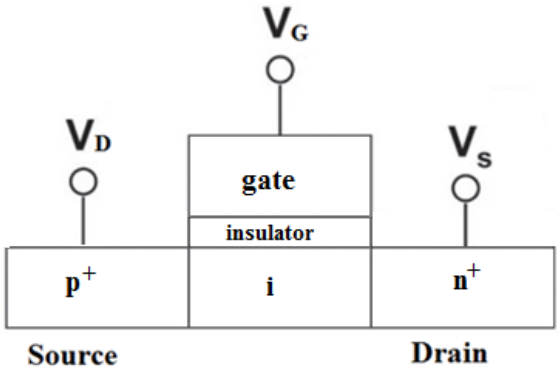


Fig. 1 Structure of conventional TFET

## IV. WORKING PRINCIPLE OF TFET

### 4.1 OFF state

In OFF state, applied gate voltage ($V_{gs}$) is either zero or less than threshold voltage ($V_t$) so the channel between source and drain does not exists and hence, the tunnel barrier width becomes very large. The electrons from the valance band of the source cannot tunnel to the conduction band of the intrinsic region because of the large tunneling barrier thus giving an extremely low current generally known as OFF current ($I_{OFF}$).

### 4.2 ON state

In ON state, the applied gate voltage is greater than the threshold voltage so the electrons starts accumulating on the surface below the gate in the intrinsic region. This reduces the tunneling barrier width which increases the electric field near the p-n junction. The band-to-band tunneling (BTBT) occurs when the electric field across a p-n junction is sufficiently large and the electrons from the valance band of the source region tunnel to the conduction band of the intrinsic region without the assistance of traps. These electrons are then transported to the drain through drift diffusion and gives the ON current ($I_{ON}$). The energy band diagram for ON and OFF state of n-TFET is shown in Fig. 2.

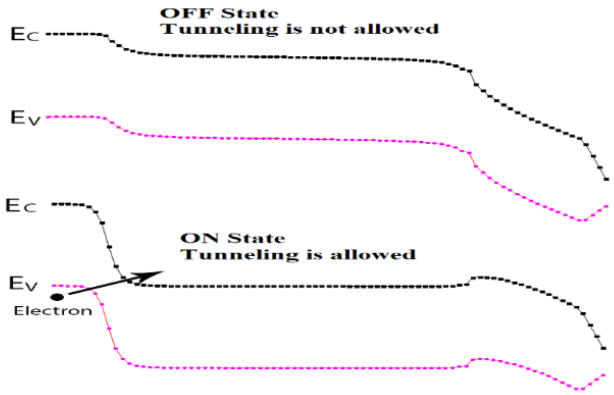


Fig. 2 Energy band diagram in the OFF/ON states of the n-channel TFET

## V. InGaAs TFET

Silicon as a TFET channel material limits the thermal conductance, transit time and switching energy because of its high band gap [11]. However, Germanium has lower band gap ($E_g$) but Si and Ge both have indirect band gap that means the electrons absorb some extra energy from the vibrations in the lattice while transitioning from one band to another which reduces the tunneling probability significantly and hence reduces the current carrying capability [9]. The band to band generation rate according to the Hurkx's model is given by [12],

$$G_{BTBT} = D_{tunnel} \times A_{BTBT} \frac{E^{C_{BTBT}}}{2} \times e^{\left(-B_{BTBT} \times E_g^{3/2}\right)} \quad (1)$$

where $G_{BTBT}$ is band to band generation rate, $D_{tunnel}$ is the tunneling factor which takes into account the probability of having a filled state to tunnel from and empty state to tunnel to and $A_{BTBT}$, $B_{BTBT}$ and $C_{BTBT}$ are material related parameters.

From above equation, it can be observed that band to band generation rate is highly dependent on band gap ($E_g$). Thus, band to band generation rate can be increased by using smaller and direct band gap materials [13]. The III-V compounds are direct band gap materials such as InAs, GaSb, InGaAs, GaAsSb etc. [14].

In this work, III-V compound semiconductor $In_xGa_{1-x}As$ with mole fraction $x$ = 0.47 which is $In_{0.53}Ga_{0.47}As$ is used as channel material. It is having a bandgap of 0.85 eV and effective mass $0.043m_0$, ensuring a higher tunneling probability. The simulation structure of $In_{0.53}Ga_{0.47}As$ TFET is shown in Fig. 3. In this, Source region is highly doped with p-type, drain region is highly doped with n-type and channel region is moderately doped with p-type. N-polysilicon is used for gate and $HfO_2$ high-$k$ dielectric is used as the gate dielectric. Al contacts are used for source and drain regions. Nitride type spacers are used for the protection of source/drain electrodes from outside environment and reduce the capacitance between gate and source/drain electrodes. The various parameters used in device simulation for $In_{0.53}Ga_{0.47}As$ N-TFET is summarized below in Table 1.

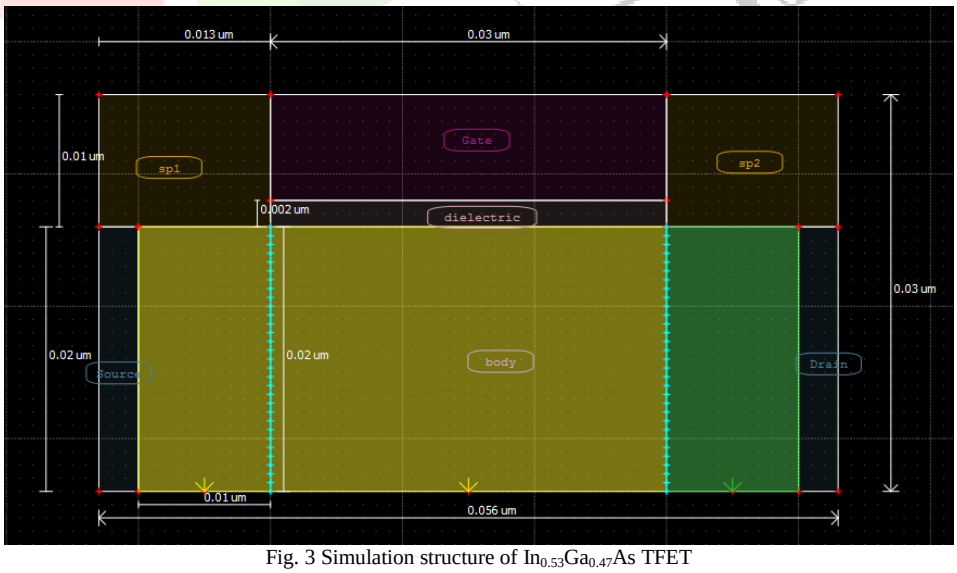


Fig. 3 Simulation structure of $In_{0.53}Ga_{0.47}As$ TFET

Table 1. Various Parameters used in Simulation of $In_{0.53}Ga_{0.47}As$ N-TFET

| Parameter | Value |
|---|---|
| Gate length | 30 nm |
| Thickness of dielectric layer | 2 nm |
| Length of spacers | 13 nm |
| Thickness of spacers | 10 nm |
| Source concentration (p-type) | $10^{20}$ $cm^{-3}$ |
| Drain concentration (n-type) | $10^{18}$ $cm^{-3}$ |
| Channel concentration (p-type) | $10^{16}$ $cm^{-3}$ |

## VI. RESULTS AND DISCUSSION

The simulation of $In_{0.53}Ga_{0.47}As$ TFET was done by using drift-diffusion model with Poisson's equation at 300K. The $I_d$-$V_g$ characteristics of $In_{0.53}Ga_{0.47}As$ TFET is demonstrated and compared with the $I_d$-$V_g$ characteristics of Si MOSFET and Si TFET. The various performance parameters such as threshold voltage, subthreshold swing, DIBL are also investigated.

### 6.1 $I_d$ – $V_g$ characteristics of $In_{0.53}Ga_{0.47}As$ TFET

The $I_d$-$V_g$ characteristic describes the drain current response to the input gate to source voltage. These characteristics are also known as input characteristics and are plotted by keeping source at constant voltage mode (0V), drain at constant voltage mode (0.1V, 0.3V, 0.5V and 0.8V) and gate at voltage sweep mode (start voltage = 0V, stop voltage = 0.8V and step voltage = 0.02V) at work function of 4.3 eV. These characteristics shows the threshold voltage i.e., the voltage at which device leaves the OFF state and current starts conducting through the device. The comparison log plot of $I_d$-$V_g$ characteristics of $In_{0.53}Ga_{0.47}As$ TFET at work function 4.3 eV for $V_d$=0.1V, $V_d$=0.3V, $V_d$=0.5V and $V_d$=0.8V, is shown in Fig. 4. These characteristics showed that the leakage current is minimum when $V_d$=0.1V which make TFETs suitable for ultra-low power applications.

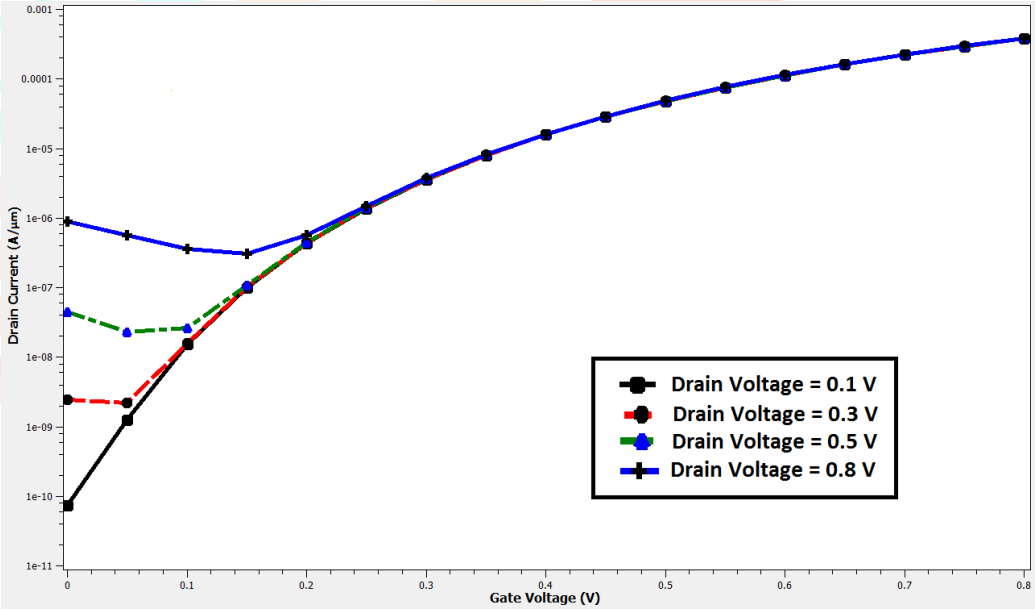


Fig. 4 Log plot of $I_d$-$V_g$ characteristics of $In_{0.53}Ga_{0.47}As$ TFET at different values of $V_d$

The comparison of $I_d$-$V_g$ characteristics of MOSFET and TFET is shown in Fig. 5, form these characteristics, it is evident that the leakage current of TFET is much lower than that of the MOSFET's. However, the drive current of the MOSFET is slightly more than that of the TFET.

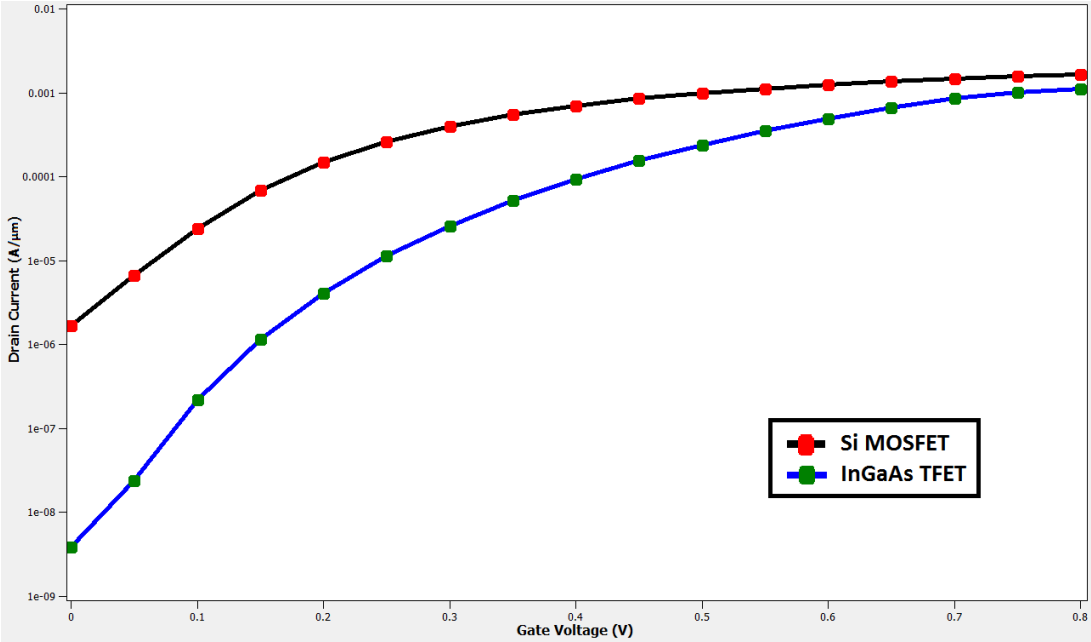


Fig. 5 The comparison log plot of $I_d$-$V_g$ characteristics of TFET and MOSFET

The significant reduction in leakage current and improvement in drive current in InGaAs TFET as compared to Si TFET can be seen in the Fig. 6. The reason for this improvement is the direct bandgap of InGaAs which makes tunneling probability higher.

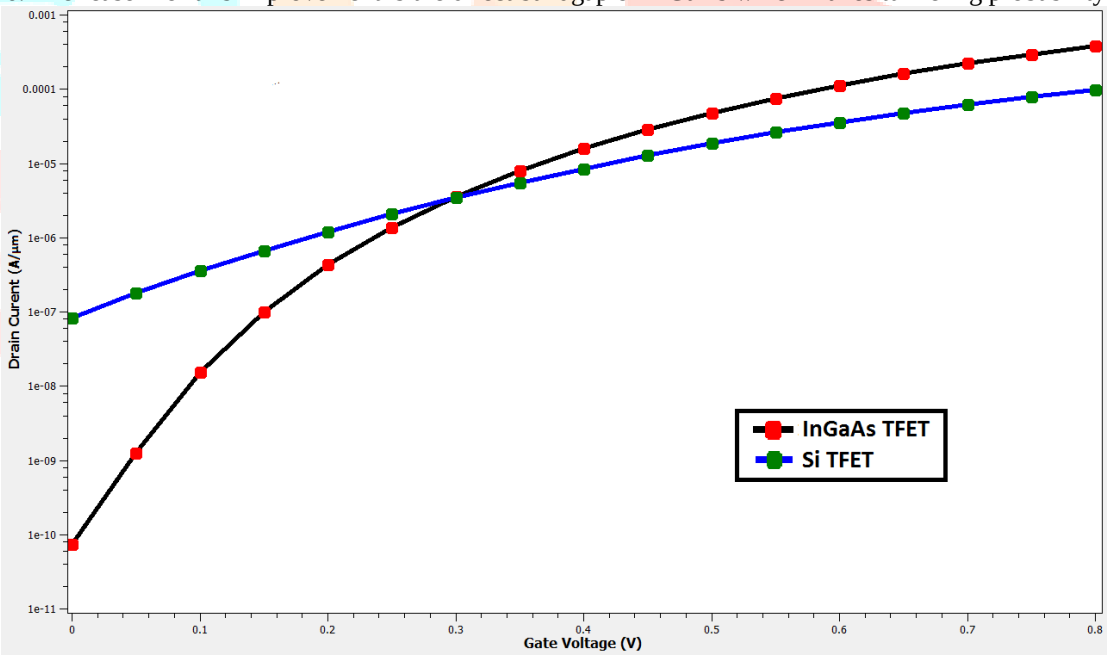


Fig. 6 The comparison log plot of $I_d$-$V_g$ characteristics of InGaAs TFET and Si TFET

Now, constant current threshold voltage method is used in order to calculate threshold voltage, according to which threshold voltage is value of voltage at which current is defined by equation as [15]

$$I_t = W/L * 10^{-7} \text{ A} \quad (2)$$

Here, W is width of the channel and L is length of channel. In this device, W=1µm, L=30nm. Hence, $I_t = 0.33*10^{-7}$A = 30 nA and hence, threshold voltages for $In_{0.53}Ga_{0.47}As$ TFET at $V_d$=0.1V is 0.298V.

The Drain Induced Barrier Lowering (DIBL) is defined by above equation as

$$DIBL = (V_{t\_Lin} - V_{t\_Sat}) / (V_{Sat} - V_{Lin}) \text{ mV/V} \quad (3)$$

Here, $V_{t\_Lin}$ is threshold voltage in linear mode, $V_{t\_Sat}$ is threshold voltage in saturation mode $V_{Sat}$ is voltage in saturation mode and $V_{Lin}$ is voltage in linear mode. Thus, by using this concept, DIBL of $In_{0.53}Ga_{0.47}As$ TFET at work function 4.3 eV is 57.14 mV/V.
In order to calculate subthreshold swing, subthreshold slope method is used, according to which sub threshold swing is calculated by equation as [16]

$$SS = d(V_g) / d(\log I_d)\ mV/dec \qquad (4)$$

Here, $d(V_g)$ is change in gate voltage, $d(\log I_d)$ is one decade increase in the output current. Thus, the subthreshold swing of $In_{0.53}Ga_{0.47}As$ TFET is 44.802 mV/dec.

### 6.2 Contours $In_{0.53}Ga_{0.47}As$ TFET

Contours describes the distribution of various device parameters such as electron density, hole density, net doping, net electric charge etc.

#### 6.2.1 Electron Density Distribution

The electron density distribution explains the distribution of electrons across the device. At $V_{gs}$=0V, its distribution is higher across drain as it is using donor type doping while source and channel are using acceptor type doping. At $V_{gs}$=0.8V, its distribution is higher in the channel because device is in ON state and current is flowing through the device. The electron density distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0V and $V_{gs}$=0.8V is shown in Fig. 7(a) and Fig. 7(b) respectively.

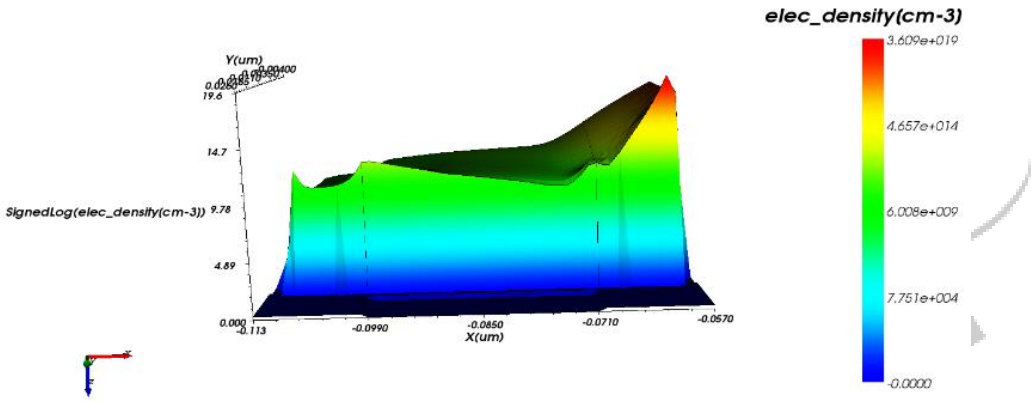


Fig. 7(a) Electron Density Distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0V

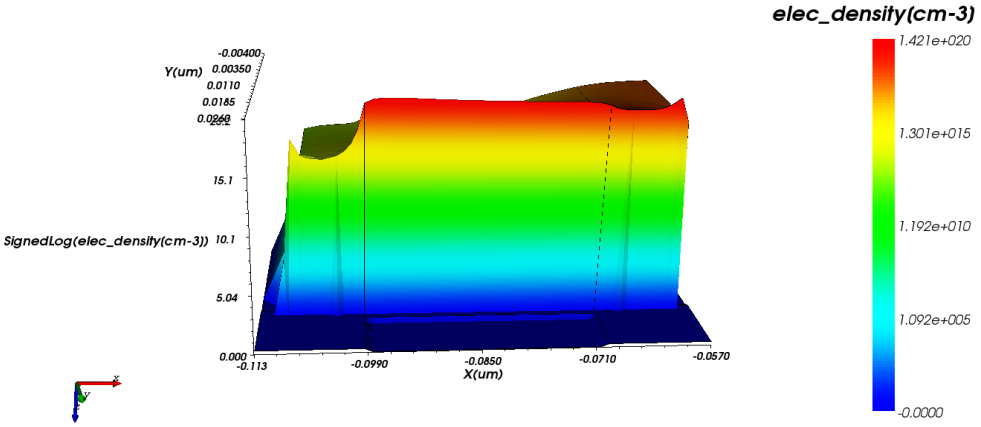


Fig. 7(b) Electron Density Distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0.8V

### 6.2.2 Hole Density Distribution

The hole density distribution explains the distribution of holes across the device. At $V_{gs}$=0V, its distribution is higher across source and channel as they both are using acceptor type doping. At $V_{gs}$=0.8V, its distribution is varying across the body. The hole density distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0V and $V_{gs}$=0.8V is shown in Fig. 8(a) and Fig. 8(b) respectively.

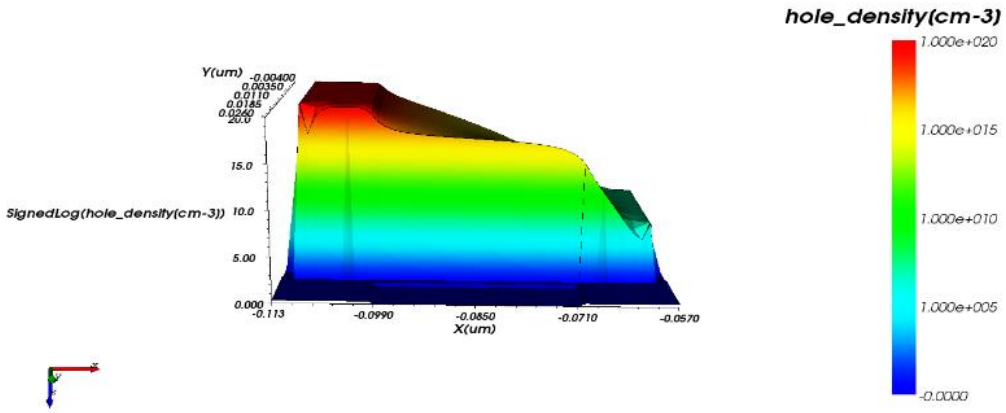


Fig. 8(a) Hole Density Distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0V

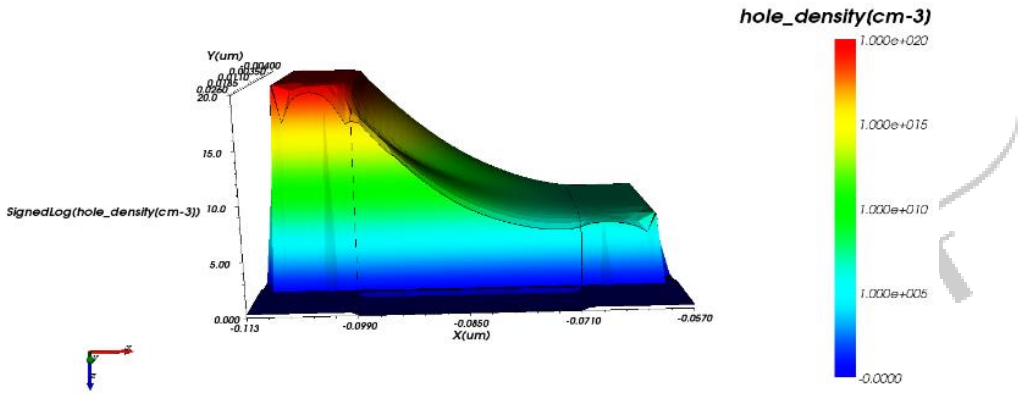


Fig. 8(b) Hole Density Distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0.8V

### 6.2.3 Net Doping Distribution

The net doping distribution explains the productive level of doping done in the device. Here, source is using acceptor type doping of $10^{20}$ $cm^{-3}$ & drain is using donor type doping whose range is $10^{18}$ $cm^{-3}$ while channel is using acceptor type doping whose range is $10^{16}$ $cm^{-3}$. The net doping distribution of $In_{0.53}Ga_{0.47}As$ TFET is shown in Fig. 9.

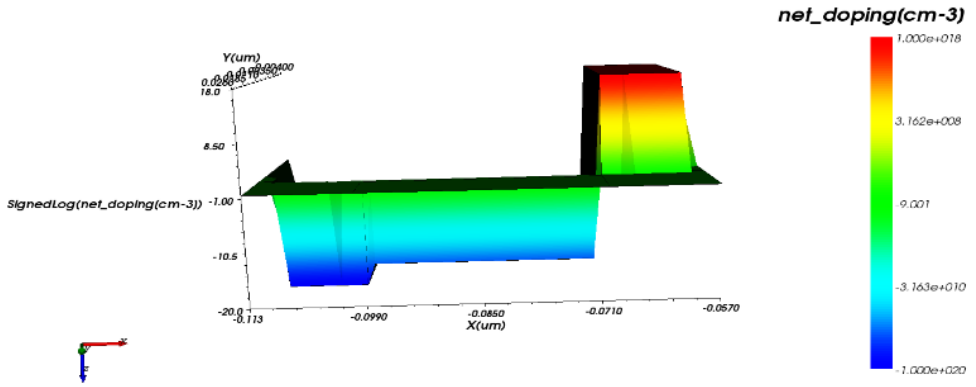


Fig. 9 Net Doping Distribution of $In_{0.53}Ga_{0.47}As$ TFET

### 6.2.4 Net Charge Distribution

The net charge distribution explains the electrostatic charge in the device. At $V_{gs}$=0V, there is no charge in the channel and at $V_{gs}$=0.8V, the net charge in the channel region is high. The net charge distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0V and $V_{gs}$=0.8V is shown in Fig. 10(a) and 10(b) respectively.

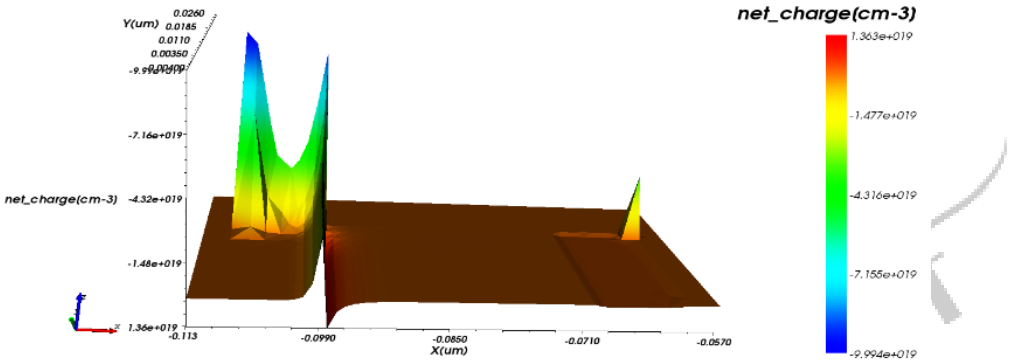


Fig. 10(a) Net Charge Distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0V

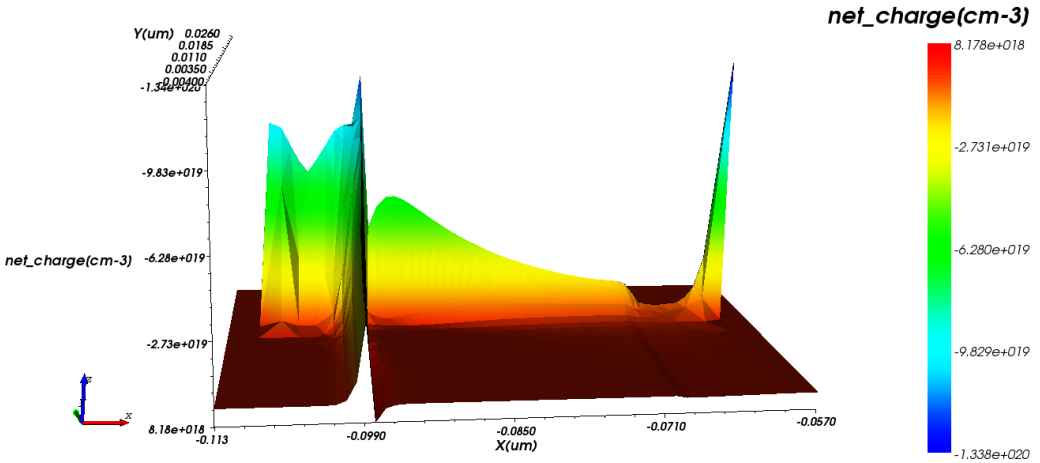


Fig. 10(b) Net Charge Distribution of $In_{0.53}Ga_{0.47}As$ TFET at $V_{gs}$=0.8V

## VII. CONCLUSION

As the dimensions of the MOS devices have continuously scaled down, the performance parameters of the MOSFETs are compromised (because of their basic physical limits), to the extent that a new generation device, which can offer good performance parameters i.e. low power consumption, negligible leakage current and high speed, even in nano-scale regime, is required i.e. Tunnel Field Effect Transistor.

The TFET using $In_{0.53}Ga_{0.47}As$ showed better performance as compared to MOSFET. The threshold voltage and DIBL of proposed device is observed to be 0.298V and 57.14 mV/V respectively. The subthreshold swing of 44.802 mV/dec which is much better than the MOSFET's limit of 60 mV/dec is also observed. It is expected that performance of TFETs can be further improved by reducing diameters, by using smaller bandgap channel materials, optimized doping profile and improving the process of fabrication. Thus, future of TFET is very much encouraging in coming generation.

## REFERENCES


[1] Chander, S. Bhowmick, B. and Baishya, S. 2015. Heterojunction fully depleted SOI-TFET with oxide/source overlap. Superlattices and Microstructures, 86: 43–50.

[2] Nam, H. Cho, M. H. and Shin, C. 2015. Symmetric Tunnel Field Effect Transistor (S-TFET). Current Applied Physics, 15: 71-77.

[3] Avci, U. E. Morris, D. H. and Young, I. A. 2015. Tunnel Field-Effect Transistors: Prospects and Challenges. Journal of the Electron Devices Society, 3(3): 88-95.

[4] Mookerjea, S. Mohata, D. Mayer, T. Narayanan, V. and Datta, S. 2010. Temperature-Dependent I–V Characteristics of a Vertical $In_{0.53}Ga_{0.47}As$ Tunnel FET. IEEE Electron Device Lett., 31(6): 564–566.

[5] Dewey, G. et al. 2011. Fabrication, Characterization, and Physics of III-V Heterojunction Tunneling Field Effect Transistors (H-TFET) for Steep Sub-Threshold Swing. IEEE International Electron Devices Meeting (IEDM), 33.6.1 - 33.6.4.

[6] Vishnoi, R. and Kumar, M. J. 2015. An Accurate Compact Analytical Model for the Drain Current of a TFET from Sub-Threshold To Strong Inversion. IEEE Trans. on Electron Devices, 62: 478-484.

[7] Wang, P. Zhuang, Y. Ii, C. and Jiang, Z. 2014. Analytical Modeling for Double-Gate TFET with Tri-Material Gate. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT).

[8] Zhou, G. et al. 2012. InGaAs/InP Tunnel FETs with a Subthreshold Swing of 93 mV/dec and $I_{ON}/I_{OFF}$ Ratio Near $10^6$. IEEE Electron Device Letters, 33(6): 782-784.

[9] Praveen, C.S. Ravindran, A. John, S. K. and Abe, S. 2015. Gate Engineering of Double Gate $In_{0.53}Ga_{0.47}As$ Tunnel FET. ICTACT Journal on Microelectronics, 1(3): 91-95.

[10] Kardam, U. Saxena, M. Narang, R. and Gupta, M. 2013. Simulation Study for Dual Material Gate Hetero-Dielectric TFET: Static Performance Analysis for Analog Applications. Annual IEEE India Conference (INDICON).

[11] Zhao, H. et al. 2011. InGaAs Tunneling Field-Effect-Transistors with Atomic-Layer-Deposited Gate Oxides. IEEE Trans. Electron Devices, 58(9): 2990–2995.

[12] Hurkx, G. A. M. Klaassen, D. B. M. and Knuvers, M. P. G. 1992. A New Recombination Model for Device Simulation including Tunneling. IEEE Transactions on Electron Devices, 39(2): 331-338.

[13] Guo, P. et al. 2012. Tunneling Field Effect Transistor (TFET) with Novel Ge/$In_{0.53}Ga_{0.47}As$ Tunneling Junction. ECS Transactions, 50(9): 971-978.

[14] Lu, H. and Seabaugh, A. 2014. Tunnel Field Effect Transistor: State-of-the-Art. Journal of the Electron Devices Society, 2(4): 44-49.

[15] Loke, A. et. al. 2010. Constant-Current Threshold Voltage Extraction in HSPICE for Nanoscale CMOS Analog Design. Advanced Micro Devices Incorporation, 55(3).

[16] Boucart, K. and Ionescu, A. M. 2007. Double-Gate Tunnel FET with High-k Gate Dielectric. IEEE Transactions on Electron Devices, 54(7): 1725-1733.