Performance Enhancement using Carbon Nanotube CNTFET in digital circuit designs

[1]K. Miranji, [2]Danduboyina Lakshmi.
Assistant Professor, Dept. of ECE, Sir C.R.Reddy college of engineering, Andhra University, Andhrapradesh, India.

Abstract: Carbon Nanotube plays a major role in electronic industry to produce large number of electronic devices. The main reason behind is the dimension of CNT in nanometer size. Carbon Nanotube filed-effect transistor (CNTFET) is one of the promising alternatives to the MOS transistors. The geometry-dependent on threshold voltage are one of the CNTFET characteristics, which are used to design parallel adder. This paper presents a low voltage and high performance 4-bit parallel adder which is used to reduce the power delay product (PDP).This technique is mainly implemented by using static energy recovery full adder based on CNTFET model where we can reduce the power consumption and delay. Full adder is designed using 10 transistors. Simulation results show significant improvement in terms of power, delay and power-delay product in comparison between FA and PA .Simulations were carried out using HSPICE based on CNTFET model with 0.7v and 0.9v VDD.

Keywords: Parallel adder, Full adder, Carbon Nanotube, Carbon Nanotube Field Effect Transistor, High speed, High performance.

I. Introduction

Carbon Nanotubes (CNTs) are members of the carbon family of fullerenes that was discovered by Sumino Iijima, a Japanese scientist, as the elongated fullerenes in 1991. He used a high-resolution transmission electron microscopy to observe CNT directly [1]. Carbon Nanotube becomes a pioneer in the electronics industry during the first day of its invention. The main reason behind is the dimension of CNT in nanometer size. CNTs are promising for many applications due to their excellent electrical properties [2]. Chirality of graphene has a huge impact on developing the Nanotube as a metallic or semiconducting type based on their different indices [3]. With the semiconducting properties, Nanotube contributes a large number of electronic devices productions such as, sensors, transparent conducting coatings [4], film transistors [5], displays [6], and solar cells [7]. Therefore CNTs become potential research to the scientist by developing the field effect transistor. As a promising candidature CNTFET overcome the limitation of MOSFET device.

II. CNTFET

As the technology grows the demand for scaling down has increased. The CMOS shows various false effects of scaling down. Some of them are short channel effects, hot carrier effect and drain induced barrier lowering. Due to these effects a new device has been introduced named CNTFET [8]. Carbon Nanotube field effect transistor (CNTFET) is the very effective technology to extend due to [9],[10],[11] three reasons.

1) The operation principle and the device structure are similar to CMOS devices. We can reuse the established CMOS design infrastructure.

2) We can reuse CMOS fabrication process. The most effective reason is that CNTFET [14] has the best experimentally demonstrated current carrying ability till today.

The carbon Nanotubes are formed of graphene sheet. Graphene has advantages of being soft and mechanically strong which make it a suitable component of carbon over diamond for CNT manufacturing. CNTFET offers

1) Ballistic transport, i.e. current flows only in forward or backward direction. There is no scattering of electrons due to collision because CNT is a hollow tube. So scattering of electrons is almost negligible.

2) Almost negligible leakage current.

3) High tolerance to temperature.

4) High conductivity [12] [13].

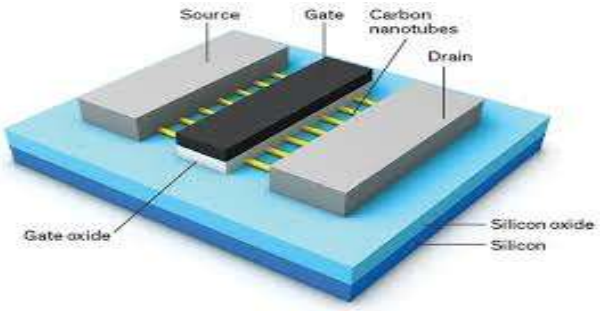


Figure 1: CNTFET Structure.

III. Parallel Adder

This paper presents a low voltage and high performance 4-bit parallel adder implemented by using static energy recovery full adder based on CNTFET model. Here a parallel adder is taken as an example for a full adder, with a 4-bit value and each single bit full adder consists of 10 transistors [15] as shown in fig 4. It has total of 40 transistors. Here all the four bits are connected in parallel so as to perform sum and carry is shown in fig2. In practical situations the least significant bits A0, B0, and CIN are added to the produce sum output SUM0 and carry output C0.Carry output C0 is then added to the next significant bits A1 and B1 producing sum output SUM1 and carry output C1. C1 is then added to A2 and B2 and so on. Thus finally producing the four-bit sum output SUM0 SUM1 SUM2 SUM3 and final carry output C3.

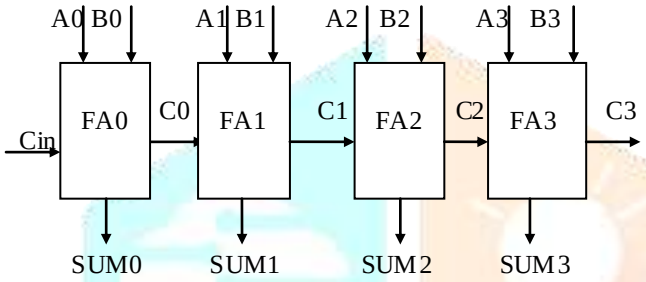


Figure2: Cascading of four Full Adder Circuits.

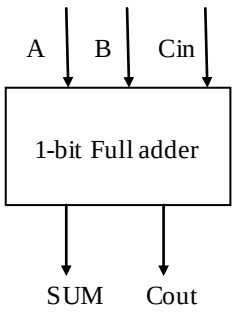
IV. Full Adder

The adder is one of the most critical components of a processor, as it is used in the Arithmetic Logic Unit (ALU). Increasing demand for mobile electronic devices such as cellular phones and laptop computers requires the use of power efficient VLSI circuits.

The full adder operation can be stated as follows: Given the three 1-bit inputs A, B, and Cin. It is desired to calculate the two 1-bit outputs Sum and Cout, where

Sum= (A XOR B) XOR Cin ……. (1)
Cout= AB+BC+CA …….. (2)

Schematic diagram and Truth table for 1-bit Full adder is shown in fig3.



A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig3: Schematic diagram and Truth table of 1-bit Full Adder.

V. Static Energy Recovery Full adder (SERF)

The Static Energy Recovery Full Adder (SERF) [15] uses only 10 transistors to implement the full adder function. The design was inspired by the XNOR gate full adder design. The structure of SERF is given in figure 4. In non-energy recovery design the charge applied to the load capacitance during the logic level high is drained to ground during logic level low. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to ground reduces power consumption, removing the Psc variable (Product of Isc and Voltage) from the total power equation. The charge stored at the load capacitance is reapplied to the control gates, the combination of not having a direct path to ground and re-application of the load charge to the control gate makes the energy – recovering full adder an energy efficient design but it has the threshold loss problem. To the best of our knowledge this new design has the lowest transistor count for the complete realization of a full adder. The performance of the SERF full adder cell is compared for power consumption, delay and Power delay product (PDP) against Parallel adder for different voltages 0.7v and 0.9v VDD.

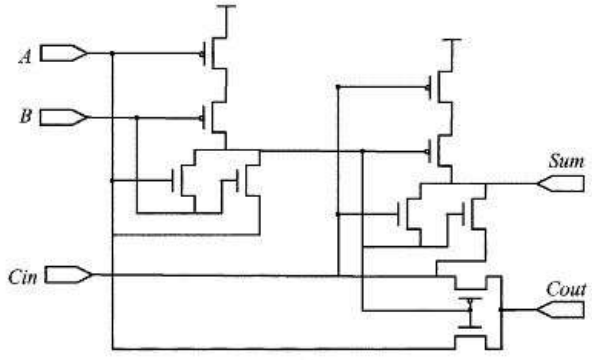


Fig4: Structure of SERF adder.

VI. Simulation Results

In this paper work we will use HSPICE version A-2008.03. HSPICE will be used for coding and simulation. Synopsys HSPICE is an optimizing analog circuit simulator. You can use it to simulate electrical circuits in steady-state, transient, and frequency domains. HSPICE is

used for fast and accurate circuit simulation [16]. The simulation is carried out on 7nm and 20nm technology for 0.7v, 0.9v of power supply. Temperature is taken 25 degree Celsius.

Fig5: Simulation result for Static Energy Recovery Full adder (SERF) 7nm Technology.

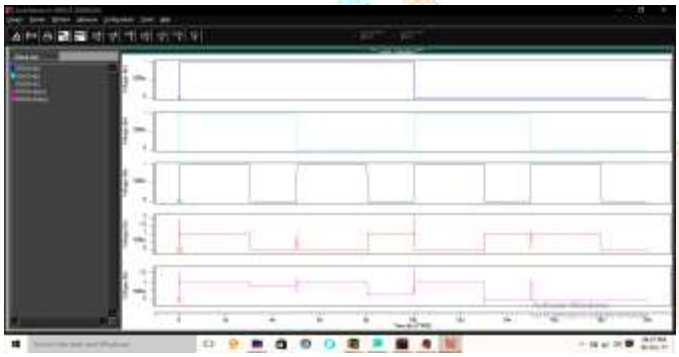


Fig5: Simulation result for Static Energy Recovery Full adder (SERF) 20nm Technology.

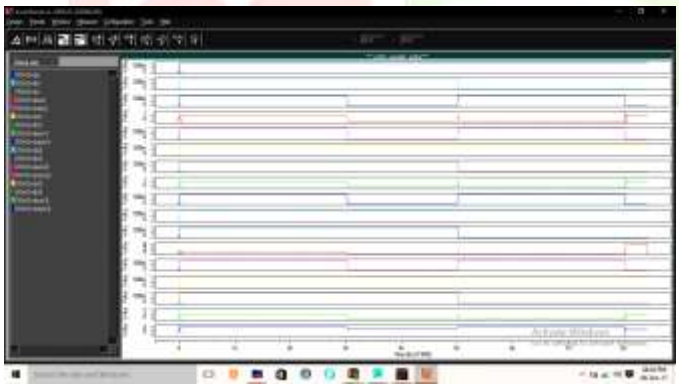


Fig6: Simulation result for Parallel adder for 7nm Technology.

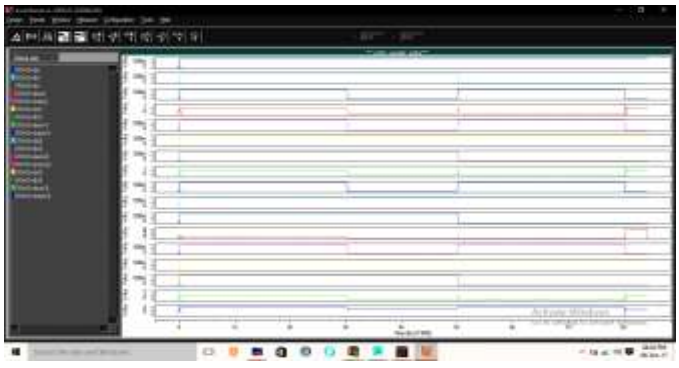


Fig6: Simulation result for Parallel adder for 20nm Technology.

Table1: Parameters Calculation of Full adder for 7nm and 20nm technology.

Power Supply	0.7v	0.9v
Power(w)	1.3298E-07	2.8787E-09
Delay(s)	1.8E-09	5.5E-12
Power Delay Product(PDP)	2.39E-16	1.5E-20

Table2: Parameters Calculation of Parallel Adder for 7nm and 20nm technology.

Power Supply	0.7v	0.9v
Power(w)	2.1508E-07	1.0310E-08
Delay(s)	45E-09	140E-12
Power Delay Product(PDP)	9.6E-15	1.44E-18

VII. Conclusion

In this paper the Low voltage and High Performance 4-bit parallel adder has implemented using Static Energy Recovery Full adder (SERF) based on CNTFET technology. The designed FA and PA are simulated in HSPICE A-2008.03. Full adder is designed based on XNOR gate. It performs significant advantages in the reduction of the circuit complexity low power consumption, delay and PDP and increased speed.

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VIII. References

[1] Iijima, S. (2002). Carbon Nanotube: past, present, and future.

[2]S. Hong & S. Myung (2007). Nanotube Electronics: A flexible approach to mobility. Nature Nanotechnology, *2*(4), 207-208.

[3]D. M. Guldi, & Martin, N. (Eds.). (2010). Carbon Nanotube and related structures: synthesis, characterization, functionalization, and applications. John Wiley & Sons.

[4]Kaskela.A, Nasibulin A. G., Timmermans M. Y., Aitchison, B., Papadimitratos, A., Tian, & Kauppinen, E. I. (2010). Aerosolsynthesized SWCNT networks with tunable conductivity and
Transparency by a dry transfer technique. Nano Letters, *10*(11), 4349- 4355.

[5] Sun, D. M., Timmermans, M. Y., Tian, Y., Nasibulin, A. G., Kauppinen, E. I., Kishimoto, & Ohno, Y. (2011). Flexible highperformance carbon nanotube integrated circuits. Nature nanotechnology, *6*(3), 156-161.

[6] Wang, C., Zhang, J., Ryu, K., Badmaev, A., De Arco, L. G., & Zhou, C. (2009). Wafer-scale fabrication of separated carbon Nanotube thin-film transistors for display applications. Nano Letters, *9*(12), 4285-4291.

[7] Rowell, M. W., Topinka, M. A., McGehee, M. D., Prall, H. J., Dennler, G., Sariciftci, N. S., & Gruner, G. (2006). Organic solar cells with carbon nanotube network electrodes. Applied Physics Letters, *88*(23), 233506.

[8] Ali Ghorbani and Ghazaleh Ghorbani, energy efficient full adder cell design with using carbon nanotube field effect transistors in 32 nanometer
Technology, Vol.5, No.5, October 2014.

[9] J. Deng, Device Modeling and Circuit Performance Evaluation for Nanoscale Devices: Silicon Technology beyond 45 nm Node and Carbon Nanotube Field Effect Transistors, doctoral 2007.

[10] M.H. Moaiyeri, K. Navi, and O. Hashemipour, "Design and Evaluation of CNFET-Based Quaternary Circuits," Circuits, Syst.,Signal Process., vol. 31, no. 5, Oct. 2012, pp. 1631-1652.

[11] P A Aui, K M Lal, MJ Siddiqui, carbon nanotubes field effect transistor: vol.43, Dec 2005,pp. 899-909.

[12] Dafeng Zhou, Circuit-level Modelling and Simulation of Carbon Nanotube Devices, 2010.

[13] Djamil RECHEM and Saida LATRECHE, Nanotube Diameter Effect on the CNTFET Performances, 5th International Conference: March 22-26, 2009 – TUNISIA.

[14] Aliakbar Rezaei, Mehdi Masoudi, Fazel Sharifi, Keivan Navi, A Novel High Speed Full Adder Cell based on Carbon Nanotube FET (CNFET), Int. J. Emerg. Sci.(IJES), issue 4(2),pp. 64-74, June 2014.

[15] J. F. Lin, Y. T. Hwang, M. H. Sheu, and C. C. Ho, (2007) "A novel high-speed and energy efficient 10-transistor full adder design," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 54, no. 5, pp. 1050-1059.

[16]"HSPICE User Guide: Simulation and Analysis" Version B 2008.09.