A Third Harmonic Injection PWM controlled novel ZVS single phase full bridge inverter with dynamic load

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ABSTRACT

In a ZVS single full bridge inverter with dynamic load with THI PWM is employed. The THIPWM (Third Harmonic injection Pulse Width Modulation) generates more voltage as compared to traditional SPWM. The ZVS THIPWM is evolved from the double-frequency THIPWM by adding gate drive to the auxiliary switch. The ZVS condition is analyzed and the circulation loss of the resonant branch is optimized by adjusting the energy storage in the resonant inductor. The reverse recovery of the body-diode of MOSFET is relieved and ZVS is realized for both main and auxiliary switches. The filter inductors are significantly reduced with higher switching frequency. The design guideline of resonant parameters and the implementation of ZVS THIPWM with dynamic load in MATLAB software are given with graphical representation and reports.

I. INTRODUCTION

With ZVS operation, it is possible to operate the converter with high switching frequency using MOSFETs so that its size can be reduced without generating excessive switching losses. Under lighter load conditions, however, the converter switches cannot turn ON with ZVS as there is insufficient current to discharge their output capacitances. Many researchers, therefore, have proposed variations on the basic ZVS-PWM-FB topology to extend the load range of ZVS operation.

Some of these topologies use extra passive components to generate current in the converter's primary side to discharge the output capacitances of the switches [1]–[7]. This additional current, however, creates conduction losses that offset gains in efficiency due to ZVS operation so that the net converter efficiency is less than expected. Another approach has been to add active components to the standard topology [8]–[11], either on the primary side [8]–[10] or the secondary side [11]. With this approach, the current needed to discharge the output capacitances of the switches under light-load conditions can be generated without increasing conduction losses significantly. This occurs because this generated current flows in the converter for only a small fraction of the switching cycle, just before and after a switching transition has been made.

Although ZVZCS PWM FB converters have these two key advantages over ZVS-PWM FB converters, they have one major drawback—extinguishing the freewheeling mode current eliminates the ability of the lagging leg switches to turn on with ZVS as there is no current available to discharge their output capacitances before they are turned on. As a result, these lagging leg switches are implemented with IGBTs (which have lower output capacitances than MOSFETs) to limit turn-on losses, but IGBTs cannot turn on and off as fast as MOSFETs and there is increased cost associated with having to implement the converter with two different types of switches instead of just one type.

According to the predecessors' research, the dc side ZVS full-bridge inverters [10], [11] have the simplest structure. With this principal advantage, this paper mainly focuses on improving the efficiency and power density of dc side ZVS full-bridge inverter. The ZVS full-bridge inverter is based on the topology proposed in [10]. High circulation loss is found with existing modulation scheme. In order to optimize the efficiency, a novel ZVS SPWM scheme is proposed. For the purpose of realizing the ZVS condition, an adjustable short-circuit stage controlled by the short-circuit pulse in every switching cycle is designed to reset the energy in the auxiliary resonant branch [20], [21]. The duration of the short-circuit stage varies according to the different load condition for optimizing the efficiency in both light and heavy load cases. The ZVS condition will be analyzed and the design procedure for the ZVS SPWM will be presented in this paper. MOSFETs are utilized and zero-voltage switching for both main and auxiliary switches is realized. The filter is reduced with higher switching frequency and a 3 kW prototype is built to verify the theoretical analysis.

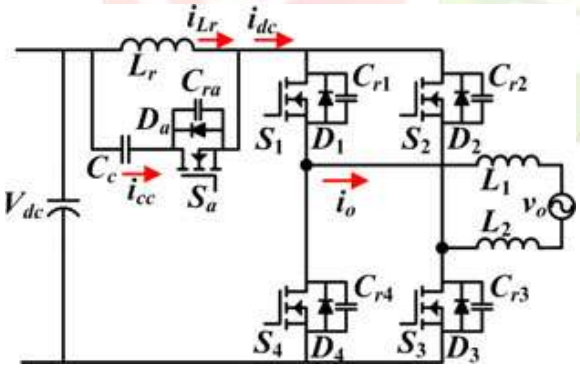

Fig. 1: ZVS full bridge inverter

II. CONTROL STRATEGY

The operation stages with the proposed ZVS THI PWM are given as follows. The switching waveforms in a switching period and operation circuits are shown in Fig 2. The analysis is based on the steady operation state. The output filters (L_1 and L_2) and the clamping capacitor (C_c) is supposed to be large enough so the load current and the voltage across the clamping capacitor (V_{cc}) could be treated as constants in a switching period. The resonant capacitor paralleled with MOSFET represents the parasitic capacitance and the external capacitor. The resonant capacitors of the main switches have equal capacitance.

Stage 1 (Freewheel, $t_0 - t_1$): The load current i_o is freewheeling through the main switches S_3 and S_4. The voltage across the resonant inductor L_r is clamped to $-V_{cc}$ and the slope of its current i_{Lr} is

$$\frac{di_{Lr}}{dt} = -\frac{V_{cc}}{L_r} \quad \text{.....(1)}$$

Stage 2 (Freewheel, t_1–t_2): The main switch S_4 is turned off at t_1 by SPWM. The load current i_o is freewheeling through the main switch S_3 and the body diode D_4

Stage 3 (Resonance, $t_2 - t_3$): The gate-source voltage (v_{gsa}) of auxiliary switch S_a is set to zero at t_2 by ZVS SPWM. The drain-source channel of S_a is turned off rapidly. The resonant capacitors C_{r1} and C_{r2} are discharged while C_{ra} is charged by the resonant inductor. The initial resonant current i_{Lr} at t_2 is defined as I_{res1}. During the resonant process the current i_{Lr} reaches its minimum value I_{min}. Stage 3 ends when the voltage across capacitors C_{r1} and C_{r2} is discharged to zero.

Stage 4 (Charging, $t_3 - t_4$): After the voltage of main switches S_1 and S_2 resonates to zero, the body-diodes (D_1 and D_2) turn on. The voltage of both phase legs is clamped to zero and the ZVS turn-on of main switches S_1 and S_2 is achieved. The across the resonant inductor (L_r) voltage is clamped to V_{dc}. The current in resonant inductor begins to increase and the slope is

$$\frac{di_{Lr}}{dt} = \frac{V_{dc}}{L_r} \quad \text{.....(2)}$$

Then the short-circuit pulse is sent to all the main switches before the current in resonant inductor increases to zero and Stage 4 is finished.

Stage 5 (Short-Circuit and Charging, $t_4 - t_5$): Main switchesS_1, S_2 and S_4 are ZVS turned on by the short-circuit pulse at t_4 . The current i_{Lr} keeps increase through the MOSFETs with the same slope. The body-diodes are bypassed because of the low on resistance of MOSFET and the reverse recovery is relieved. At t_5, the current i_{Lr} is equal to I_{sc}.

Stage 6 (Resonance, $t_5 - t_6$): At t_5, the short-circuit pulse Vsc is removed from all the main switches. S_1 and S_3 keep turning on by the high level drive pulse of DF SPWM. The drain-source channels of S_2 and S_4 are turned off rapidly without the short-circuit pulse. Then capacitors C_{r2} and C_{r4} are charged while C_{ra} is discharged by the resonant inductor. The current in resonant inductor i_{Lr} reaches its maximum value I_{max} during the resonant process. Stage 6 ends when the voltage across capacitor C_{ra} is discharged to zero. The load current i_o flows through main switches S_1 and S_3 and the commutation from the body-diode D_3 to main switch S_1 finishes.

Stage 7 (Clamping, $t_6 - t_7$): The body-diode (D_a) of auxiliary switch turns on at t_6. The drain-source voltage v_{dsa} is clamped to zero and the voltage across the resonant inductor is $-V_{cc}$. The dc voltage source begins to transfer energy to the grid.

Stage 8 ($t_7 - t_8$): The auxiliary switch S_a is ZVS turned on at t_7. The durations from t_6 to t_8 depend on the SPWM.

Stage 9 ($t_8 - t_9$): The drain-source channel of S_3 is turned off rapidly at t_8 by SPWM. The charging of capacitor C_{r3} and the discharging of capacitor C_{r2} both help the ZVS turn-on of main switch S_2 and ZVS turn-off of main switch S_3.

Stage 10 ($t_9 - t_{10}$): The voltage across resonant capacitor C_{r2} is discharged to zero by the load current i_o and the body-diode (D_2) of main switch S_2 turns on at t_9. Main switch S_2 is ZVS turned on by THI PWM at t_{10}. The duration of stage 9 and stage 10 ($t_8 \sim t_{10}$) is the dead-time of SPWM.

Stage 11 ($t_{10} - t_{11}$): Main switch S_2 is ZVS turned on by the THI PWM. This stage is similar to stage 1

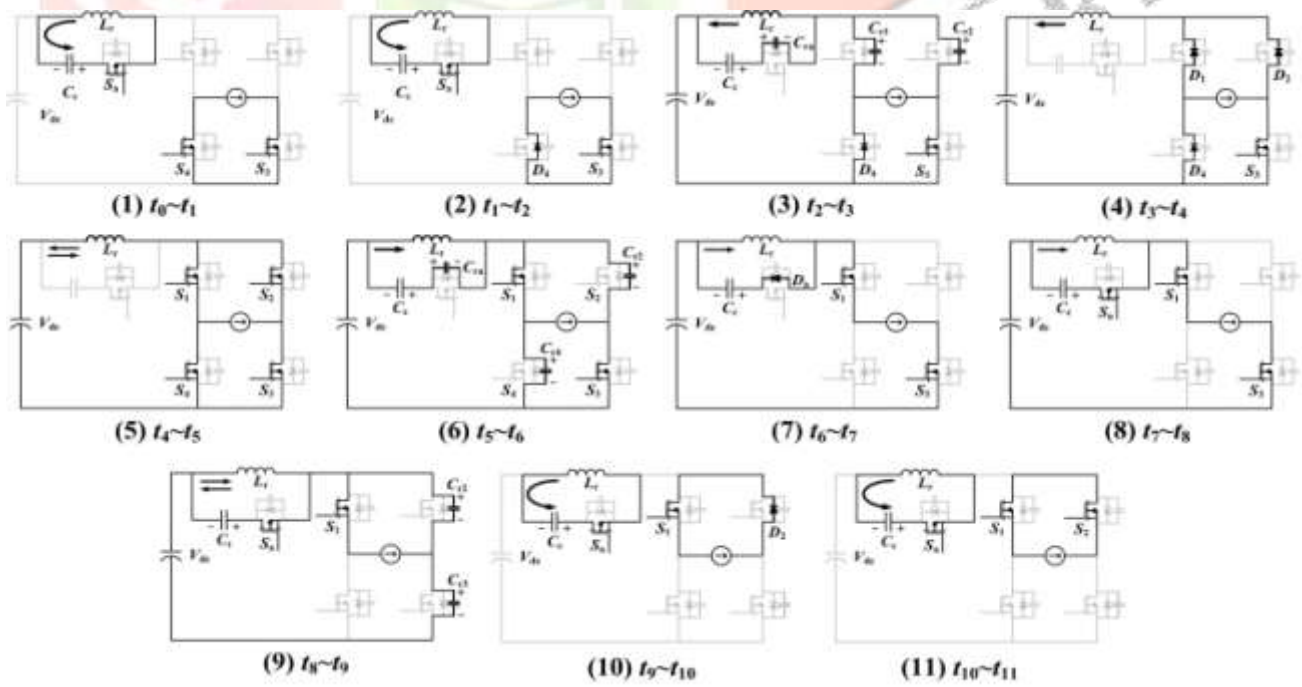

Fig. 2: Mode of operation for proposed topology

III. Third Harmonic Injection (THI) PWM

The third–harmonic PWM is analogous to the selected harmonic injection strategy and it is executed in an indistinguishable way from sinusoidal PWM. The distinction is that the reference signal (V_r) is not sinusoidal however comprises of both a fundamental signal component (V_1) and a third-harmonic signal component (V_3). Subsequently, the resulting reference function from the peak-to-peak voltage amplitude of waveform does not surpass the DC supply voltage V_s, but rather the fundamental component is higher than the accessible supply V_s. The reference voltage V_r is included with signal having frequency three times of fundamental frequency and the magnitude is 1/6th of the fundamental amplitude.The output voltage generated by THI PWM strategy is 1.15 times the output generated by SPWM.

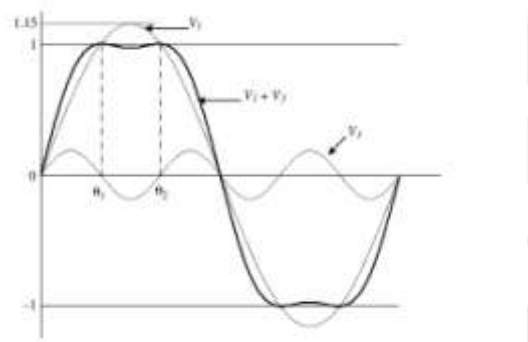

Fig: 3: Third Harmonic Injections to the Reference Signal

The amplitude peak of the reference signal of THI PWM is reduced as it is a flat-topped waveform. Due to which, the linear modulation index increases and the width of the pulses also increase. Thereafter, the magnitude of the output voltage increases. The number of pulses generated reduces and the switching losses become low.

The sinusoidal PWM is the simplest modulation strategy to understand but the DC bus supply voltage is not completely utilized. Because of this issue, the THI PWM technique is employed to enhance the inverter execution. The sinusoidal PWM method causes diminish most extreme output voltage. For this situation, an expansion of most extreme achievable output voltage is studied. Subsequently, by essentially adding a third harmonic signal to each of the reference signals, it is conceivable to acquire a noteworthy adequacy increment at the output voltage without loss of quality, as represented in Figure 3.

On the other hand, the reference signal takes two maxima at wt = π/3 and wt = 2π/3 equal to 1. The first and third harmonic equations are given by

$$V_1 = V_{1max} \sin wt \quad \text{.....(3)}$$

$$V_3 = V_{3max} \sin(3wt) \quad \text{.....(4)}$$

Therefore, when wt= π/3, the first harmonic of the output voltage (line to neutral) takes the value $V_{bus}/2$. By substituting in Equation [4] , we find

$$V_{bus}/2 = V_{1max} \sin(\pi/3) \quad \text{.....(5)}$$

Accordingly, the amplitude of the first harmonic results

$$V_{1max} = V_{bus}/1.732 \quad \text{.....(6)}$$

We see that the quality of the voltage waveform has not been significantly degraded. For each phase reference, the third harmonic injected is equal

$$V_{1max} \sin wt + V_{3max} \sin(3wt) \quad \text{.....(7)}$$

The equation (7) represents the THI PWM for phase voltage injected into the PWM.

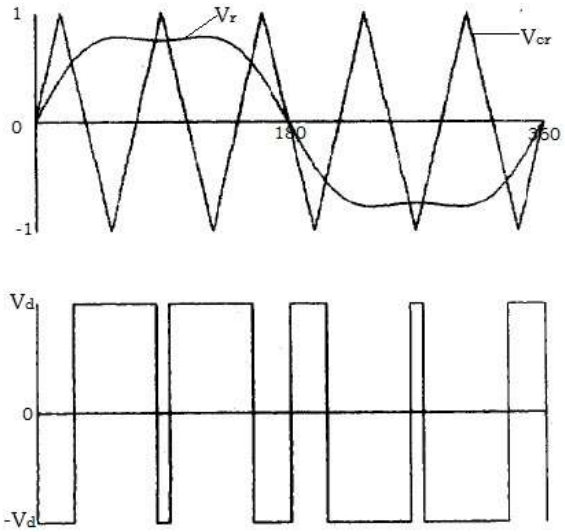

Fig.4: Generation of THI PWM pulses

The generation of gate pulses through THI PWM strategy is represented in the above fig. The frequency of reference signal decides the frequency of inverter. The carrier signal frequency is higher than the reference signal by which the number of gate pulses is generated. The THI PWM strategy provides better output voltage than SPWM and the number of pulses are reduced due to which switching losses becomes low.

Sinusoidal PWM (SPWM)

The SPWM technique is used to provide sinusoidal output voltage by varying the width of the pulses. The SPWM is generated by comparing sine reference signal with the triangular carrier signal. The frequency of triangular carrier waveform is higher than that of the reference signal which generates varying pulses to trigger the power electronic switch to obtain sinusoidal output voltage.

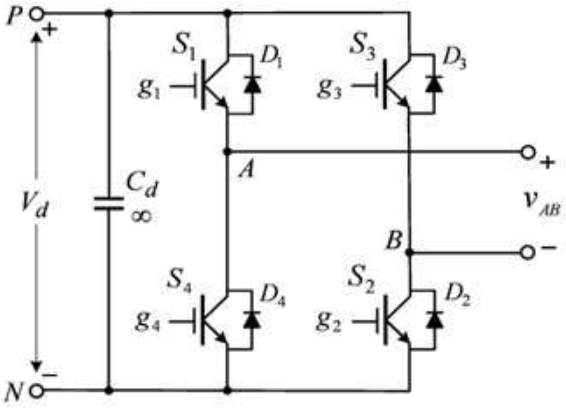

Fig. 5: Single phase full bridge inverter

The full bridge inverter of single phase configuration is represented in the fig. The terminals PN represent the DC link voltage or input DC link at the input of the inverter. The terminals AB represent the output voltage terminals of the inverter.

The switches S_1, S_2, S_3 and S_4 are triggered by applying gate pulses with the SPWM technique to achieve the AC output voltage and the diodes D_1, D_2, D_3, D_4 are connected in anti-parallel to the switches in order to bypass the currents during turn-off of the switch. The SPWM switching waveforms and the output waveform are represented in the fig6.

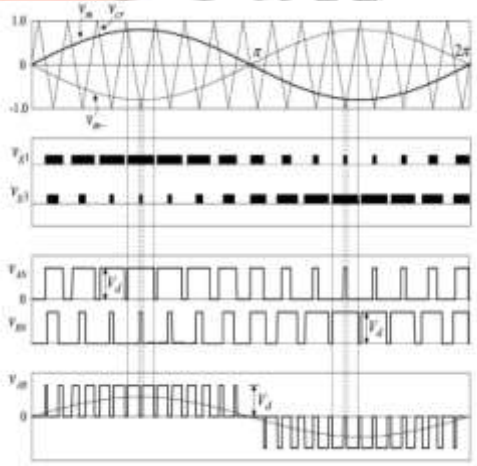

Fig. 6: SPWM Gate pulses for Single phase inverter

The SPWM with unipolar modulation is employed to reduce switching losses as the output voltage of inverter switches from 0 to $+V_d$ during positive cycle and from 0 to $–V_d$ during negative

half cycle. The output voltage waveform is represented with output pulses in the fig 6.

IV. SIMULINK RESULTS AND OUTPUTS

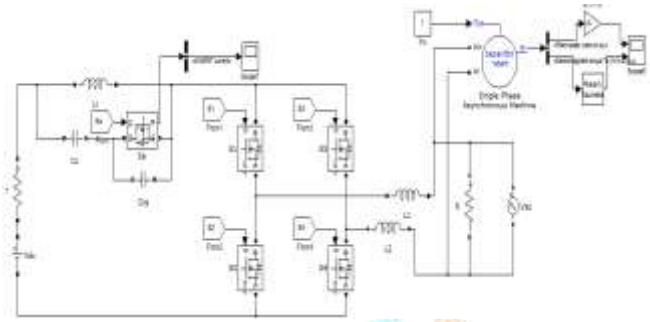

Fig. 7: Simulink modeling of proposed topology

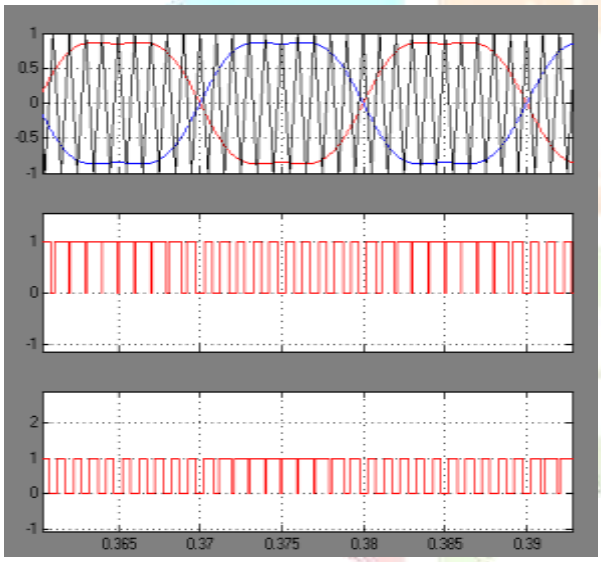

Fig. 8: Third harmonic injection pulses and reference waveforms

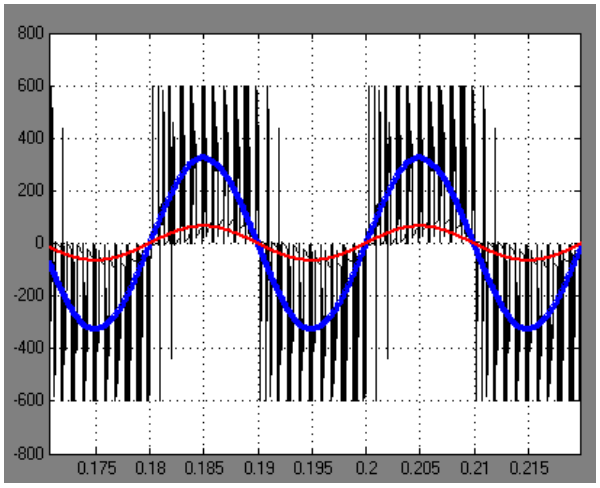

Fig. 9: PWM AC with load voltage and current waveforms

The simulation results of the proposed topology have been represented with the MATLAB simulation results where the increase in output voltage with THI and SPWM is compared and represented in fig. 10. The characteristics of the Asynchronous machine of single phase have been represented in fig 11.

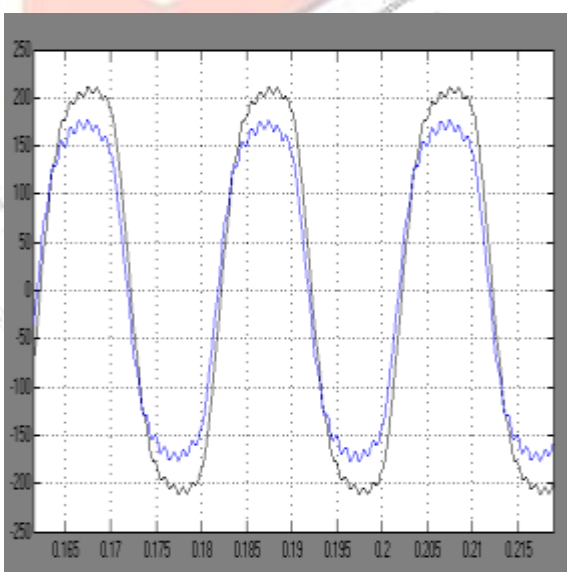

Fig. 10: Comparison of SPWM and THIPWM voltages

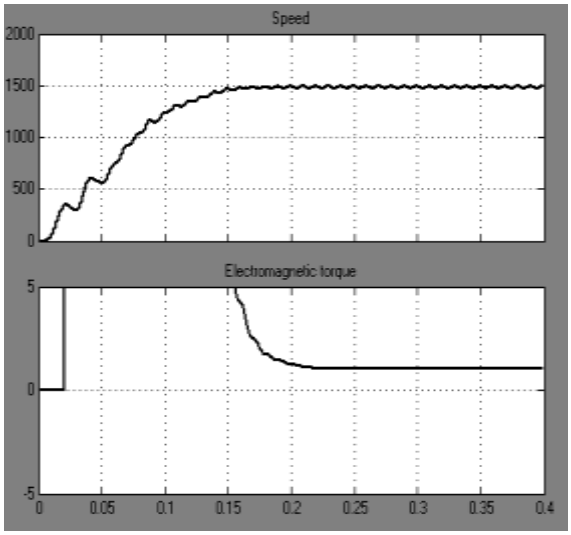

Fig. 11: AC machine characteristics

V. CONCLUSION

With the above results of the proposed topology of the THIPWM compared to SPWM the voltage output of the THIPWM has higher amplitude as compared to traditional PWM technique. The efficiency of the converter also improvises, making the AC motor characteristics more efficient and reduced ripple content.

REFERENCES

[1]P.K.Jain,W.Kang,H.Soin,andY.Xi,"Analysisanddesignconsiderationsofaloadandlineindependentzerovoltageswitchingfullbridge DC/DCconvertertopology,"IEEETrans.PowerElectron.,vol.17,no.5,pp.649–657,May2002.

[2]Y.D.Kim,C.E.Kim,K.M.Cho,K.B.Park,andG.W.Moon,"ZVSphaseshiftfullbridgeconverterwithseparatedprimarywinding,"inProc. IEEEEnergyConvers.Congr.Expo.,2009,pp.484–489.

[3]I.LeeandG.Moon,"Soft-switchingDC-DCconverterwithafullZVSrangeandreducedoutputfilterforhigh-voltageapplications,"IEEETrans. PowerElectron.,vol.28,no.1,pp.112–122,Jan.2013.

[4]C.Yufang,H.Wencong,L.Lirong,andW.Danwen,"ResearchontheZVS-PWMfull-bridgeconverterbasedonUC3875,"inProc.Asia-Pacific PowerEnergyEng.Conf.,Mar.25–28,2011,pp.1–4.

[5]Z.Chen,B.Ji,F.Ji,andL.Shi,"Analysisanddesignconsiderationsofanimproved ZVSfull-bridgeDC-DCconverter,"inProc.IEEEAppl.Power Electron.Conf.,Feb.21–25,2010,pp.1471–1476.

[6]M.BrunoroandJ.L.F.Vieira,"Ahigh-performanceZVSfull-bridgedc-dc0–50-V/0–10-Apowersupplywithphase-shiftcontrol,"IEEETrans. PowerElectron.,vol.14,no.3,pp.495–505,May1999.

[7]Y.Xue,L.Chang,S.B.Kjaer,J.Bordonau,andT.Shimizu, "Topologiesofsingle-phaseinvertersforsmalldistributedpowergenerators:An overview,"IEEETrans.PowerElectron.,vol.19,no.5,pp.1305–1314, Sep.2004.

[8]M.D.Bellar,T.S.Wu,A.Tchamdjou,J.Mahdavi,andM.Ehsani,"A reviewofsoftswitcheddc-acconverters,"IEEETrans.Ind.Appl.,vol.34, no.4,pp.847–860,Jul./Aug.1998.

[9]W.Yu,J.-S.Lai,H.Qian,andC.Hutchens,"High-efficiencyMOSFETinverterwithH6-typeconfigurationforphotovoltaicnonisolatedac-module applications,"IEEETrans.PowerElectron.,vol.26,no.4,pp.1253–1260, Apr.2011.

[10]J.Salmon,J.Ewanchuk,andA.M.Knight,"PWMinvertersusing split-woundcoupledinductors,"IEEETrans.Ind.Appl.,vol.45,no.6, pp.2001–2009,Nov.2009.

[11]D.Garabandic,"Methodandapparatusforreducingswitchinglossesina switchingcircuit,"U.S.Patent6847196,Aug.28,2002.

[12]B.Chen,B.Gu,L.Zhang,J.-S.Lai,andW.Yu,"Ahighefficiencyand reliabilitysingle-phasephotovoltaicmicro-inverterwithhighmagnetics utilizationfornonisolatedac-moduleapplications,"inProc.IEEEEnergy Convers.Congr.Expo.,2013,pp.2406–2411.

[13]D.M.Divan,"TheresonantDClinkconverter-Anewconceptinstatic powerconversion,"IEEETrans.Ind.Appl.,vol.25,no.2,pp. 317–325, Mar./Apr.1989.

[14]D.M.DivanandG.Skibinski,"Zero-switching-lossinvertersforhigh powerapplications,"IEEETrans.Ind.Appl.,vol.25,no.4,pp. 634–643, Jul./Aug.1989.

[15]A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans.ind. App., vol.19, no.5, pp. 518-523, Sept./Oct.1981.

[16]R. Kumar Ahuja1, A. Kumar, "MATLAB Simulation and Analysis of Nine-Level Inverter Using Different Schemes of Sinusoidal PWM" International Journal of Innovative Research in Science Engineering and Technology, pp. 13626-13633, 6 June 2014.

[17]V. Naga haskar Reddy, Ch. Sai. Babu and K. Suresh, "Advanced Modulating Techniques for Diode Clamped," APRN J Eng Appl Sci , vol.6, no.5, pp. 90-99, Jan 2011.

[18]X. Zheng, L. Song, and P. Hongying, "Study of Five-level diodes-clamped Inverter Modulation Technology Based on Three-harmonic Injection Method," EMEIT-2012., pp.1973-1976.

[19]Mahmud Ismaila, Idris Ismail and Nor Zaihar Yahaya, "A Comparative Study of SPWM on A 5-Level H-NPC Inverter" Research Journal of Applied Sciences, Engineering and Technology, pp. 2277-2282,July 30, 2013.