DESIGN AND SIMULATION OF AN IMPROVED PERFOMANCE BY FACTS DEVICE

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ABSTRACT: PI controller with control algorithms are used for load compensation and voltage regulation in D-STATCOM. Because of variation in dc capacitor voltage, load changes might affect the compensation. In this paper, we propose the new method of connecting the external inductor to the system. The main problems in distribution side are load variations, voltage sag, swell, unbalanced in loads, these types of problems are rectified in this paper by our proposed method. This will be proved using this proposed approach with MATLAB simulation results.

Keywords: DC Link Voltage Control, DSTATCOM, PI Controller, Transient Response, VSI.

I. INTRODUCTION

The biggest network in the world is power system and controlling of this network is very big task. The main objective of power system control is to maintain continuous supply of power with an acceptable quality, to all the consumers in the system. The system will be in equilibrium, when there is a balance between the power demand and the power generated. As AC power has two components: Real and Reactive. The system requires two mechanisms to achieve reactive power balance (voltage profile) and real power balance (acceptable frequency values The voltage distortion can be kept within the acceptable range by limiting the harmonics current drawn by the consumers. So, the quality of power needs to be maintained to an acceptable benchmark to minimize the interaction between the supply and the load equipment The reactive power balance (voltage) can be achieved by Automatic Voltage Regulator (AVR). The real power balance (Frequency) can be achieved by Load Frequency Control (LFC).When a load is connected to nearly a stiff source, feeder impedance will be negligible [1]–[4]. Under these circumstances, DSTATCOM cannot provide sufficient voltage regulation at the load terminal.

In This paper proposes a new control algorithm based DSTATCOM topology for voltage regulation even under stiff source. It is achieved by connecting a suitable external inductor in series between the load and the source point. Point of common coupling (PCC) will be the point where external inductor and source are connected. DSTATCOM, connected at the load terminal, provides voltage regulation by indirectly regulating the voltage across the external inductor. Proposed control algorithm to obtain variable reference load voltage is formulated as a function of the desired source current. This voltage indirectly controls the current drawn from the source for a permissible range of source voltage. Therefore, the control algorithm makes source currents balanced, sinusoidal,

and in phase with respective source voltages during normal operation. During voltage disturbances, a constant voltage is maintained at the load terminal. Hence, proposed topology and control algorithm make compensator multifunctional so that it provides fast voltage regulation at load terminal and additionally provides advantages of CCM while operating in VCM.

PROBLEM IDENTIFICATION:

In power system network, a sudden load perturbation in any area causes the deviation of frequencies distortion of power (voltage, current) may occur. If loads are nonlinear loads, it draws non-sinusoidal currents which cause the voltage distortion at the common point of interconnection (CPI). The distorted supply currents at CPI are the source of poor voltage for the other customers at the same CPI. Poor PQ causes a huge loss to the sensitive loads due to the malfunctioning of control equipment and as well as reducing the lifetime of equipment. Even abnormal conditions also power quality disturb makes power system network unbalance. It leads to voltage sag, Voltage swell, Harmonics, voltage flickers *etc* interruptions.

II. DSTATCOM CONFIGURATION

A neutral point clamped voltage source inverter (VSI) topology is chosen as it provides independent control of each leg of the VSI [7]. A single phase equivalent circuit of DSTATCOM in distribution network is shown in Fig. 1.VSI represented by u V dc is connected to load terminal through an LC filter ().

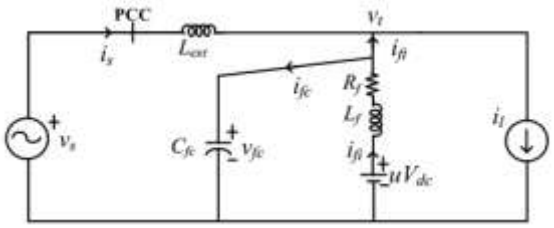


Fig.1.Single phase equivalent circuit of DSTATCOM in distribution network.

The load terminal is connected to the PCC through an external series inductance Lext. Vdc is the voltage maintained across the each dc capacitor and u is a control variable which can be +1 or -1 depending upon switching state. If i, if t, and if c are currents through VSI, DSTATCOM, and Cfc respectively. Vs and Vt are source and load voltages respectively. Loads have both linear and nonlinear elements with balanced or unbalanced features. Load and source currents are represented by I and is respectively.

II. SELECTION OF EXTERNAL INDUCTOR

Under normal operation, external impedance (Zext) does not have much importance, whereas it plays a critical role during voltage disturbances. The value of external impedance is decided by the rating of the DSTATCOM and amount of sag to be mitigated. At any time, the source current in any phase by assuming balanced source voltage is given as

$$\bar{I}_s = \frac{V_s \angle 0 - V_t \angle -\delta}{R_{ext} + jX_{ext}} \qquad (1)$$

Where, Vs, Vt, Rext, Xext, and are rms source voltage, rms load voltage, external resistance, external reactance, and load

angle respectively. For most practical case >>. As a worst case design the reactive source current (Im [Is]) which is supplied by the compensator, will be maximum when is minimum. For this, source will supply only losses in the VSI. Therefore, it will be very small. Hence, Im [Is] is given as

$$I_m[\bar{I}_s] = \frac{V_t - V_s}{X_{ext}} \quad (2)$$

During voltage disturbances, the aim is to protect the sensitive loads with focus is on to improve the DSTATCOM capability to mitigate deep sag. Therefore, keeping it into account, the load voltage during voltage sag is taken as 0.9 pu (per unit) which is sufficient to protect the load. Assuming that the reactive current that a compensator can inject is 20 A and load needs to be protected from sag of 40%, then the value of external reactance is found to be

$$X_{ext} = \frac{0.9-0.6}{20} \times 230 = 3.45\Omega \quad (3)$$

External reactance of 3.45 that corresponds to an inductance of 11 mH for a 50 Hz supply is used.

III. PROPOSED-CONTROL ALGORITHM

Proposed control algorithm aims to provide fast voltage regulation at the load terminal during voltage disturbances while retaining the advantages of CCM during normal operation. Firstly, currents that must be drawn from the source to get advantages of CCM are computed. Using these currents, magnitude of voltages that need to be maintained at load terminal is computed. If this voltage magnitude lies within a permissible range then same voltage is used as reference voltage to provide advantages of CCM. If voltage lies outside the permissible range, it is a sign of voltage disturbance and a fixed voltage magnitude is selected as reference voltage. A two loop controller, whose output is load angle, is used to extract load power and VSI losses from the source. Finally, a discrete model is derived to obtain switching pulses. All these steps are presented in detail in this section.

A. Computation of Reference Voltage Magnitude (Vt*)

During normal operation, load voltage must be regulated in such a way that following advantages provided by CCM operation are achieved:

- Source currents are balanced and sinusoidal.
- Unity power factor (UPF) at PCC.
- Source supply load average power and VSI losses.

To achieve all aforementioned objectives, instantaneous symmetrical component theory [15] is used to get reference source currents. DSTATCOM makes the load voltages balanced and sinusoidal, but still may contain some switching harmonics which will give unacceptable reference source currents when directly used. Therefore, positive sequence component of load voltages (v+ta1, v+tb1, and v+tc1) are extracted and used to compute reference source currents (i*sa, i*sb, and i*sc) as follows:

$$i_{sa}^{*} = \frac{v_{ta}^{+}}{\Delta_1^{+}}\left(P_{lavg} + P_{loss}\right)$$
$$i_{sb}^{*} = \frac{v_{tb}^{+}}{\Delta_1^{+}}\left(P_{lavg} + P_{loss}\right)$$
$$i_{sc}^{*} = \frac{v_{tc1}^{+}}{\Delta_1^{+}}\left(P_{lavg} + P_{loss}\right) \quad (4)$$

Where, $\Delta^{+}_{1}=\sum_{j=a,b,c}(V_{tj1}^{+})^2$

Plavg is average load power and is calculated using a moving average filter (MAF). Total losses in the inverter, Ploss, computed using a PI controller, helps in maintaining averaged dc link voltage (Vdc1 + Vdc2) at a predefined reference value (2Vdcref) by drawing a set of balanced currents from the source and is given as follows:

$$P_{loss} = K_{pdc}\, e + K_{idc} \int e\, dt \qquad (5)$$

Where, Kpdc, Kidc, and e = 2Vdcref- (Vdc1 + Vdc2) are proportional gain, integral gain, and voltage error of the PI controller respectively. The reference currents to be drawn from the source are computed using (4), reference voltages at the load terminal can be derived. Applying KVL in the circuit shown in Fig. 1

$$\bar{V} = \bar{I}_s Z_{ext} + \bar{V}_t \qquad (6)$$

Source voltage and source current will be in phase for the UPF operation. Also, source voltage is taken as reference.

Therefore $V_s = I_s(R_{ext} + j\,X_{ext}) + V_t \angle -\delta$.
From the above equation, the load voltage can be computed as follows:

$$V_t = \sqrt{(V_s - I_s R_{ext})^2 + (I_s X_{ext})^2} \qquad (7)$$

Based on standards, load voltage has a permissible range of variations between 0.9 to 1.1 Pu. Therefore, as long as Vt, obtained using (7) lies between 0.9 to 1.1 Pu, is used as reference load voltage (V*t) and the advantages of CCM operation are achieved. Here, Vt is indirectly controlled by the desired source current. During sag and swell, the load voltage magnitude will be between 0.9 to 0.1 Pu and 1.1 to 1.8 Pu respectively for half cycle to 1 minute [16]. Therefore, reference load voltage magnitudes are set to 0.9 Pu and 1.1 Pu during sag and swell respectively. The reason to keep load voltages at these values is to maximize the DSTATCOM disturbance withstanding ability while keeping load voltage at the safe limits for satisfactory operation. Therefore, following conclusions can be drawn:

$$\begin{aligned} &If\ 0.9\,pu \le V_t \le 1.1\,pu\ \text{then}\ V_t^* = V_t \\ &\text{Else}\quad \text{If}\ V_t > 1.10\,pu\ \text{then}\ V_t^* = 1.1\,pu \\ &\quad \text{else if}\ V_t < 0.9\,pu\ \text{then}\ V_t^* = 0.9\,pu \end{aligned} \qquad (8)$$

B. Computation of Load Angle ()

The block diagram of controller to compute load angle is shown in Fig. 2. It ensures that the load average power and losses in the VSI are supplied by the source [7]. Alternately, Ploss responsible for maintaining dc link voltage must be equal to shunt link power Psh. Comparing Ploss and Psh, an error is generated which is passed through a PI controller to compute as follows:

$$\delta = K_{pa}(P_{loss} - P_{sh}) + K_{ia} \int (P_{loss} - P_{sh})\, dt \qquad (9)$$

Where, and Kia are proportional and integral gains of the inner PI controller respectively. The value of shunt link power, Psh, is computed using a MAF as follows:

$$P_{sh} = \frac{1}{T}\int_{t_1}^{t_1+T} (V_{ta}\, i_{fta} + v_{tb}\, i_{ftb} + v_{tcc}\, i_{ftc})\, dt \qquad (10)$$

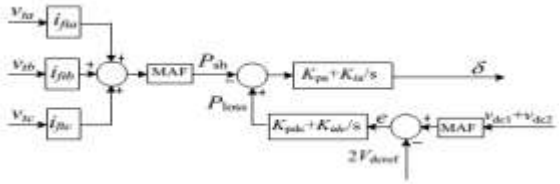


Fig.2. Controller to calculate and P loss.

A positive value of Psh means power flow from DSTATCOM to load terminal, whereas negative value of Psh represents power flow from load terminal to DSTATCOM. In steady state, VSI losses are compensated by taking power from the source. Hence, Psh will be negative in steady state. Moreover, capacitor voltage decreases from its reference voltage in steady state. Deviation of capacitor voltage from reference voltage represents losses in the VSI. Hence, Ploss will be negative during steady state. Therefore, at all time, Psh and Ploss should be equal. Hence, difference of Psh and Ploss should be minimized. Output of inner PI controller, shown in Fig. 2, is delta which ensures that shunt link power Psh drawn from source equals to losses in the capacitor Ploss. **C.**

Generation of Instantaneous Reference Voltage

By knowing the zero crossing of phase-a source voltage, selecting suitable reference load voltage magnitude from (8) and computing load angle from (9) the three phase reference voltages are given as follows:

$$v_{trefa} = \sqrt{2}V_t^* \sin(wt - \delta)$$
$$v_{trefb} = \sqrt{2}V_t^* \sin(wt - \frac{2\pi}{3} - \delta)$$
$$v_{trefc} = \sqrt{2}V_t^* \sin(wt + \frac{2\pi}{3} - \delta) \quad (11)$$

Where, is the frequency

C. Generation of Switching Pulses

Each phase of the VSI can be controlled independently and hence, a discrete model of single phase has been derived to generate switching pulses. Dynamics of filter inductor and capacitor can be presented by following equations:

$$\frac{dv_{fc}}{dt} = \frac{1}{c_{fc}} i_{fi} - \frac{1}{c_{fc}} i_{ft} \quad (12)$$
$$\frac{di_{fi}}{dt} = -\frac{1}{l_f} v_{fc} - \frac{R_f}{l_{fi}} + \frac{V_{dc}}{l_f} u. \quad (13)$$

Matrix representation of (12) is given as follows:

$$\dot{x} = Ax + Bz \quad (13)$$

where

$$A = \begin{bmatrix} 0 & \frac{1}{c_{fc}} \\ -\frac{1}{l_f} & -\frac{R_f}{l_{fi}} \end{bmatrix},$$
$$B = \begin{bmatrix} 0 & -\frac{1}{c_{fc}} \\ \frac{V_{dc}}{l_f} & 0 \end{bmatrix}$$
$$x = [v_{fc}\, i_{fi}].^t, \quad z = [u \;\; i_{fi}]^t.$$

Where,(13), given in continuous form, can be represented in discrete time form as follows:

$$x(k+1) = Gx(k) + H\, z(k) \quad (14)$$

Where, matrix G and H are given as

$$G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix},$$
$$H = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}$$

From (14) capacitor voltage will be

$$v_{fc}(k+1) = G_{11} v_{fc}(k) + G_{12} i_{fi}(k) + H_{11} u_k + H_{12} i_{ft}(k) \quad (15)$$

The reference voltage, Vt ref, is maintained at the load terminal. A cost function, J, is chosen as

$$J = [v_{tref}(k+1) - v_{fc}(k+1)]^2 \quad (16)$$

Cost function is

$$v_{fc}(k+1) = v_{tref}(k+1) \quad (17)$$

Finally, reference discrete voltage control law from (15) and (17) is given as

$$u^*(k) = \left[v_{tref}(k+1) - G_{11} v_{fc}(k) - G_{12} i_{fi}(k) - H_{12} i_{ft}(k) \right] / H_{11} \quad (18)$$

U*(k) is regulated around a hysteresis band h to generate switching pulses of VSI using hysteresis control.

IV. MATLAB/SIMULINK RESULTS

Here simulation is carried out in several cases, in that 1) Proposed DSTATCOM Topology for PQ Improvement Features. **Proposed DSTATCOM Topology for PQ Improvement Features by using PI controller**

Proposed Novel Multifunctional Distributed Compensation Scheme can mitigate several power quality (PQ) problems. In current control mode (CCM), it injects harmonic and reactive components of load currents to make source currents balanced, sinusoidal, and in phase with load voltages. In voltage control mode (VCM), it regulates load voltage at a constant value to protect sensitive loads from voltage disturbances such as sags, swells, transients, and/or fluctuations. However, the objectives of these two modes are different and it can be Achieve by proposed DSTATCOM.

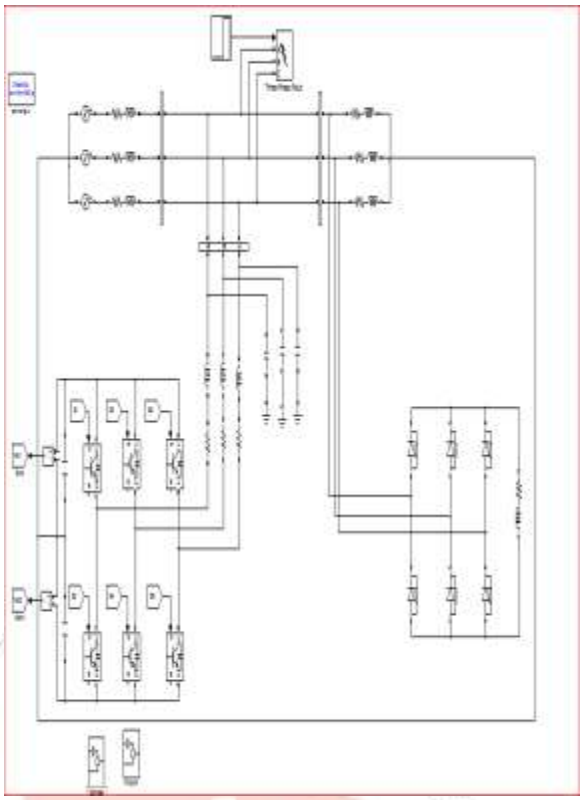
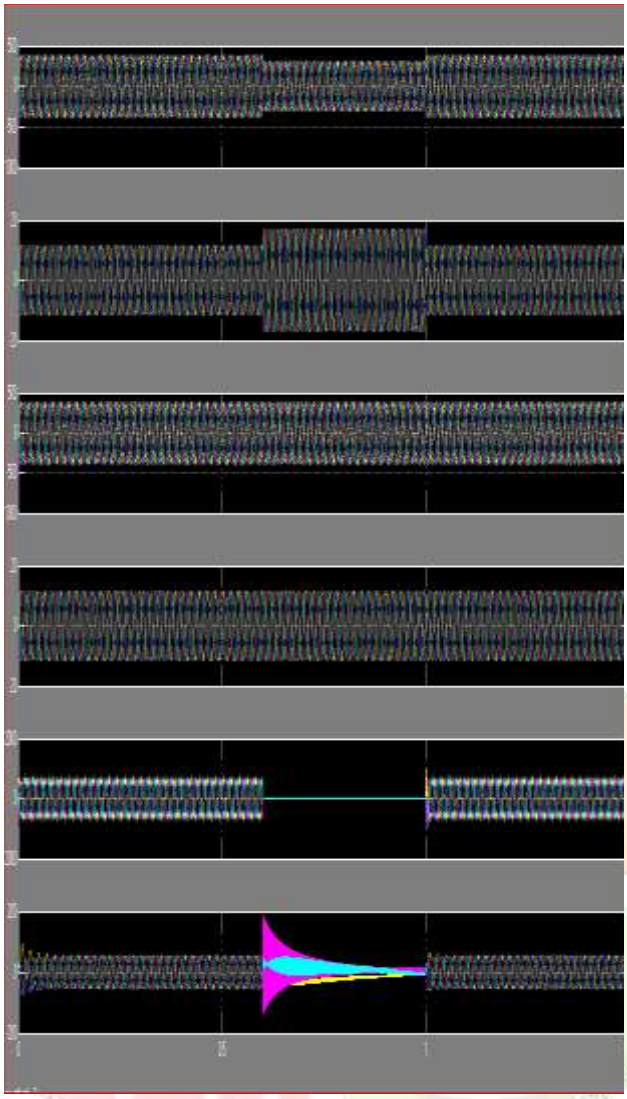


Fig.4. MATLAB/Simulink Model of Proposed DSTATCOM Topology for PQ Improvement Features.

Fig.4 gives the Simulation model of system with M-DSTATCOM. In a distribution system with a non-linear load connected to the system will generates harmonics. A nonlinear load in a power system is characterized by the introduction of a switching action and consequently current interruptions. This behavior provides current with different components that are multiples of the fundamental frequency of the system. These components are called harmonics. The amplitude and phase angle of a harmonic is dependent on the circuit and on the load it drives.



Waveform 1 shows the sag representation
2 shows swell
3 compensated load voltage
4 compensated current

VI. CONCLUSION:

D STATCOM based PI controller to the dc link has been proposed in this paper. System performance can be improves by discussed PI control strategy, varies the gain of the PI controller during the transient period. The system has been modeled and simulated in the MATLAB. The performance of the dc link and compensation were observed with and without PI controller. Simulation results show a 50% reduction in voltage deviation of the dc link voltage with faster settling time. Instantaneous symmetrical component theory has been used for load compensation. Good compensation has been observed as in fault conditions even in voltage sag and swells. Through simulation studies, the implementation of PI controller for DC link voltage control in a DSTATCOM using instantaneous symmetrical component theory for load were observed.

VII. REFERENCES

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