Implementation of Efficient Binary Adder using Quantum-Dot Cellular Automata

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Abstract : *Quantum-dot cell automata (QCA) are an alluring rising innovation appropriate for the improvement of ultra-thick low-power elite advanced circuits. Effective arrangements have been proposed for a few number juggling circuits, for example, adders, multipliers, and comparators. By and by, since the plan of advanced circuits in QCA still represents a few difficulties, novel usage procedures and systems are very alluring. As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. In this brief, we propose a new adder that outperforms all state-of-the-art competitors and achieves the best area-delay trade off. The above advantages are obtained by using an overall area similar to the cheaper designs known in literature. The 16-bit, 32-bit and 64-bit version of the novel adder is implemented by verilog.*

Index Terms - QCA, Adder, Majority gate.

I. INTRODUCTION

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or one's complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subractor. Other signed number representations require a more complex adder.

In this brief, an innovative technique is presented to implement high-speed low-area adders in QCA. Carry look ahead adder(CLA) and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG).

In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections. An adder designed as proposed runs in the RCA fashion, but it exhibits a computational delay lower than all state-of the- art competitors and achieves the lowest area-delay product (ADP).

In this short, a creative procedure is displayed to execute rapid low-region adders in QCA. Carry look ahead adder(CLA) and parallel-prefix adders are here misused for the acknowledgment of a novel 2-bit expansion cut. The last enables the bring to be engendered through two resulting bit-positions with the deferral of only one dominant part door (MG).

The organization of the paper as follows:

The related works of research are discussed in section II. Section III deals with the methodology of QCA. Results and discussions are explained in step by step manner in the section IV. Finally, the summary and conclusions were incorporated in section V

II. RELATED WORK

The essential component of a nanostructure in light of QCA is a square cell with four quantum dabs and two free electrons. The last can burrow through the specks inside the cell, be that as it may, inferable from Columbic aversion, they will dependably live in inverse corners, in this way prompting just two conceivable stable states, likewise named polarizations. Areas of the electrons in the cell are related with the paired states 1 and 0. Contiguous cells collaborate through electrostatic strengths and have a tendency to adjust their polarizations. Be that as it may, QCA cells don't have inherent information stream directionality. In this manner, to accomplish controllable information bearings, the phones inside a QCA configuration are divided into the purported clock zones that are continuously connected with four clock flags, each stage moved by 90◦. This clock conspire, named the zone timing plan, makes the QCA outlines inherently pipelined, since each clock zone carries on like a D-lock.

Quasi-adiabatically switched quantum-dot cellular automata (QCA) devices present the opportunity to extend our effort from the implementation of combinational logic devices to more useful sequential logic devices. One very important application of sequential logic is in the recognition of patterns in serial bit streams. This is important, for example, in Internet applications, where particular bit patterns are designated as “sentinel” characters that indicate a particular action should be taken. The foundation of a

serial bit-stream analyzer is a shift register, which can be implemented very easily using quasi-adiabatically switched QCA devices. In addition to the shift register, the device will require a multiple-bit comparator, which has not yet been demonstrated in QCA architecture. We will present a multiple-bit serial stream analyzer that combines the functions of the shift register and the comparator.

The basic Boolean primitive in quantum cellular automata (QCA) is the majority gate. In this paper, a method for reducing the number of majority gates required for computing three-variable Boolean functions is developed to facilitate the conversion of sum-of-products expression into QCA majority logic. Thirteen standard functions are introduced to represent all three variable Boolean functions and the simplified majority expressions corresponding to these standard functions are presented. We describe a novel method for using these standard functions to convert the sum-of-products expression to majority logic. By applying this method, the hardware requirements for a QCA design can be reduced. As an example, a 1-bit QCA adder is constructed with only three majority gates and two inverters.

A quantum-dot cellular automaton (QCA) is an emerging nanotechnology for electronic circuits. Its advantages such as faster speed, smaller size, and lower power consumption are very attractive. The fundamental device, a quantum-dot cell, can be used to make gates, wires, and memories. As such it is the basic building block of nanotechnology circuits. While the physical nature of the nano scale materials is complicated, the circuit designer can concentrate on the logical and structural design, so the design effort is reduced. Because of its novelty, the current literature shows only simple circuit structures. So this paper broadens the QCA circuit designs with larger circuits and shows analyses based on those designs. This paper proposes three kinds of adder designs in QCA.

A quantum-dot cellular automaton (QCA) is a rising nanotechnology, with the potential for speedier speed, littler size, and lower control utilization than transistor-based innovation. Quantum-spot cell automata have a basic cell as the essential component. The cell is utilized as a building square to develop doors and wires. Before hand, snake plans in light of regular outlines were analyzed for execution with QCA innovation. That works showed that the outline exchange offs are altogether different in QCA. This paper uses the novel QCA qualities to plan a convey stream viper that is quick and effective. Recreations show exceptionally alluring execution (i.e., intricacy, region, and postponement). This paper likewise investigates the plan of serial parallel multipliers. A serial parallel multiplier is planned and reenacted with a few diverse operand sizes.

III. METHODOLOGY

The circuits were designed to implement in QCA the novel equations demonstrated in the previous Section. To introduce the novel architecture proposed for implementing ripple adders in QCA, let us consider two n-bit addends A = $a_{n-1}, \ldots, a_0$ and B = $b_{n-1}, \ldots, b_0$ and suppose that for the i^{th} bit position (with i = n − 1, . . . , 0) the auxiliary propagate and generate signals, namely $p_i = a_i + b_i$ and $g_i = a_i \cdot b_i$, are computed. ci being the carry produced at the generic (i−1) th bit position, the carry signal c_i+2, furnished at the (i+1)th bit position, can be computed using the conventional Carry look ahead adder(CLA) logic reported

$$C_{i+2} = g_{i+1} + p_{i+1} \cdot g_i + p_{i+1} \cdot p_i \cdot c_i$$

The latter can be rewritten as given in c_{i+2} = M (M (a_{i+1}, b_{i+1}, g_i) M (a_{i+1}, b_{i+1}, p_i) c_i). In this way, the Ripple Carry Adder(RCA) action, needed to propagate the carry c_i through the two subsequent bit positions, requires only one Majority Gate(MG). Conversely, conventional circuits operating in the Ripple Carry Adder fashion, namely the RCA and the Carry Forward Adder (CFA), require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

The proposed n-bit adder is then implemented by cascading n/2 2-bit modules as shown in Sum Chain. Having assumed that the carry-in of the adder is c_{in} = 0, the signal p_0 is not required and the 2-bit module used at the least significant bit position is simplified. The sum bits are finally computed as shown in Carry Chain.

Sum Chain:

The figure 1 shows the sum chain of an adder where the non inverted carry output is connected to next stage and inverted carry output is connected to next level logic.

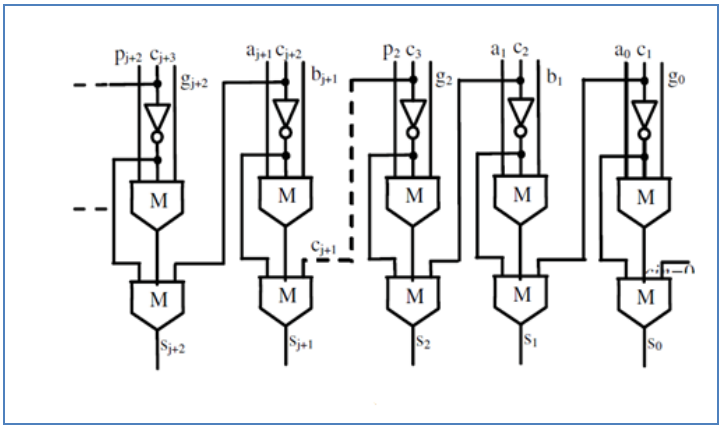

Figure 1: Sum chain of an adder

Carry Chain:

The figure 2 shows the carry chain.

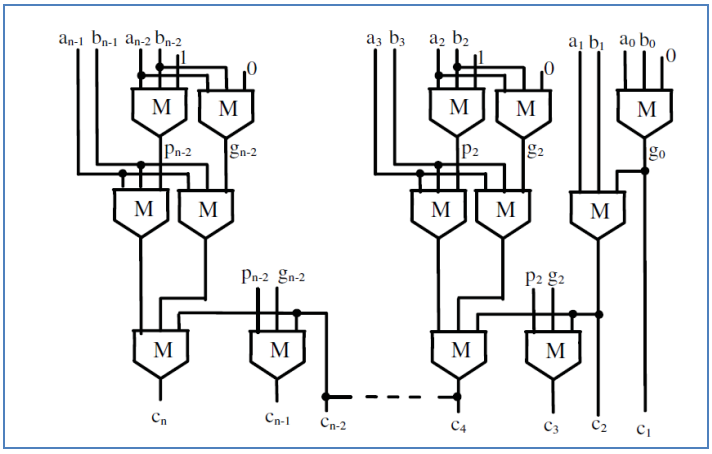

Figure 2: Carry chain

IV. RESULTS

Figure 3 shows the simulation results of 16 bit adder using QCA.

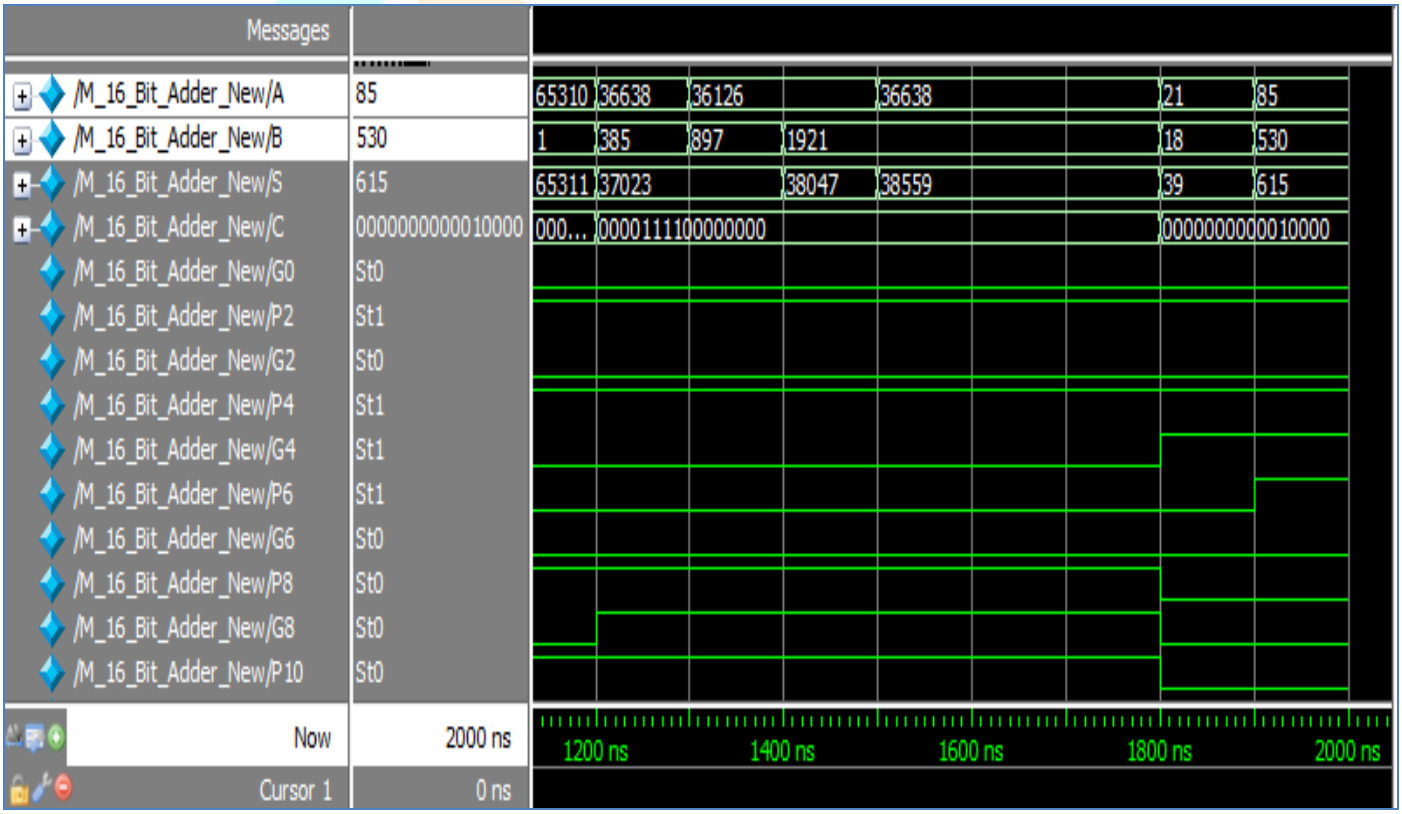

Figure 3: simulation results of 16 bit adder

RTL Schematic:

Figure 4 shows the RTL schematic of 16 bit adder. In which there are 16 inputs with the variables A and B. Adder performs the addition of two binary digits and produces the output as sum and carry.

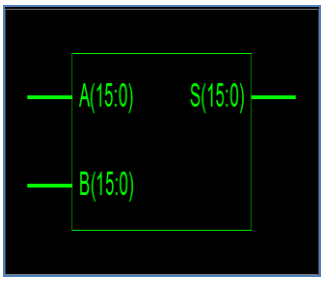

Figure 4: RTL of a 16 bit adder.

Figure 5 shows the device utilization summary of a 16 bit adder.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	30	7,168	1%	
Logic Distribution				
Number of occupied Slices	21	3,584	1%	
Number of Slices containing only related logic	21	21	100%	
Number of Slices containing unrelated logic	0	21	0%	
Total Number of 4 input LUTs	30	7,168	1%	
Number of bonded IOBs	48	141	34%	
Total equivalent gate count for design	183			
Additional JTAG gate count for IOBs	2,304			

Figure 5: Device utilization summary of 16 bit adder.

The total number of 4 input look up tables is 30.the total equivalent gate count for design is 183.

V. CONCLUSION

A new adder designed in QCA was presented. It achieved Area & speed performances higher than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited.

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