An Advanced vector controlled Induction Motor ASD System

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Abstract: This paper proposes a novel four-quadrant vector controlled induction motor (IM) adjustable speed drive (ASD) framework in light of an as of late proposed matrix converter topology called quasi-Z-source direct matrix converter (QZSDMC). The QZSDMC is shaped by falling the quasi-Z-source impedance arrange and the ordinary direct matrix converter (DMC). The QZSDMC can give buck-support operation voltage exchange proportion controlled by controlling the shoot-through obligation proportion and bidirectional operation capacity. The control system, which depends on the indirect field arranged control calculation, can control the motor speed from zero to the appraised an incentive under full load condition amid motoring and recovering operation modes. The proposed four-quadrant vector controlled IM-ASD framework in view of the QZSDMC topology defeats the voltage pick up restriction of the customary DMC and accomplishes buck and lift condition in four-quadrant modes with diminished number of switches, in this manner accomplishing minimal effort, high productivity, and unwavering quality, contrasted with back-with back converter.

Record Terms—Direct matrix converter (DMC), indirect field situated control (IFOC), induction motor (IM), quasi-Z-source converter (QZSC), quasi-Z-source DMC (QZSDMC), Z-source converter (ZSC).

I.INTRODUCTION

The utilization of variable speed motor drives is a developing pattern in modern and car applications, ensuring high effectiveness, expanded vitality sparing, and higher adaptability and adaptability [1]. The consecutive converter, which is shaped by entwining two VSI spans at their mutual dc-interface, is generally connected in many motor drive applications. One of the converters works in the correcting mode, while the other converter works in the upsetting mode. The dc-interface voltage must be higher than the pinnacle line-to-line voltage to accomplish full control of the motor torque [2], [3].

The source-side inductors are likewise a weight to the framework; their size is ordinarily 20%– 40% of the framework size while working at an exchanging recurrence of a few kilohertzs. Moreover, the consecutive topology is delicate toward electromagnetic impedance and different sources of clamors that can unintentionally turn ON two changes from a similar stage leg, causing a short out blame thusly. In this manner, the downsides of customary consecutive converters are high cost, substantial size, overwhelming weight, moderately high vitality misfortunes, and affectability toward electromagnetic obstruction [3].

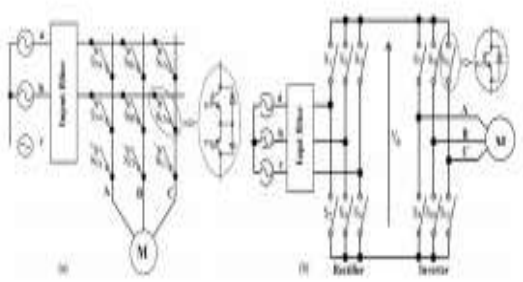

Fig.1. (a) DMC and (b) IMC topology

The matrix converter is an appealing other option to the consecutive converter since it can change over an air conditioner voltage directly into an air conditioner yield voltage of variable sufficiency and recurrence without the requirement for a middle of the road dc-connection and capacitor. Moreover, it gives bidirectional power stream, sinusoidal information/yield ebbs and flows, controllable information control factor, and has minimized plan. The volume investment funds of a matrix converter contrasted with a back-with back converter has been assessed to be a factor of three [3]. The expansive dc-interface capacitor and vast info inductors of the consecutive converter are supplanted by little information channel with capacitors and inductors in the matrix converter. Besides, as a result of a high joining capacity and higher unwavering quality of the semiconductor gadgets, the matrix converter topology is a superior answer for outrageous temperatures and basic volume/weight applications [5].

Matrix converters can be isolated into two classes: the DMC and IMC, as appeared in Fig. 1. The DMC plays out the voltage and current transformation in one phase (direct) control change while the IMC highlights a two-organize (indirect) control conversion. The DMC and IMC circuit topologies are equivalent in their basic functionality. The difference in the categories results from a difference in loading of the semiconductors and a different commutation scheme. The IMC has a simpler commutation due to its two-stage structure, however, this is achieved at the expense of more series connected power devices in the current path, which results in a higher semiconductor losses and typically a lower achievable efficiency compared with the DMC. However, the differences between the control performances of DMC and IMC are quite negligible in practice. Therefore, the DMC will be investigated within this paper as a candidate topology to achieve highest conversion efficiency [6].

Improving the voltage transfer ratio is an important research topic. One easy solution is to connect a transformer between the power supply and the MC. However, the mains frequency transformer is bulky, expensive, and affects the system efficiency. Other solution is to use a MRFC, which consists of a MC and a ac chopper, and has a voltage transfer ratio greater than one. The MRFC converter is categorized into two groups: the integrated and cascade MRFCs, as shown

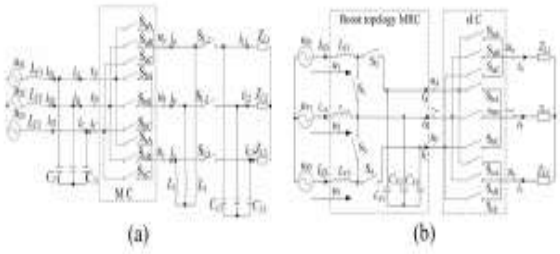

Fig.2. (a) IMRFC and (b) CMRFC topologies.

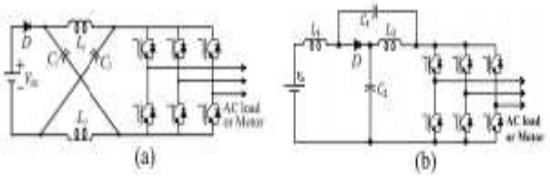

Fig. 3. (a) Basic ZSC and (b) QZSC structures

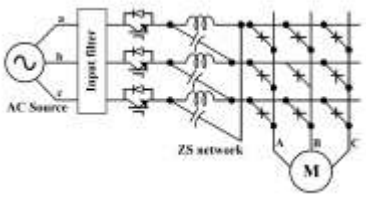

Fig. 4. Voltage fed ZSDMC topology

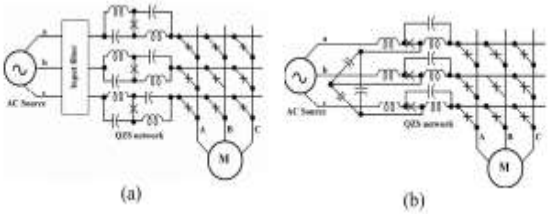

Fig. 5. Voltage fed QZSDMC topologies with (a) discontinuous and (b) continuous input current.

Z-source network allows the short circuit, which makes the ZSDMC commutation easier. The ZSDMC is derived from the traditional DMC by only adding three inductors, capacitors, switches, and diodes. However, the ZSDMC has a limited voltage boost ratio (voltage gain can only reach 1.15), inherited phase shift caused by the Z-network, which makes the control inaccurate, and also discontinuous current in the front of Z-source network. However, for the QZSDMC, as shown in Fig. 5, the voltage gain can go to four to five times or even higher depending on the voltage rating of the switches, no phase shift, which can cause less error in the control, and lower switch voltage and current stress [14]. In addition, the circuit in Fig. 5(b) has continuous input current [15]

In this paper, the application of the QZSDMC topology for four-quadrant IM-ASD system is proposed. The QZSDMC can produce the desired ac output voltage, even greater than the input line voltage due to its boost voltage capability. The four-quadrant speed control is implemented using the IFOC during motoring and regenerating operation modes. The system's configuration, equivalent circuit, analysis, and control are presented in detail. Simulation and dSPACE realtime implementation results demonstrate the high performance of the proposed four-quadrants QZSDMC-IM-based ASD system

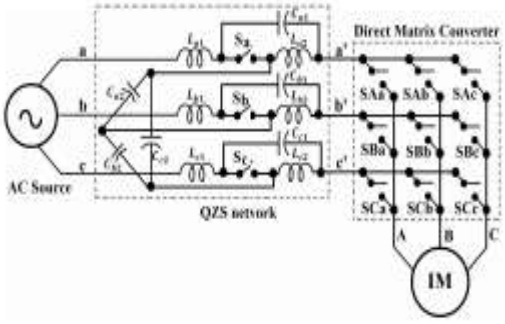

Fig. 6. QZSDMC-based IM-ASD system.

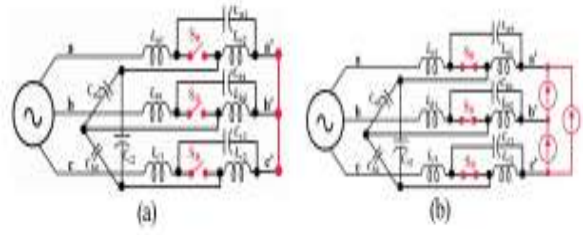

Fig. 7. Equivalent circuit of the QZSDMC. (a) ST state. (b) NST state.

II. QZSDMC-BASED ASD

A. Topology

The main circuit configuration of the proposed QZSDMC based four-quadrant IM-ASD system is shown in Fig. 6. It consists of four parts, namely, input filter, QZS-network, DMC, and IM. The QZS-network includes six inductors $(L_{a1}, L_{a2}, L_{b1}, L_{b2}, L_{c1}, L_{c2})$ the capacitors $(C_{a1}, C_{a2}, C_{b1}, C_{b2}, C_{c1}, C_{c2})$, and three additional bidirectional switches (S_a, S_b, S_c). One gate signal can be used to control these three switches because they have the same switching state. Therefore, the drive signal for $S_a, S_b,$ and S_c can be denoted as S_0.

B. Operation and Modeling

The operation principle of the QZSDMC can be divided into two switching states: ST and NST states. Fig. 7 shows the QZSDMC equivalent circuits during these states. During the ST state, Fig. 7(a), switch S0 is off and the output of the QZSDMC is shorted for boost operation. While, during the NST state, Fig. 7(b), switch S0 is on for normal DMC operation. Due to the symmetry of the system, inductors of QZS-network $(L_{a1}, L_{a2}, L_{b1}, L_{b2}, L_{c1}, L_{c2})$ have the same inductance (L), and the capacitors $(C_{a1}, C_{a2}, C_{b1}, C_{b2}, C_{c1}, C_{c2})$ also have the same capacitance (C) For one switching cycle, Ts, the time interval of the ST state is T , and the time interval of the NST state is T1, hence, Ts = T + T1, and the ST duty ratio is D = T/Ts. From Fig. 7(a), during the ST state, one can get the following

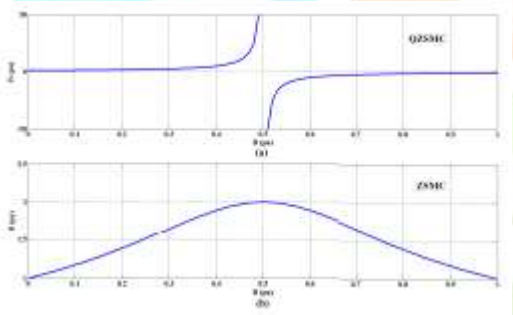

Fig. 8. Boost factor of the ZSDMC and QZSDMC versus D.

voltage equations:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{La1} \\ v_{Lb1} \\ v_{Lc1} \end{bmatrix} + \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} - \begin{bmatrix} v_{Cb1} \\ v_{Cc1} \\ v_{Ca1} \end{bmatrix} - \begin{bmatrix} v_{Lb1} \\ v_{Lc1} \\ v_{La1} \end{bmatrix} \quad (1)$$

where v denotes the voltage, and the subscript Cx1 and Cx2 are the capacitors 1 and 2 of phase-x; Lx1 and Lx2 for the inductors 1 and 2 of phase-x; x = a, b, c. During the NST state, its equivalent circuit is shown in Fig. 7(b), and one can get

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{La1} \\ v_{Lb1} \\ v_{Lc1} \end{bmatrix} + \begin{bmatrix} v_{Ca1} \\ v_{Cb1} \\ v_{Cc1} \end{bmatrix} + \begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} - \begin{bmatrix} v_{Cb1} \\ v_{Cc1} \\ v_{Ca1} \end{bmatrix} - \begin{bmatrix} v_{Lb1} \\ v_{Lc1} \\ v_{La1} \end{bmatrix}. \quad (2)$$

In steady state, the average voltage of the inductors over one switching cycle should be zero, and owing to the symmetric voltages of three-phase capacitors, one gets [12]

$$\begin{bmatrix} v_{a'b'} \\ v_{b'c'} \\ v_{c'a'} \end{bmatrix} = \frac{1}{1-2D} \begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix}. \quad (3)$$

Define B as the boost factor and it is expressed as [12]

$$B_{\text{QZSDMC}} = \frac{v_o}{v_i} = \frac{1}{1-2D} \quad (4)$$

where vi is the amplitude of input voltage source and vo is the output voltage amplitude of the QZS-network. However, the boost factor for the ZSDMC is given by [12]

$$B_{\text{ZSDMC}} = \frac{v_o}{v_i} = \frac{1}{\sqrt{3D^2 - 3D + 1}}. \quad (5)$$

Fig. 8 shows the boost factor for both converter topologies. Thus, the voltage gain G of the QZS-network in the one switching cycle, is given by

$$G = \text{BM}. \quad (6)$$

C. ST Boost Control Method The principle of applying ST state for the QZSDMC is to replace some of the zero state by ST state, to not affect the output voltage. Using the carrier-based PWM, the zero output voltage state in MC is corresponding to the switching state that all three output phases are connected to the same input phase. It happens when all three phase output voltages are either higher or lower than the carrier signal. Therefore,

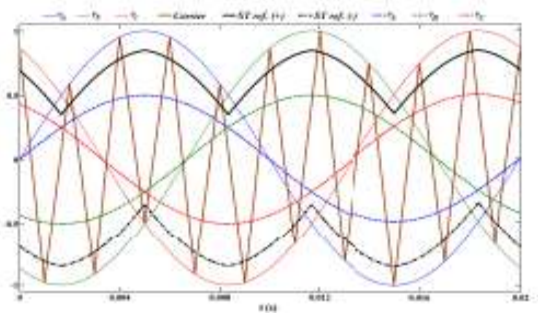

Fig. 9. Simple boost PWM control for the QZSDMC.

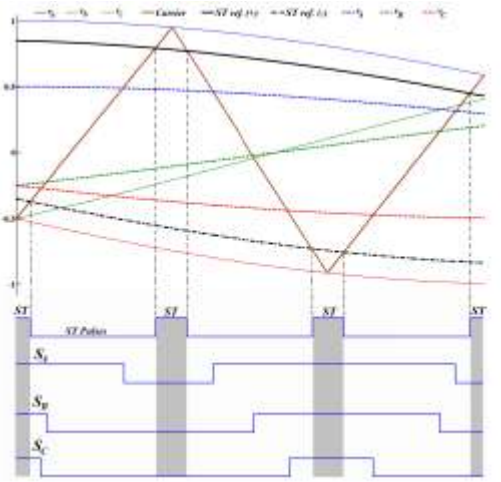

Fig. 10. QZSDMC switching states generation.

the ST reference ought to be either higher than the most extreme reference voltage or lower than the base reference voltage [14]. All the lift control techniques that have been investigated for the customary ZSC, for example, straightforward lift, most extreme lift, greatest consistent lift, and altered space vector balance [21], can be connected to the QZSDMC with an adjustment of the transporter envelope. Fig. 9 demonstrates a basic lift PWM control technique for the QZSDMC. The transporter waveform has a similar envelope with the three-stage source voltages, va, vb, and vc. The best envelope comprises of the most extreme voltage among the three information stage voltages, and the base envelope comprises of the base voltage among them. Amid each exchanging period, the adjusted bearer flag is contrasted and the yield voltage references vA, vB, and vC to create their PWM exchanging groupings (SA, SB, SC).

The ST beats are produced by contrasting the ST references and the changed transporter waveform, as appeared in Fig. 10. The PWM switching sequences SA, SB, and SC should be distributed to nine ac switches to generate the expected PWM pulses. For this purpose, six additional logical signals are used, as shown in Fig. 11, where Sx1, Sy1, and Sz1 denote the indicators for their respective phase-a, -b, and -c of the top voltage envelope. Sx2, Sy2, and Sz2 denote the indicators for their respective phase-a, -b, and -c of the bottom voltage envelope. These six voltage envelope indicators are combined with the three PWM switching sequences to generate nine switching signals.

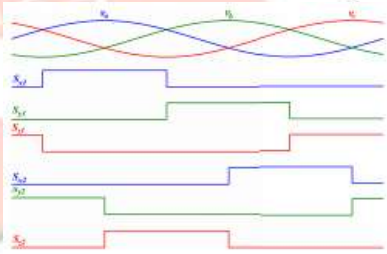

Fig. 11. Voltage envelopes indicators.

According to the following logics:

$$\begin{aligned}
S_{Aa} &= S_{x1}S_A + S_{x2}\bar{S}_A \\
S_{Ab} &= S_{y1}S_A + S_{y2}\bar{S}_A \\
S_{Ac} &= S_{z1}S_A + S_{z2}\bar{S}_A \\
S_{Ba} &= S_{x1}S_B + S_{x2}\bar{S}_B \\
S_{Bb} &= S_{y1}S_B + S_{y2}\bar{S}_B \\
S_{Bc} &= S_{z1}S_B + S_{z2}\bar{S}_B \\
S_{Ca} &= S_{x1}S_C + S_{x2}\bar{S}_C \\
S_{Cb} &= S_{y1}S_C + S_{y2}\bar{S}_C \\
S_{Cc} &= S_{z1}S_C + S_{z2}\bar{S}_C.
\end{aligned} \quad (7)$$

The above logical functions can be used to drive the QZSDMC after inserting the ST states. A simple boost control is achieved through two ST

references, in which both references are related to both envelopes by [12]

$$v_{st,r} = \frac{(y_{max} - y_{min})n + y_{max} + y_{min}}{2} \quad (8)$$

where n will determine the ST duty ratio, and its value has a limitation that the resultant minimum value of the top ST reference should be less than 0.5 p.u. and larger than M. Therefore $1 \geq n \geq (1+4M)/3$ for the top ST reference, and its negative value is (−n) for the bottom ST reference. The modulation index should be less than 0.5, given that the output references v_A, v_B, and v_C can be any frequency with any phase angle and with no harmonic injection. y_{max} and y_{min} are the top and bottom envelopes of the source voltages, respectively. For the simple boost control, the ST interval from the top reference can be calculated as [12]

$$T_0 = \frac{1-n}{2} T_c \quad (9)$$

where T0 and Tc are the ST duration per switching cycle and switching time, respectively, and its ST duty ratio in half carrier cycle is [12]

$$D_h = \frac{1-n}{2}. \quad (10)$$

Fig. 12 shows the complete process to generate the switching signals for the QZSDMC. First, the triangle carrier signal is modulated by the input reference signals v_a, v_b, and v_c to generate the modified carrier signal, which is bounded by the maximum and minimum envelopes of the input reference signals. Second, the ST references are generated from the input

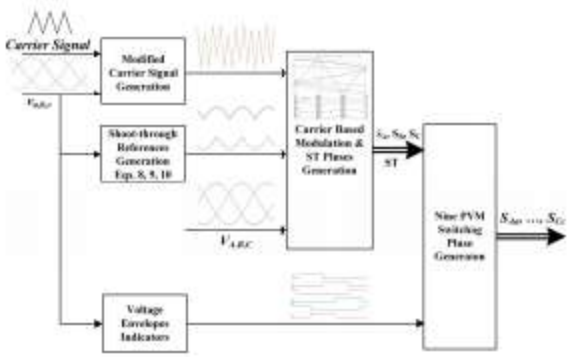

Fig. 12. Block diagram of QZSDMC PWM generation with ST insertion

reference signals and the desired boost ratio using (8)–(10). Then, the switching sequences SA, SB, SC, and ST pulses are generated by comparing the output voltage references vA, vB, and vC and the ST references with the modified carrier signal. Furthermore, voltage envelopes indicators are generated from the input reference signals va, vb, and vc. For example, Sx1 = 1 when phase-a voltage is the largest value among the three phase voltages and Sx2 = 1 when phase-a has the minimum voltage among the three-phase voltages. Finally, these six voltage envelope indicators are combined with the three PWM switching sequences, SA, SB, SC, and the ST pulses to generate nine switching signals.

Existing Method Results

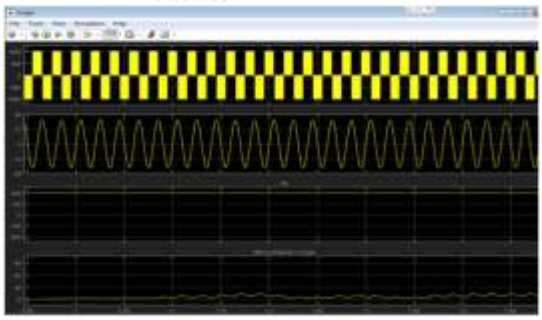

Fig.13.With improved Voltage transfer ratio in DMC with Quasi Z source Inverter (1000 V)

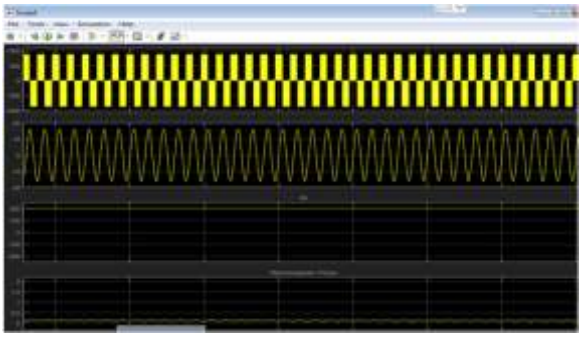

Fig.14.With poor input output voltage ratio in DMC without Quasi z source inverter (866 V)

III. IFOC TECHNIQUE

Vector control is a method, which permits the IM to act like a different energized dc machine with decoupled control of torque and transition, making it conceivable to work the IM as a superior four-quadrant servo drive. The thought behind vector control is that the stator current of the IM is deteriorated into orthogonal parts as a magnetization segment (transition creating) and a torque segment. These parts are controlled separately. To acquire high unique execution of the IM, the magnetizing current segment is kept up at its evaluated level while the torque ought to be controlled through the torque segment of the stator current. The field orientation can be generally classified into stator flux, air-gap flux, and rotor flux orientations. Since the rotor flux orientations are extensively used in ac drives, this scheme is used in this paper [17]. The rotor flux orientation is achieved by aligning the d-axis of the synchronous reference frame with the rotor flux $\lambda^{-}r$ vector. The resultant d- and q-axis rotor flux components are given as

$$\lambda_{qr} = 0 \quad \lambda_{qr} = 0$$
$$\lambda_{dr} = \lambda_r. \quad \lambda_{dr} = \lambda_r. \qquad (11)$$

The d-axis current i_{ds} is referred to as flux-producing current while the q-axis current i_{qs} is the torque-producing current. In the field-oriented control ids, is normally kept at its rated value while i_{qs} is controlled independently. These steady-state d_q-components of the current are given as

$$i_{ds}^* = \frac{\lambda_r^*}{L_m}$$
$$i_{qs}^* = \frac{2}{3}\frac{2}{p}\frac{L_r}{L_m}\frac{T^*}{\lambda_r^*} \qquad (12)$$

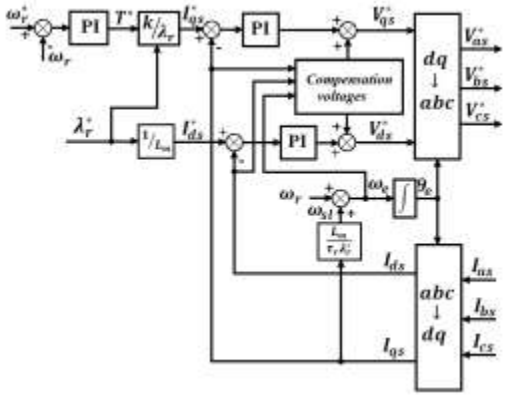

Fig. 15. Block diagram of the IFOC controlled IM

TABLE I

PI CONTROLLERS PARAMETERS EQUATIONS

Speed controller	$k_{p_1} = 2J\xi\omega_n - F$ $k_{i_1} = J\omega_n^2(2\xi^2 - 1)$
Current controller	$k_{p_2} = r_s(2T_m\xi\omega_n - 1_1)$ $k_{i_2} = r_s T_m \omega_n^2(2\xi^2 - 1)$

The slip frequency, ω_{sl}, is given by

$$\omega_{sl} = \frac{L_m}{\tau_r \lambda_r^*} i_{qs}. \qquad (13)$$

The rotor flux angle θ_e which required for coordinate transformation, is generated from the rotor speed, ω_r, and the slip frequency, ω_{sl}, as given by

$$\theta_e = \int (\omega_e + \omega_r)dt. \qquad (14)$$

The torque reference T ∗ is generated by a PI speed controller based on the reference speed ω∗ r and the measured rotor speed ω_r. The rotor flux reference λ_r^* is kept constant at its rated value. The feedback d_q-axis

stator currents i_{ds} and i_{qs} are compared with their references, i_{ds}^* and i_{qs}^*, and the errors are sent to the PI current controllers to generate the stator voltage reference components v'_{ds} and v'_{qs} as indicated in (16), while, the remaining terms in (6) must be added to the output of each controller for voltage compensation [18]

$$v_{ds} = \underbrace{r_s i_{ds} + \sigma L_s \frac{di_{ds}}{dt}}_{v'_{ds}} + \underbrace{\frac{L_m}{L_r}\frac{d\lambda_{dr}}{dt} - \omega_e \sigma L_s i_{qs}}_{v_{ds}^{comp}}$$

$$v_{qs} = \underbrace{r_s i_{qs} + \sigma L_s \frac{di_{qs}}{dt}}_{v'_{qs}} + \underbrace{\omega_e \sigma L_s i_{ds} + \omega_e \frac{L_m}{L_r}\lambda_{dr}}_{v_{qs}^{comp}} \quad (15)$$

The dq-axis voltages in the synchronous frame are then transformed to the three-phase stator voltages v_{as}^*, v_{bs}^*, and v_{cs}^* in the stationary frame for the PWM block. Fig. 13 shows the block diagram of the IFOC controlled IM. The parameters of the speed and current PI controllers are calculated based on Table I, where ξ, ω_n are the desired damping and dynamics response specifications $T_m = \sigma L_s / r_s$, $\sigma = 1 - L_m^2 / L_s L_r$ [19].

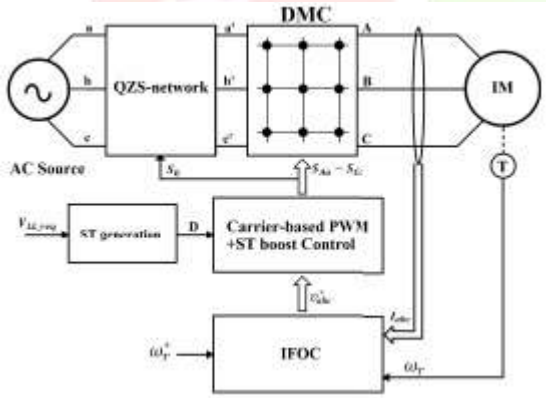

Fig. 16. Block diagram of the proposed QZSDMC-based IM-ASD.

TABLE II

SIMULATION SYSTEM PARAMETERS

Parameter	Value
QZSDMC parameters:	
QZS-network inductance, L	100 µH
QZS-network capacitance, C	10 µF
QZSDMC Switching frequency, F_s	10 kHz
Input voltage source parameters:	
AC input line-to-line RMS voltage	380 V
AC input voltage frequency	50 Hz
Induction Motor parameters:	
Output power	4 kW
RMS line voltage	400 V
Motor frequency	50 Hz
No. of poles, p	4
Stator resistance, R_s	1.405 Ω
Rotor resistance, R_r	1.395 Ω
Stator inductance, L_{ls}	5.839 mH
Rotor inductance, L_{lr}	5.839 mH
Mutual inductance, L_m	172.2 mH
Inertia, J	0.0131 kg. m2
Friction coefficient, F	0.002985 N.m.s

IV. PROPOSED QZSDMC-BASED IM-ASD SYSTEM

The control block diagram of the IM drive system with QZSDMC is shown in Fig. 14. The speed encoder detects the rotor speed to contrast it and the reference speed. The speed controller, a PI controller, manages the speed blunder and produces the required torque reference. The IFOC piece creates the balance signals, vabc, as indicated by the working conditions amid various working modes. The ST obligation proportion, D, is composed by (4), the relating voltage pick up (G) and yield voltage can be acquired to meet the coveted voltage esteem. The bearer based modulator produces the gating signals for the DMC and the extra switches in the QZS-organize.

V. SIMULATION AND REAL-TIME IMPLEMENTATION RESULTS

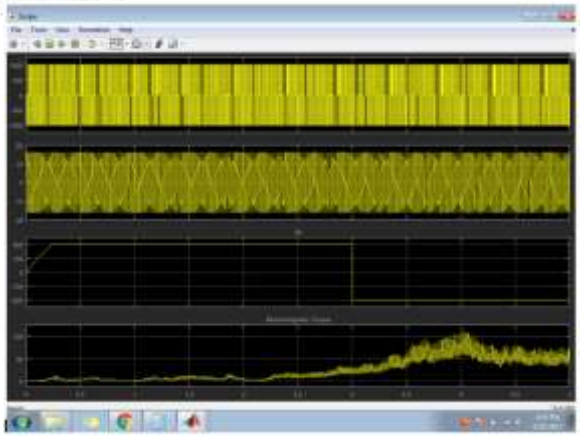

Fig. 17. Motor response during motoring and regenerating operation modes.

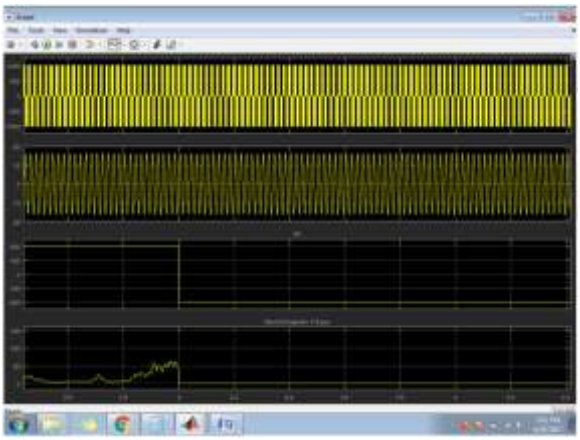

Fig. 18. Motor response during speed reverse

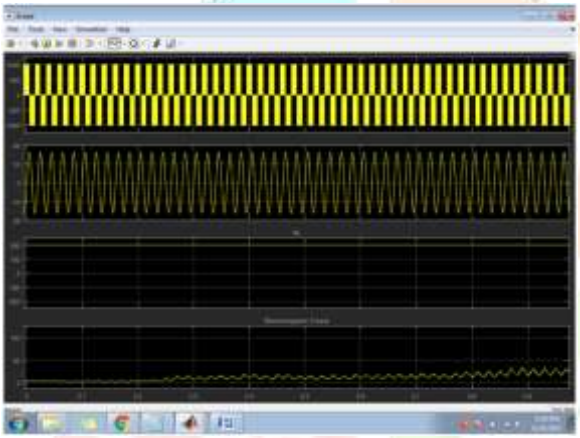

Fig. 19. Steady-state motor current and voltage waveforms during motoring at rated conditions.

VI. CONCLUSION

This paper proposed another four-quadrant vector controlled IM ASD framework in view of the QZSDMC topology. The proposed framework beats the lessened voltage exchange proportion impediments of conventional DMC-based ASD framework, along these lines, the proposed QZSDMC-IM-based ASD will build the use of the DMC in various industry handle the proposed ASD framework can work at full load with little QZSnetwork components. The QZSDMC can accomplish buck and lift operation with lessened number of switches required, subsequently accomplishing minimal effort, high productivity, and unwavering quality, contrasted and the conventional DMCs, what's more, there is no prerequisite of dead time with QZS-organize, consequently recompense of the QZSDMC is less demanding than the customary DMC.

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