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Power Analysis of 2x1Multiplexer using ECRL, MERL, and PFAL Logic

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Abstract:
This paper presents power efficiency of 2x1 Mux using ECRL, MERL and PFALtechnique. A 2x1 multiplexer is designed by using these techniques for the analysis of power dissipation with the variation of supply voltage. All adiabatic schematic of Mux are designed and simulated on mentor graphics VLSI design software Pyxis _v10.5_5_201606075 using 130nm technology.

Keywords:
ECRL, MERL, PFAL and Adiabatic switching.

1. Introduction:

Low power devices or circuits requirements increase the designer interest in CMOS technology, because it has become one of the most dominant technologies for VLSI circuits [1]. The portable device power consumption is a serious issue because of their small chip size with large density of components which in turn increases the switching frequencies and complexity of the circuit. Supply voltage plays an important role in low power circuit designing because supply voltage reduction effectively minimizes the power consumption and dissipation [2].For reduction in supply voltage,the designer have an alternative to minimize the switching capacitance and frequency [3]. The input of dynamic design uses high supply voltage for logic evaluation and low supply voltage for clocking dynamic logic [4]. The power dissipation source in high performance battery based portable digital systems such as note-book, cellular phones etc. have low power consumption is prime requirement, because it directly affect the performance [5].

Traditionally used low power techniqueswerenot sufficient to fulfill the present scenario requirement. Hence, different science and technology domain concepts are being used to optimize the power equation [6]. Power and performance has direct impact on system requirement and system cost.Adiabatic logic approach use constant source current with the reducing energy dissipation possibility during switching events, and reused some of the

energy drawn from the supply. In this approach, most of consumed energy recycled back to power supply as a result, the overall power consumption is reduced [7].

In this paper, a 2x1 multiplexer is designed by using ECRL, MERL and PFAL technologies and their performance analysis such as power dissipation with respect to supply voltage is calculated.

2. Different Adiabatic Logic Designs:

2.1. PFAL 2x1 Multiplexer: A.Vetali in 1996 introduced PFAL (Positive Feedback Adiabatic Logic) Mux. It is unique from other due to its dual rail nature.Its cross-coupled inverter stage helps to maintain its two outputs with two inputs [8],which does not allow degradation of logic level on its two outputs. PFAL is a relatively new logic family which utilizes positive feedback. The functionalblocks of the logic function are realized with NMOS and PMOS transistor parallel connection [9]. PFAL based 2x1 multiplexer schematic is shown below fig.1 and simulation result shown in fig.2.

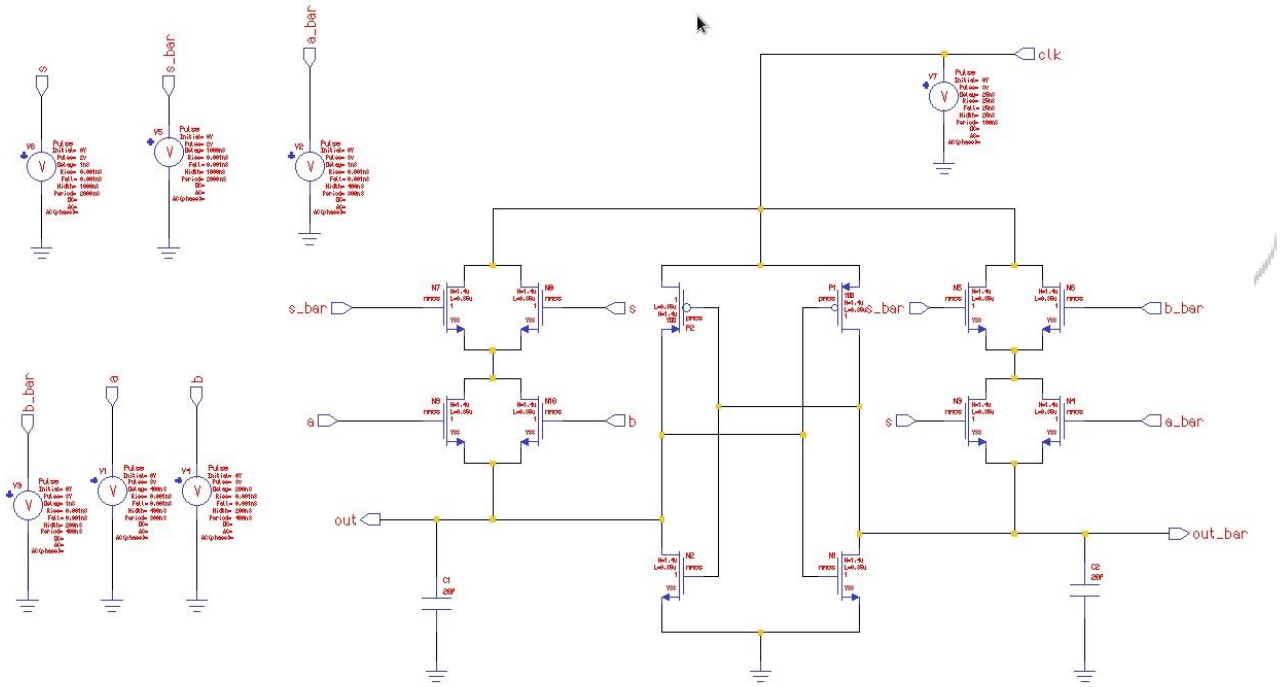

Fig.1: Schematic of PFAL based 2x1 Multiplexer.

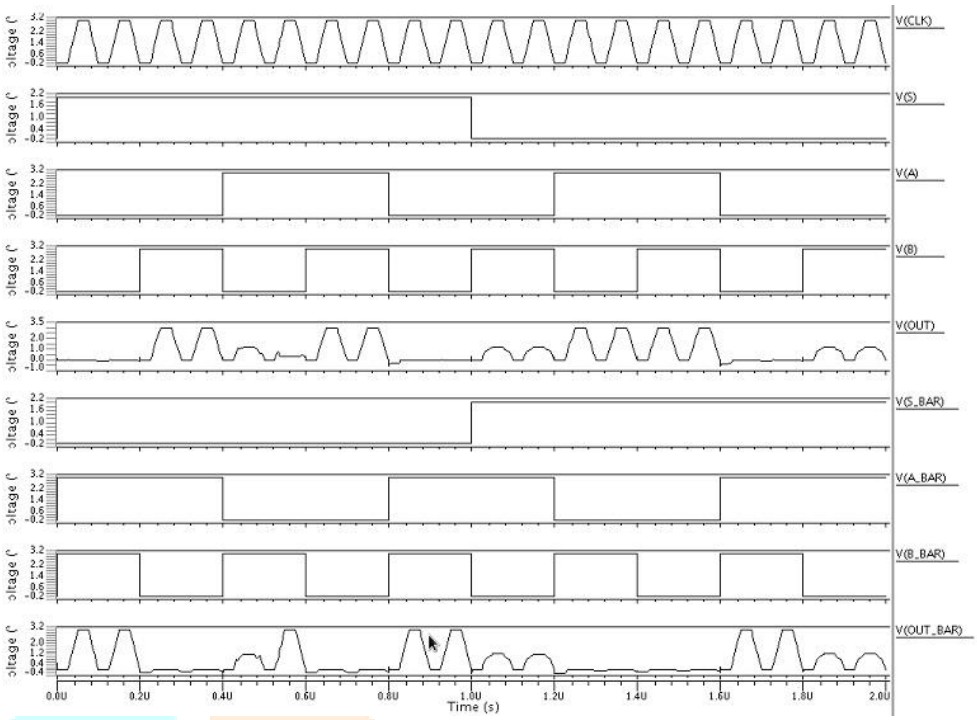

Fig.2: Simulation results of the PFAL 2x1 Multiplexer

When A, A_BAR, B, B_BAR and CLK is 300mV, then OUT=299.9471mV and OUT_BAR=23.2511mV, VSS=233.3215mV, VDD=137.7264mV and total power dissipation=130.6049nW.

When A, A_BAR, B, B_BAR and CLK is 500mV, then OUT=499.9798mV and OUT_BAR=47.3221mV, VSS=180.4326mV, VDD=397.6728mV and total power dissipation=5.5837µW.

When A, A_BAR, B, B_BAR and CLK is 700mV, then OUT=340.7229mV and OUT_BAR=353.0908mV, VSS=207.2225mV, VDD=557.8352mV and total power dissipation=4.1798µW.

When A, A_BAR, B, B_BAR and CLK is 900mV, then OUT=899.9169mV and OUT_BAR=121.8615mV, VSS=218.3235mV, VDD=757.5898mV and total power dissipation=79.4503µW.

When A, A_BAR, B, B_BAR and CLK is 1.1V, then OUT=1.0998V and OUT_BAR=158.7726mV, VSS=231.2737mV, VDD=946.0723mV and total power dissipation=155.0408µW.

When A, A_BAR, B, B_BAR and CLK is 1.4V, then OUT=1.3992V and OUT_BAR=214.7902mV, VSS=272.0891mV, VDD=1.2337V and total power dissipation=320.6193µW.

2.2MERL 2x1 Multiplexer:

For designing of Modified Energy Recovery Logic (MERL) based 2x1 multiplexer 2-PMOS, 14-NMOS, 9-Pulse Voltage source are used. Each voltage source has different configuration then other. MERL based 2x1 multiplexer schematic is shown below fig.3 and simulation result shown in fig.4. In MERL realization the Differential Cascode Voltage Switch Logic (DCVSL) is used due to its potential for complex logic function realization [10]. It has been observed from the figure that, at constant input, power is dissipated during charging or discharging at the output by power clock [11].

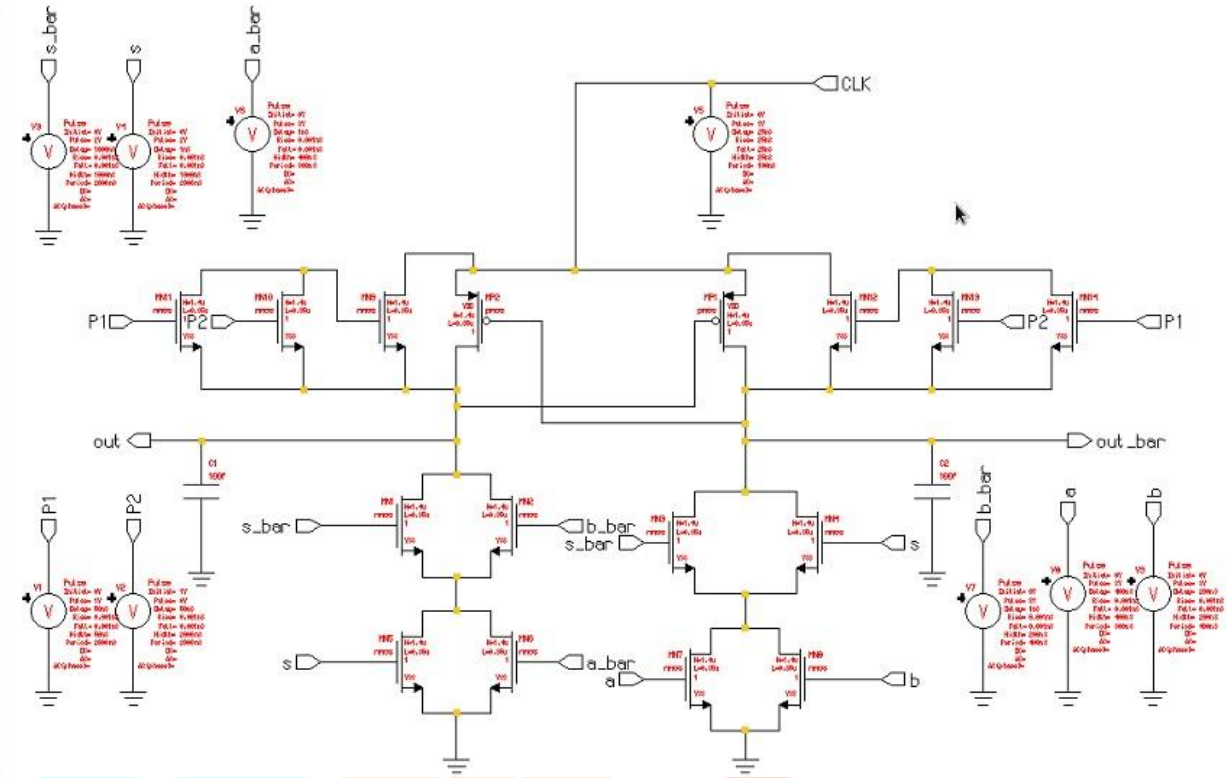

Fig.3: Schematic of MERL based 2x1 Multiplexer

When A, A_BAR, B, B_BAR and CLK is 300mV, then OUT=185.7593mV and OUT_BAR= 183.2562µV, VSS=62.0966mV, VDD=202.4213mV and total power dissipation=169.7724nW.

When A, A_BAR, B, B_BAR and CLK is 500mV, then OUT=57.4978mV and OUT_BAR=21.2088mV, VSS=56.2312mV, VDD=339.5806mV and total power dissipation=7.5756µW.

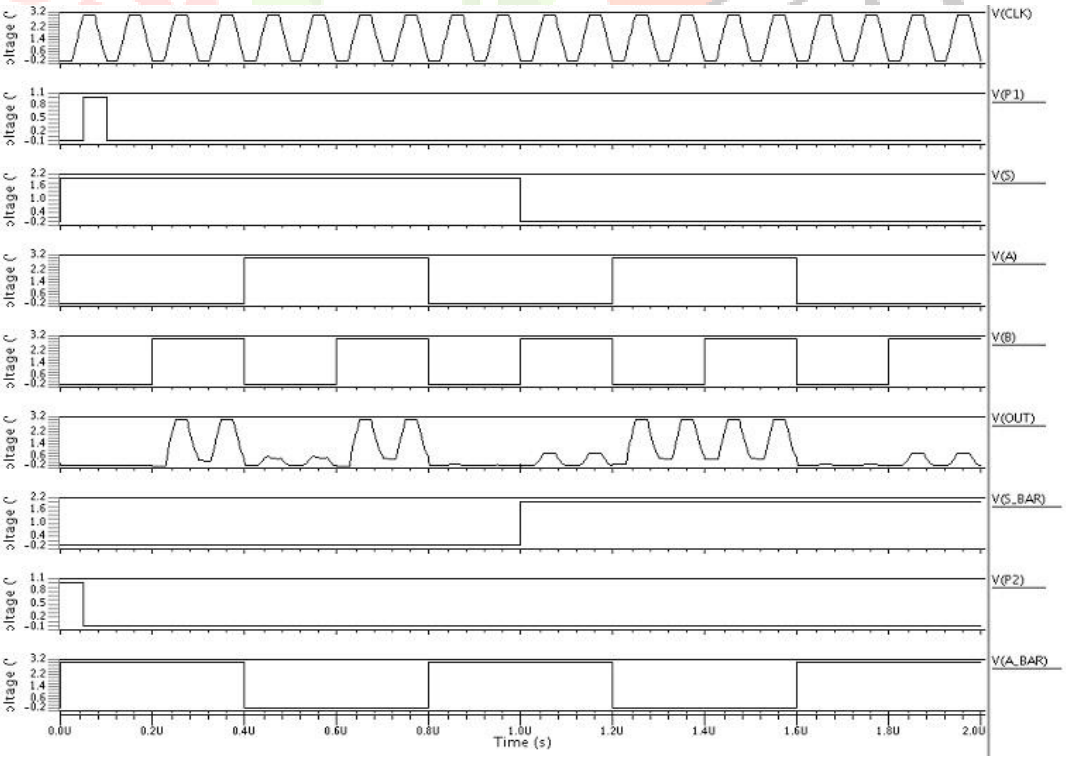

Fig.4: Simulation results of the MERL 2x1 Multiplexer

When A, A_BAR, B, B_BAR and CLK is 700mV, then OUT=76.9006mV and OUT_BAR=49.7249mV, VSS=82.5041mV, VDD=521.6573mV and total power dissipation=35.7103µW.

When A, A_BAR, B, B_BAR and CLK is 900mV, then OUT=102.6478mV and OUT_BAR=90.3288mV, VSS=109.6622mV, VDD=710.8523mV and total power dissipation=90.1129µW.

When A, A_BAR, B, B_BAR and CLK is 1.1V, then OUT=128.4423mV and OUT_BAR=145.2341mV, VSS=133.4688mV, VDD=903.2749mV and total power dissipation=174.0044µW.

When A, A_BAR, B, B_BAR and CLK is 1.4V, then OUT=158.4083mV and OUT_BAR=275.5678mV, VSS=160.0378mV, VDD=1.1953V and total power dissipation=354.5365µW.

2.3ECRL 2x1 Multiplexer:

ECRL (Efficient Charge Recovery Logic) provides a new technique as compared to other adiabatic circuits, because it performs precharge and evaluation in same time and eliminates precharge diode, which results in low power dissipation [12].

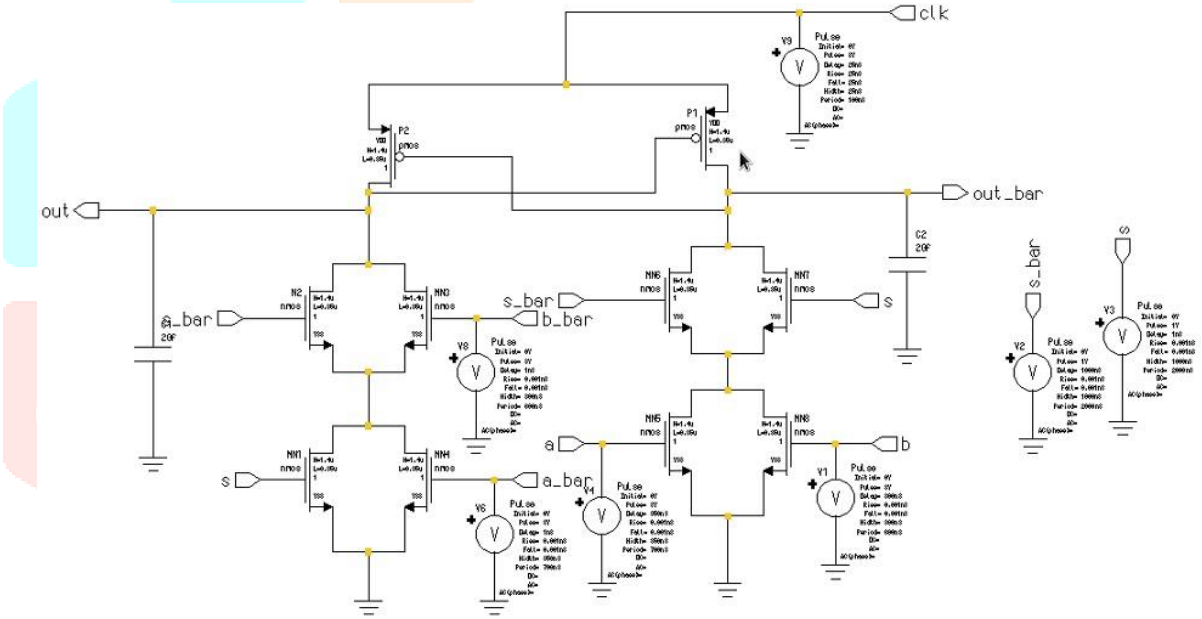

Fig.5: Schematic of ECRL based 2x1 Multiplexer.

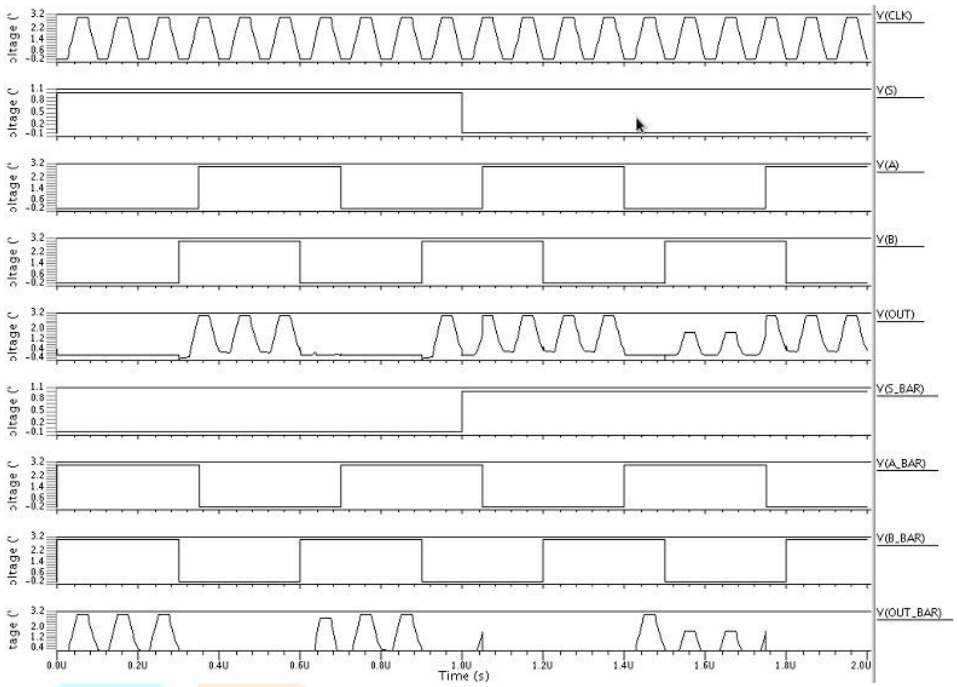

Fig.6: Simulation results of the ECRL 2x1 Multiplexer

The schematic and simulated waveform of the ECRL 2x1 Multiplexer is shown in fig.5 and fig.6 respectively.

When A, A_BAR, B, B_BAR and CLK is 300mV, then OUT=238.7689mV and OUT_BAR= 39.5867µV, VSS=213.6162mV, VDD=28.7863mV and total power dissipation=144.8191nW.

When A, A_BAR, B, B_BAR and CLK is 500mV, then OUT=63.8824mV and OUT_BAR=20.9112mV, VSS=15.9895mV, VDD=339.9928mV and total power dissipation=7.3746µW.

When A, A_BAR, B, B_BAR and CLK is 700mV, then OUT=80.4709mV and OUT_BAR=50.3742mV, VSS=26.5329mV, VDD=521.8222mV and total power dissipation=35.3407µW.

When A, A_BAR, B, B_BAR and CLK is 900mV, then OUT=105.7921mV and OUT_BAR=92.1899mV, VSS=39.6830mV, VDD=710.9884mV and total power dissipation=89.3674µW.

When A, A_BAR, B, B_BAR and CLK is 1.1V, then OUT=130.8464mV and OUT_BAR=149.5059mV, VSS=54.5118mV, VDD=903.4145mV and total power dissipation=172.5618µW.

When A, A_BAR, B, B_BAR and CLK is 1.4V, then OUT=156.7069mV and OUT_BAR=290.8429mV, VSS=80.1463mV, VDD=1.1955V and total power dissipation=350.2022µW.

3. Results and Discussion:

Table.1: Power analysis of ECRL, MERL and PFAL Mux w.r.t Voltage

Supply Voltage	PFAL(µW)	ECRL(µW)	MERL(µW)
0.3	0.1306049	0.1448191	0.1697724
0.5	5.5837	7.3746	7.5756
0.7	4.1798	35.3407	35.7103
0.9	79.4503	89.3674	90.1129
1.1	155.0408	172.5618	174.0044
1.4	320.1693	350.2022	354.5365

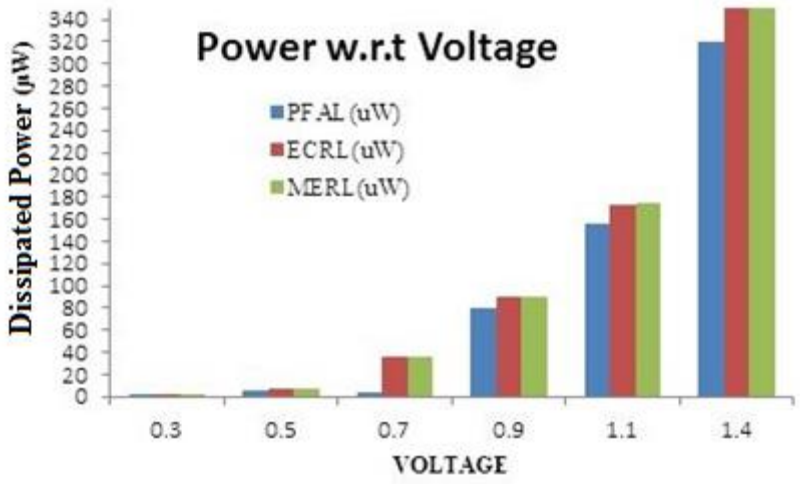

Fig.7: Power Dissipation Graph of ECRL, MERL and PFAL 2x1 Multiplexer

The circuits of 2x1 multiplexer are verified using different input combination for different sets of input voltages. The schematic and simulation results are shown in fig. 1,2 for PFAL, fig. 3,4 for MERL and fig. 5,6 for ECRL respectively. Table1shows power dissipation analysis of above mux circuits w.r.t Voltage and fig. 7 shows graphical power dissipationanalysis of PFAL, MERL and ECRL.

4. Conclusion: The proposed multiplexer circuits are simulated on 130nm technology. From the obtained results, it has been concluded that PFAL technique based multiplexer is more power efficient as compared to MERL and ECRL technique based multiplexer. The power dissipation in PFAL is greatly reduced as compared to ECRL and MERL due to recycling process.

5. References:

[1]. H. J. Veendrick, "Short-Circuit Dissipation of Static CMOSCircuitry and Its Impact on the Designof Buffer Circuits" IEEE, Vol. Sc-19, No.- 4, pp.468-473, August 1984.

[2]. T. Kuroda, M. Hamada, "Low-Power CMOS digital design with dual embedded adaptive power supplies"IEEE, Vol. -35, No.- 4, pp.452-455, April2000.

[3]. V. S. K. Bhaaskaran, "Energy recovery performance of quasi-adiabatic circuits using lower technology nodes" IEEE, 2011.

[4]. S. R. Sahool, K. K. Mahapatra, "Performance analysis of modified feedthrough logic for low and high speed" IEEE, pp.340-344, 30-31March 2012.

[5]. D. Shinghal, A. Saxena, A. Noor, "Adiabatic logic circuits: A Retrospect" MIT-IJECE, Vol-3, No.-2, pp.108-114, August 2013.

[6]. A. K. Bakshi, M. Sharma, "Design of basic gates using ECRL and PFAL" (ICACCI) IEEE, pp.580-585, 2013.

[7]. M. L. Keote, P. T. Karule, "Design and implementation of energy efficient adiabatic ECRL and basic gates"IEEE, pp.87-91, 8-10 Oct. 2015.

[8]. B. Patel, P. Kadam, "Modified PFAL adiabatic technique for low power "Communications on Applied Electronics (CAE)" , pp.40-43, Vol.3-No.7, Dec.-2015.

[9]. S. Alam, S. R. Ghimiray, M. Kumar, "Performance analysis of a 4-bit comparator circuit using different adiabatic logics" IEEE, pp.1-5, 2017.

[10]. N. Singh, S. Deb, "Analysis and Design guidelines for customized logic families in cmos" IEEE International symposium on VLSI Design and Test (VDAT), June 2015.

[11]. H. Sharma, R. Singh, "Comparative power analysis of CMOS and adiabatic logic gates" "IEEE, pp.7-11, 2015.

[12]. C. Venkatesh, A. Mohanapriya and R. S. Anandhi, "Performance analysis of adiabatic techniques using full adder for efficient power dissipation" ,ICTACT JOURNAL ON MICROELECTRONICS,pp.510-514, Vol.04, Issue-01, April 2018.