International Journal of Creative Research Thoughts
Volume 1, Issue.4, April 2013
ISSN:-2320-2882

ORIGINAL ARTICLE

"DESIGNING OF PARAMETERIZED FPGA-BASED GENERAL PURPOSE NEURAL NETWORK"

Mr. Chandrashekhar Kalbande
Ms. Padmaja Ayachit
Ms. Mrunali Dhande
&
Prof. Anil Bavaskar
Dept of Electronics Engg.
Priyadarshini College of Engineering
Nagpur, Maharashtra India

ABSTRACT

The usage of the FPGA (Field Programmable Gate Array) for neural network implementation provides flexibility in programmable systems. For the neural network based instrument prototype in real time application, conventional specific VLSI neural chip design suffers the limitation in time and cost. With low precision artificial neural network design, FPGAs have higher speed and smaller size for real time application than the VLSI design. In addition, artificial neural network based on FPGAs has fairly achieved with classification application. The programmability of reconfigurable FPGAs yields the availability of fast special purpose hardware for wide applications. Its programmability could set the conditions to explore new neural network algorithms and problems of a scale that would not be feasible with conventional processor. The goal of this work is to realize the hardware implementation of neural network using FPGAs. Digital system architecture is presented using Very High Speed Integrated Circuits Hardware Description Language (VHDL) and is implemented in FPGA chip.

INTRODUCTION

It is a computational system inspired by the Structure, Processing Method, Learning Ability of a biological brain. Artificial Neural Networks (ANNs) can solve great variety of problems in areas of pattern recognition, image processing and medical diagnostic. The biologically inspired ANNs are parallel and distributed information processing systems. This system requires the massive parallel computation.

ANN is an information processing system that aims to simulate human brain's architecture and function. It is now a popular subject in many fields and is also a tool in many areas of problem solving. ANNs have been successfully applied to solve problems where conventional methods have been unsuccessful, such as speech recognition and synthesis, image processing and coding, pattern recognition and classification, power load forecasting, interpretation and prediction of financial trends for stock-market, manufacturing of composite structures, processing modeling, monitoring and control etc.

Characteristics of Artificial Neural Networks

A large number of very simple processing neuron-like processing elements. A large number of weighted connections between the elements Distributed representation of knowledge over the connections Knowledge is acquired by network through a learning process.

Reasons for Usage of Artificial Neural Networks

The main reasons for using an Artificial Neural Networks are as follows. It provides Massive Parallelism. A Distributed representation of any system can be developed with enhance Learning ability and Generalization ability of the system. It will also provide Fault tolerance.

Elements of Artificial Neural Networks

- Processing Units

- Topology

- Learning Algorithm

FPGAs are chosen for implementation ANNs with the following reason:
They can be applied a wide range of logic gates starting with tens of thousands up to few millions gates.
They can be reconfigured to change logic function while resident in the system.
FPGAs have short design cycle that leads to fairly inexpensive logic design.
FPGAs have parallelism in their nature. Thus, they have parallel computing environment and allows logic cycle design to work parallel.
They have powerful design, programming and syntheses tools.

Comparison between Software and Hardware Implementation

ANN is an abstract description of human brain. As it is a mathematical model, it can be implemented by integrated circuits or simulated using computer program. Nonetheless, the inherent parallelism embedded in neural network dynamics can be only fully realized in hardware implementation. Neumann-type computers are well-known for ANN simulation. However, the speed of this kind of simulation is constrained when the size of ANN become large. In addition, software simulation is executed sequentially. Many researchers are developing VLSI implementations using various techniques, ranging from digital to analog and even optical. Complete parallel architecture can be realized with ASIC or VLSI, but as ANN design is targeted for certain problem solving, it is a waste to use ASIC or VLSI for implementation. While the primary disadvantages of analog implementation are the inaccurate computations and low design flexibility even though they can possibly provide higher speed with low resource cost, the major problems

ANN with digital architecture are the implementation of the large quantity of multipliers and nonlinear activation function of neurons. Both of them are usually large in size.

Network Architecture

By using of the FPGA features hardware implementation of fully parallel ANN's is possible. In the fully parallel ANN's architecture number of multipliers per neuron equals to number of connections to this neuron and number of the full adders equals to number of connections to the previous layer mines one [9]. For example in 2-4-1 network output neuron have 4 multipliers and 3 adders. In this work a VHDL library were designed for floating point addition fp_add and floating point multiplication fp_mul. But most resources of FPGAs are used by multiplication and addition algorithm. So in fully parallel ANN's must be used low number precision (for example 8 bit). With the low number precision fully parallel network is not suitable for any application. With the using fp_lib (32 bit floating point number precision)in ANN's is suitable for any application. But the architecture has one multipliers and one adders per layer and is not full parallel because of area resource of FPGAs.
In this structure there is one multiplier and one adder per layer. The inputs from previous layer enter the layer parallel and multiplier serially with their corresponding weights. The results of multiplication are stored in their neuron area in the addition
Neural Network Implementation in Hardware Using FPGAs 1109 storage ROM. Multiplied value of per neuron are inputs for adder. The inputs of adder are added serially and each addition are inputs for sigmoid lookup table. The results of look up table are stored for next layer. This ANNs architecture is shown in Figure
2. In this design number of layer and number of neuron are changed easily during the working phase.

Fig.2. Executing multiple instructions from a single program in a single cycle. Multiprocessors (MP) exploit thread-level parallelism (TLP) by executing different threads in parallel on Different processors.

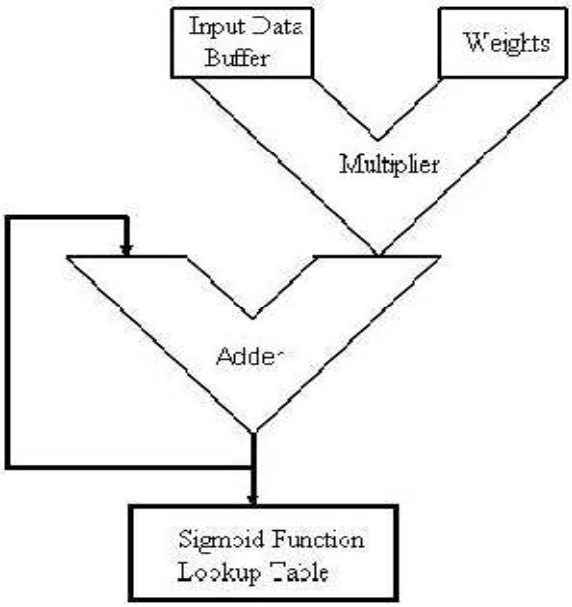

Fig. 2. Block diagram of ANNs

4 Recognizable Neural Networks

Among the recongurable systems currently designed in our laboratory, we present here a hardware implementation of multi-layer perceptrons. These net-works are well-suited for classi_cation problems like hand-written character recognition. Let us briey consider this problem. The network is trained with
a set of characters written by di_erent people. After pre-processing steps (nor-malisation, smoothing,...) we obtain a grey-level image (M x N pixels) of each character. The M x N grey-level values are stored in an input vector to which is assigned a class attribute.
Figure 3 depicts the learning system. An input vector is presented to the neural network which determines an output. The comparison between the com-puted and desired output (class attribute) provides an output error. This signal
is used by a learning algorithm to adapt the network parameters.
We now brief describe the architecture of a multi-layer perceptron. It is composed of several layers of interconnected processing elements (PEs) or neurons:
Learning algorithm
Comparison
Error term

4.1 The Backpropagation Algorithm

The Backpropagation algorithm is widely used for training multi-layer percep-trons [9]. It iteratively computes the values of weights using a gradient descent algorithm.
The Backpropagation algorithm consists of the following stages:
1. Network initialization.
All weights are initialized to small random numbers.
2. Forward propagation.
An input vector is presented and propagated layerwise through the network.
3. Output error computation.
4. Backward propagation.
The output error signal is back-propagated through the network. This pro-cess allows to assign errors to hidden neurons.
5. Weight update.
Previously computed errors (stages 3 and 4) and neuron activations deter-mine the weight changes.
Steps 2 to 5 are carried out for all vectors in the database.
This training process is repeated until the output error signal falls below a predetermined threshold.
When we train a system by example, it is usually impossible to provide every possible input signal. Therefore, an important issue of training is the capabil-ity of the network to generalize to previously unseen patterns. However, the generalization capability depends on the network topology. A rule of thumb for obtaining a good generalization is to use the smallest system that can learn the training vectors.
Unfortunately, the Backpropagation algorithm does not give any information about the topology of the network (number of hidden layers, interconnections, number of neurons). Pruning (or growing) algorithms allow to _nd an optimal topology during training by removing (or adding) neurons and connections.Stands for Symmetric Multi Processing

SOFTWARE AND HARDWARE REQUIREMENT

For Software simulation I will prefer MODELSIM and for synthesis I will be prefer XILINX.
Hardware requirement is SPARTAN-3.

ACKNOWLEDGEMENTS

Authors wish to remark the great task carried out by the Xilinx and Modelsim user guide; and the authors wish to thank Anil Bavaskar for his contribution in the design process.

REFERENCES

[1] I. A. Basheer and M. Hajmeer, "Artificial neural networks: Fundamentals, computing, design, and application," *J. Microbio. Methods, vol.*43, pp. 3–31, Dec. 2000.

[2] Xu Wang, Hong Wang and Wenhui. Wang, Artificial Neural Network Theory and Application, Shenyang: Northeastern University Press,2000. I]M. Ananda Ro and J. Srinivas, Neural Networks Algorithms

[3] A. R. Omondi, "Neurocomputers: a dead end?," *International Journal of Neural Systems*, vol. 10, no. 6, pp.

[4] **J. *C.*** Rajapakse and W. Lu, "Unified approach to independent component neural networks", *Neural Computation*,2000.475-481,2000.

[5] Applications, Alpha Science International Ltd., Part Ill, pp.157, 2003

[6] Maeda, Y.; Tada, T.: "FPGA Implementation of a Pulse Density Neural Network with Learning Ability Using Simultaneous Perturbation", IEEE Transactions on Neural Networks, vol. 14, no. 3,2003, pp. 688-695.

[7] M. Paliwal and U. A. Kumar, "Neural networks and statistical techniques:A review of applications," *Expert Systems With Applications*,vol. 36, pp. 2–17, 2009

[8] Alexander Gomperts, Abhisek Ukil,, *and Franz Zurfluh* "Development and Implementation of FPGA-Based General Purpose Neural Networks for Online Applications" VOL. 7, NO. 1, FEBRUARY 2011.

[9] M. Ananda Ro and J. Srinivas, Neural Networks Algorithms and Applications, Alpha Science International Ltd., Part Ill, pp.157, 2003.