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Study of Schmitt Trigger's Improved Performance in Relation to Power Consumption

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Abstract - ***In order to improve performance in terms of power consumption, speed, magnitude, hysteresis, and dependability, the CMOS device is utilized. The Schmitt trigger circuit improved compatibility with analog components and low voltage power supplies by reducing power dissipation. This is the most efficient approach. This article presents a comparison between a conventional six-transistor (6T) Schmitt trigger and a four-transistor (4T) Schmitt trigger. The Schmitt trigger is designed in such a way that, by adjusting its voltage, the output can be ended to increase prematurely, thereby reducing the output delay with less converting time and less power consumption. The circuit is replicated in the MATLAB tool in both 180nm and 90nm technology, and a simulation result shows.***

Key Words: Schmitt trigger, Threshold voltage, Delay, Power dissipation, Hysteresis.

1. INTRODUCTION

All of these critical conditions necessitate a specific device that will "clean up" or maintain a signal, which is known as the Schmitt trigger [1]. The output state is dependent on the input state and only changes when the input level crosses a predetermined threshold level. Digital circuit is not directly suitable for defining the digital signal. For some reasons, it may have a slow rise or fall time and may have the small noise sensed by proceeding circuitry. The Schmitt trigger device is primarily utilized as a wave shaping device in analog and digital (0 or 1) circuits to address the issue of noise [2]. Additionally, this device is frequently utilized to drive loads with fast switching, low power loss, and low power supply [3]. Schmitt trigger has been utilized unimportant to develop/off (0 or 1) control state [4], and lessen the aversion to commotion, for instance, sensor [3], beat with adjustment circuit [6]. The circuit that makes decisions is SRAM with a Schmitt trigger [27]. A Schmitt trigger is used to convert a slowly changing analog signal voltage into one of several possible binary states based on whether the analog voltage is above or below a preset (preset) threshold voltage. When the input signal goes from vdd to gnd, the threshold voltage of the 6T Schmitt trigger circuit is (VH), and when the input signal goes down to gnd from vdd, the threshold voltage of the conventional Schmitt trigger is VL [15, 16]. The main difference between Schmitt trigger and comparators is demonstrated by their DC transfer characteristics. The inverter is less sensitive to noise than the conventional (6T) Schmitt trigger. This kind of property is known as hysteresis [16], and in addition to Schmitt trigger's display of a difference in switching threshold values for positive and negative edge input signals, comparator displays a single switching threshold. The Schmitt trigger is a positive feedback comparator [5]. Power supply voltage is brought down; Power leakage decreases [25]. The technology can be fully implemented at the circuit level using these methods, which require a lot of changes to the structure of the Schmitt trigger [26]. The MATLAB tool investigated the structural and electronic properties of the Schmitt trigger [28], and all of the results derived in this paper can be transformed into well-known formulas for nanotechnology and electron statistics [29] under certain limiting conditions.

2. CIRCUIT DESCRIPTION

2.1 Conventional Schmitt Trigger The conventional 6T Schmitt trigger is the combination of three PMOS transistor and three NMOS transistor, (i.e. upper PMOS and lower NMOS) and considered as low for each other, the lower two NMOS transistor can be considered as series connection. Schmitt trigger can adjust its threshold in such a way that it can operate after its input exceeds the voltage of vdd/3 [17], The voltage

transfer characteristic exhibits a typical as the show in fig, VOH is maximum output voltage, and VOL is the minimum output voltage. VH is the input voltage at which output switch from VOH to Vol. VL is the input voltage at which output switch from VOL to VOH; ΔH is called the hysteresis width [16]. The voltage is VH, VL, and ΔH.

$$V_H = V_{dd} - R\frac{V_{th}}{(R+1)} \quad (1)$$

$$V_L = \frac{R\,|V_{TP}|}{(R+!)} \quad (2)$$

Where the ratio R= $\sqrt{\beta n/\beta p}$;

The NMOS and PMOS transconductance parameter are βn and βp respectively. When the input is low, only PMOS will be Considered and causes the output to be high (equal to Vdd), during this condition, P1, P2 and P3 are (because VGS < |Vtp| source voltage and gate voltage is equal). Therefore, the output voltage is pulled to Vdd. When the input increases to Vdd, N1, N2 and N3 are turned ON. Thus, the output voltage pulled down to be ground. The PMOS and NMOS ratio is set according to following equation. (3)

$$\frac{W}{Leff}(PMOS) = \gamma\frac{W}{Leff}(NM \quad (3)$$

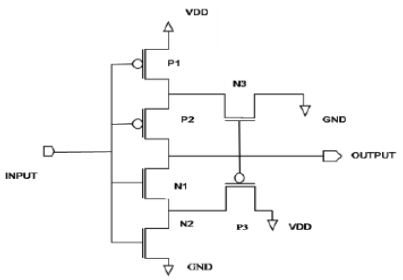

Figure1.The conventional Schmitt trigger

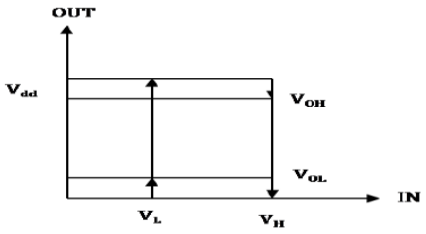

Figure 2. The transfer curve

2.2 4T Schmitt Trigger

The proposed circuit is created by a combination of one PMOS (P1) and three NMOS (N1, N2 and N3), there is no direct connection between power supply and ground as PMOS is connected to power supply and circuit output, beside NMOS is connected to output and ground node, there is no static power due to no direct connection between power supply to be ground.

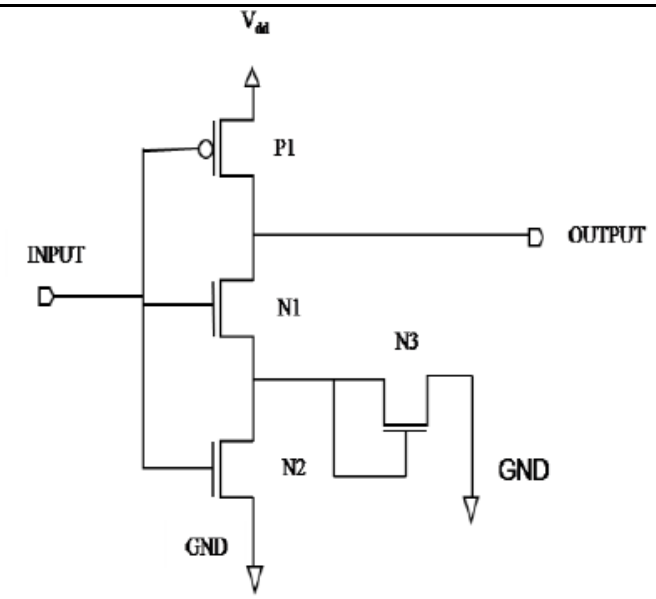

Figure 3. The proposed Schmitt trigger

3. SIMULATION RESULT:

The circuit works simulated in cadence for 180nm and 90nm technology, from the result table, we can observe that 90nm technology, and we are getting effective percentage reduction in delay and power as compared to 180nm technology.

3.1 Propagation Delay The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay, propagation delay time of the Schmitt trigger generally varies as a function with the amplitude of input; a larger input will result in a smaller delay time. The delay time after the circuit is measured as the average of response time of the gate for positive and negative output transition for the sine wave at 1GHz. Delay will reduce when the voltage is increased [13],

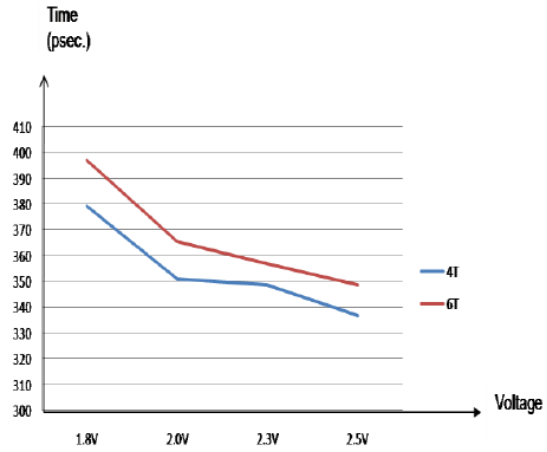

Figure 4 Delay analyses in 180nm technology

The main goal of using the Schmitt trigger in our project, that we can set the threshold limits as per our requirements. Due to observe that 4T Schmitt trigger gives a better performance as compared to 6T conventional Schmitt trigger, due to lower threshold voltage of the Schmitt trigger, we can observe that the signal rise and fall time lower provides a fast signal propagation and less delay in 90nm technology.

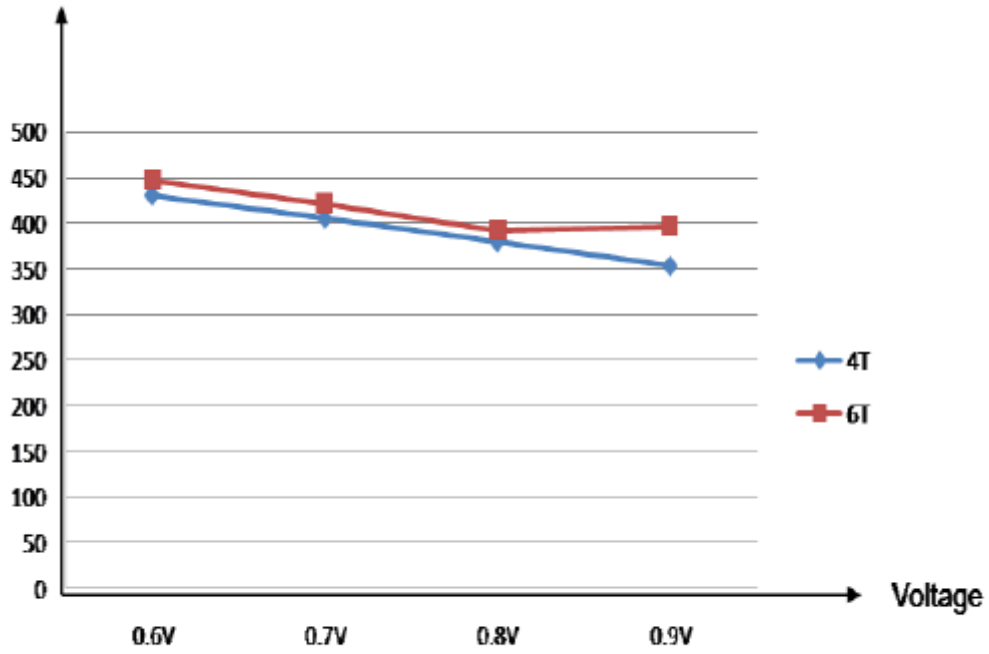

Figure 5 Delay analyses in 90nm technology

3.2 Hysteresis

Hysteresis is the property of quality of the Schmitt trigger, in which the input threshold change depending on whether the input is rising or falling, in another way hysteresis is the difference between the input signal level at which a Schmitt trigger is standby mode and active mode(OFF and ON state)[16], The little bit amount of hysteresis can be useful in a Schmitt trigger circuit because it reduces the circuit sensitivity to noise and helps reduces multiple transition of output when changing state.

$$\Delta H = V_H - V_L \quad (4)$$

$$V_H = 1.528V, V_L = 0.651V, \Delta H = 0.877V \quad (5)$$

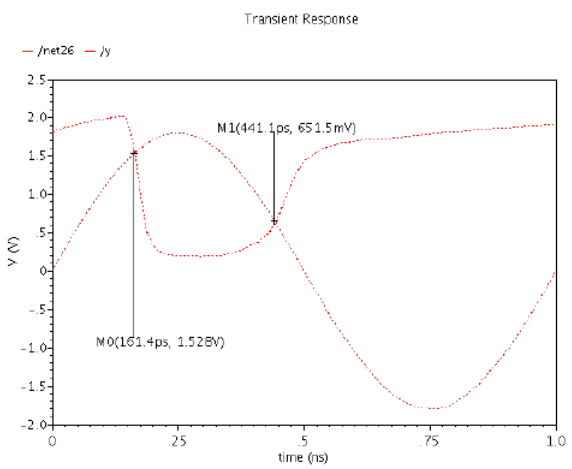

Figure 6 Hysteresis measurement of the Schmitt trigger

3.3 Power Analysis

In the Schmitt trigger either the transistors are in off mode or in on mode due to the early switching of opposite level [13], for the 180nm technology, as shown in fig, with 4T Schmitt trigger in consumes a power off 7. 38pw and with conventional Schmitt trigger, it consumes 8. 88pw power, so, we achieved a power reduction of 16.89% in this case. In 90nm technology, for the same example with 4T Schmitt trigger, it consumes a power of 1. 67pw and with 6T, conventional Schmitt trigger; it consumes 2.2pw power, so we achieved a power reduction of 24% using the 4T Schmitt trigger. It can we observe that in 90nm technology, more power reduction in comparison to 180nm technology. And also varied supply voltage and shows the change in power for both 180nm and 90nm technology as shown in figure. Power in 6T in 90nm

technology= 2.2pw, Power in 4T in 90nm technology= 1.67pw, % Reduction in power = (2.2-1.67) / 2.2pw X 100 = 24%

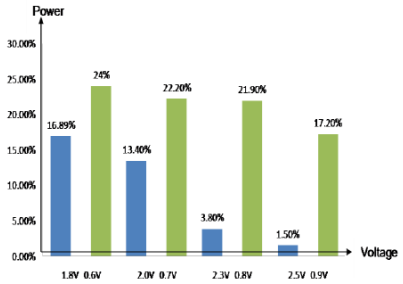

Figure 7 Power reduction graph in 180nm and 90nm technology

Table 1: Show the parameter of 6 transistor on 180nm

Voltage (Vdd)	Delay	Leakage Power	Hysteresis
1.8V	396.9Psec	8.88PW	0869V
2.0V	365.2Psec	15.33PW	0.836V
2.3V	356.8Psc	132.4PW	0.72V
2.5V	348.5Psec	235.6PW	0.58V

Table 2: Show the parameter of 6 transistor on 90nm

Voltage (Vdd)	Delay	Leakage Power	Hysteresis
0.6V	447.3Psec	2.2PW	649.61mV
0.7V	421.6Psec	9.9PW	592.01mV
0.8V	396.6Psec	18.29PW	511.6mV
0.9V	372.5Psec	19.29PW	444mV

Table 3: Show the parameter of 4 transistors on 180nm

Voltage (Vdd)	Delay	Leakage Power	Hysteresis
1.8V	379.3Psec	7.38PW	0.583V
2.0V	350.9Psec	13.27PW	0.538V
2.3V	348.0Psec	127.28PW	0.488V
2.5V	336.8Psec	232.0PW	0.429V

Table 4: Show the parameter of 4 transistor in 90nm

Voltage (Vdd)	Delay	Leakage Power	Hysteresis
0.6V	430.7Psec	1.67PW	572.35mv
0.7V	405.5Psec	7.7PW	499.1mV
0.8V	379.7Psec	17.28PW	441.3mV
0.9V	353.2Psec	15.97PW	349.2mV

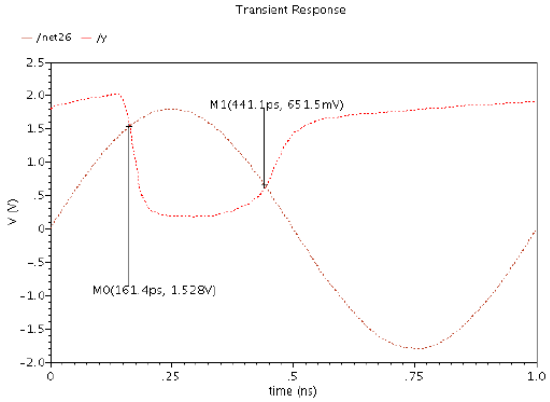

Figure 8 Transfer characteristic of 6T Schmitt trigger in 180nm

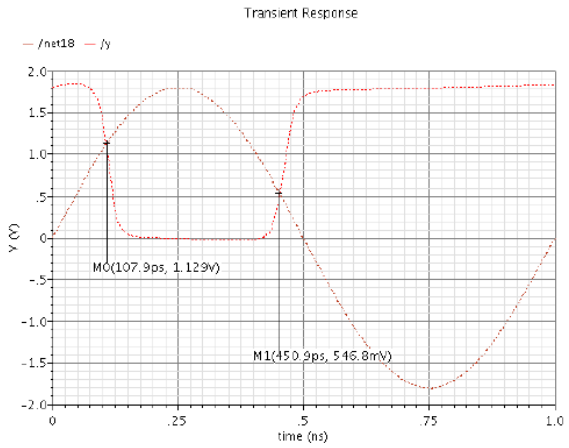

Figure 9 Transfer characteristic of the 4T Schmitt trigger in 180nm

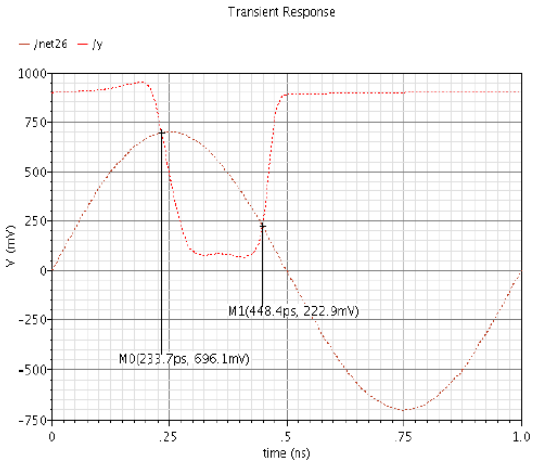

Figure 10 Transfer characteristic of the 6T Schmitt trigger in 90 nm

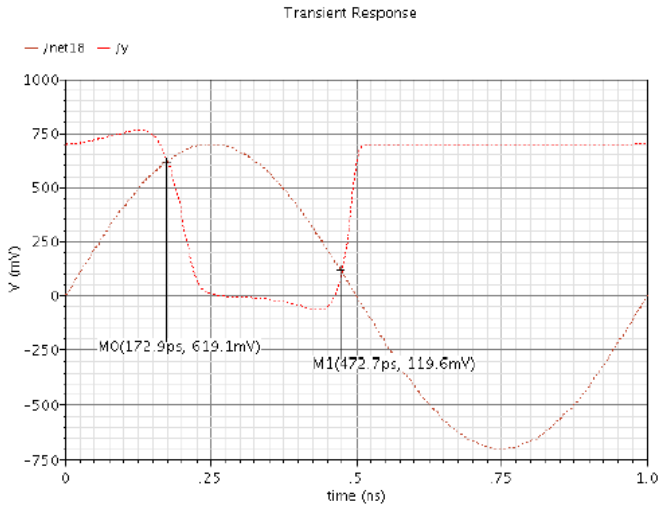

Figure 11 Transfer characteristic of the 4T Schmitt trigger in 90nm

CONCLUSION:

This work proposed Schmitt trigger is modified by using four transistors having less average power consumption with decreases in area; delay is also decreased by using only one PMOS as because delay is more concentrated to PMOS due to less mobility of holes compared to electrons, proposed Schmitt trigger is created by using 4transistor and have better performance than the conventional Schmitt trigger as there are fewer transistor counts by which area is reduced and delay is also reduced; the average power consumption of the proposed Schmitt trigger is less in comparison to the conventional Schmitt trigger, measured result correctly verified the principle of operation and characteristic of the low-power Schmitt trigger circuit. The circuit has been used for the design of low power.

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