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The Board of  
International Journal of Creative Research Thoughts  
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**Banuri Prabhavathi Devi**

In recognition of the publication of the paper entitled  
**Low Power VLSI design of 4-Bit CEPAL adder using Cadence 0.18 $\mu$ M  
CMOS Full adder**

Published In IJCRT ( [www.ijert.org](http://www.ijert.org) ) & 7.97 Impact Factor by Google Scholar

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